REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add JESD51-5 information to paragraph 2. Add sentence to note 2 as specified under figure 1. Update boilerplate paragraphs to current requirements. - ro	11-08-15	C. SAFFLE
B	Under the SS/SD pin, delete 0.7 V and replace with 0.85 V as specified on figure 3. - ro	12-03-30	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 05-09-19	**CHECKED BY** TOM HESS **APPROVED BY** RAYMOND MONNIN	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, WIDE INPUT SYNCHRONOUS BUCK CONTROLLER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/05617**
	REV B	**PAGE** 1 **OF** 15

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance wide input synchronous buck controller microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05617	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS40055-EP	Wide input synchronous buck controller sources/sinks output current
02	TPS40054-EP	Wide input synchronous buck controller sources output current only
03	TPS40057-EP	Wide input synchronous buck controller sources/sinks output current with V_{OUT} prebiased before controller is enabled

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-153	Plastic small outline package with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage range (V_{IN}) :

V_{IN} pin	45 V
V_{FB}, SS, SYNC pins	-0.3 V to 6 V
SW pin	-0.3 V to 45 V
SW pin, transient < 50 ns	-2.5 V
KFF pin, with $I_{IN(max)}$ = -5 mA	-0.3 V to 11 V
Output voltage range (V_{OUT}) for COMP, RT, and SS pins	-0.3 V to 6 V
Input current (I_{IN}) for KFF pin	5 mA
Output current (I_{OUT}) for RT pin	200 μA
Operating junction temperature range (T_J)	-55°C to +140°C
Storage temperature range (T_{STG})	-55°C to +150°C 2/
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Thermal resistance, junction to case (θ_{JC})	26.6°C/W
Thermal resistance, junction to ambient (θ_{JA})	36.5°C/W 3/ 4/
Thermal resistance, junction to bottom of thermal pad (θ_{JP})	2.1°C/W 3/
Junction to top thermal parameter (ϕ_{JT})	0.848°C/W 3/ 4/

1.4 Recommended operating conditions. 5/

Input voltage range (V_{IN})	8 V to 40 V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
3/ See technical brief SLMA002 – Power pad thermally enhanced package.
4/ Tested in accordance with the thermal metric definitions of EIA/JESD51-5.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
JESD51-5 - Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input supply section							
Input voltage range	V_{IN}		-55°C to +125°C	01,02, 03	8	40	V
Operating current section							
Quiescent current	I_{DD}	Output drivers not switching, $V_{FB} \geq 0.75$ V	-55°C to +125°C	01,02, 03		3.3	mA
BP5 section							
Output voltage	V_{BP5}	$I_{OUT} \leq 1$ mA	-55°C to +125°C	01,02, 03	4.7	5.3	V
Oscillator/ramp generator section 3/							
Accuracy	f_{OSC}	$8 \text{ V} \leq V_{IN} \leq 40$ V	-55°C to +125°C	01,02, 03	465	585	kHz
PWM ramp voltage 4/	V_{RAMP}	$V_{PEAK} - V_{VAL}$	-55°C to +125°C	01,02, 03	2 typical		V
High level input voltage, SYNC pin	V_{IH}		-55°C to +125°C	01,02, 03	2	5	V
Low level input voltage, SYNC pin	V_{IL}		-55°C to +125°C	01,02, 03		0.8	V
Input current, SYNC pin	I_{SYNC}		-55°C to +125°C	01,02, 03		11	µA
Pulse width, SYNC pin			-55°C to +125°C	01,02, 03	50		ns
RT voltage	V_{RT}		-55°C to +125°C	01,02, 03	2.37	2.59	V
Maximum duty cycle		$V_{FB} = 0$ V, $f_{SW} \leq 500$ kHz	-55°C to +125°C	01,02, 03	84%	94%	
		$V_{FB} = 0$ V, 4/ 500 kHz $\leq f_{SW} \leq$ 1 MHz			80%		
Minimum duty cycle		$V_{FB} \geq 0.75$ V	-55°C to +125°C	01,02, 03		0%	
Feed forward voltage	V_{KFF}		-55°C to +125°C	01,02, 03	3.35	3.7	V
Feed forward current operating range	I_{KFF}	4/	-55°C to +125°C	01,02, 03	20	1200	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Soft start section							
Soft start source current	I_{SS}		-55°C to +125°C	01,02, 03	1.2	3.6	µA
Soft start clamp voltage	V_{SS}		-55°C to +125°C	01,02, 03	3.7 typical		V
Discharge time	t_{DSCH}	C_{SS} = 200 pF	-55°C to +125°C	01,02, 03	1.4	3.4	µs
Soft start time	t_{SS}	C_{SS} = 220 pF, 0 V ≤ V_{SS} ≤ 1.6 V	-55°C to +125°C	01,02, 03	102	230	µs
BP10 section							
Output voltage	V_{BP10}	I_{OUT} ≤ 1 mA	-55°C to +125°C	01,02, 03	8.9	10.45	V
Error amplification section							
Feedback input voltage	V_{FB}	8 V ≤ V_{IN} ≤ 40 V	+25°C	01,02, 03	0.698	0.704	V
		8 V ≤ V_{IN} ≤ 40 V	0°C ≤ T_A ≤ 125°C		0.689	0.717	
		8 V ≤ V_{IN} ≤ 40 V	-55°C ≤ T_A ≤ 125°C		0.689	0.719	
Gain bandwidth	G_{BW}	4/	-55°C to +125°C	01,02, 03	2.8		MHz
Open loop gain	A_{VOL}		-55°C to +125°C	01,02, 03	40		dB
High level output source current	I_{OH}		-55°C to +125°C	01,02, 03	1.85		mA
Low level output source current	I_{OL}		-55°C to +125°C	01,02, 03	1.95		mA
High level output voltage	V_{OH}	I_{SOURCE} = 500 µA	-55°C to +125°C	01,02, 03	3.1		V
Low level output voltage	V_{OL}	I_{SINK} = 500 µA	-55°C to +125°C	01,02, 03		0.37	V
Input bias current	I_{BIAS}	V_{FB} = 0.7 V	-55°C to +125°C	01,02, 03		220	nA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Current limit section							
Current limit sink current	I_{SINK}		-55°C to +125°C	01,02, 03	7.5	12.2	µA
Propagation delay to output		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 0.5 V)	-55°C to +125°C	01,02, 03	300 typical		ns
		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 2 V)			200 typical		
Switch leading edge blanking pulse time	t_{ON}	4/	-55°C to +125°C	01,02, 03	100		ns
Off time during a fault	t_{OFF}		-55°C to +125°C	01,02, 03	7 typical		cycles
Offset voltage SW versus ILIM	V_{OS}	V_{ILIM} = 23.6 V	+25°C	01,02, 03	-115	-50	mV
		V_{ILIM} = 23.6 V	0°C ≤ T_A ≤ 125°C		-155	-38	
		V_{ILIM} = 23.6 V	-55°C ≤ T_A ≤ 125°C		-155	-10	
		V_{ILIM} = 11.6 V	+25°C		-118	-43	
		V_{ILIM} = 11.6 V	0°C ≤ T_A ≤ 125°C		-160	-45	
		V_{ILIM} = 11.6 V	-55°C ≤ T_A ≤ 125°C		-160	-15	
Output driver section							
Low side driver rise time	t_{LRISE}	C_{LOAD} = 2200 pF	-55°C to +125°C	01,02, 03		110	ns
Low side driver fall time	t_{LFALL}	C_{LOAD} = 2200 pF	-55°C to +125°C	01,02, 03		58	ns
High side driver rise time	t_{HRISE}	C_{LOAD} = 2200 pF, (HDRV – SW)	-55°C to +125°C	01,02, 03		105	ns
High side driver fall time	t_{HFALL}	C_{LOAD} = 2200 pF, (HDRV – SW)	-55°C to +125°C	01,02, 03		82	ns
High level output voltage, HDRV pin	V_{OH}	I_{HDRV} = -0.1 A (HDRV – SW)	-55°C to +125°C	01,02, 03	BOOST -1.9		V
Low level output voltage, HDRV pin	V_{OL}	I_{HDRV} = 0.1 A (HDRV – SW)	-55°C to +125°C	01,02, 03		0.85	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output driver section - Continued							
High level output voltage, LDRV pin	V_{OH}	I_{LDRV} = -0.1 A	-55°C to +125°C	01,02, 03	BP10 - 1.8		V
Low level output voltage, LDRV	V_{OL}	I_{LDRV} = 0.1 A	-55°C to +125°C	01,02, 03		0.6	V
Minimum controllable pulse width			-55°C to +125°C	01,02, 03		160	ns
SS/SD shutdown section							
Shutdown threshold voltage	V_{SD}	Outputs off	-55°C to +125°C	01,02, 03	85	170	mV
Device active threshold voltage	V_{EN}		-55°C to +125°C	01,02, 03	180	260	mV
Boost regulator section							
Output voltage	V_{BOOST}	V_{IN} = 24 V	-55°C to +125°C	01,02, 03	30.8	33.9	V
Rectifier zero current comparator section							
Switch voltage	V_{SW}	LDRV output OFF	-55°C to +125°C	02	-10	0	mV
SW node section							
Leakage current 4/	I_{LEAK}		-55°C to +125°C	01,02, 03		35	µA
Thermal shutdown section							
Shutdown temperature	T_{SD}	4/	-55°C to +125°C	01,02, 03	165 typical		°C
Hysteresis	T_{SD}	4/	-55°C to +125°C	01,02, 03	20 typical		°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Undervoltage lockout (UVLO) section							
KFF programmable threshold voltage	V_{UVLO}	R_{KFF} = 28.7 kΩ	-55°C to +125°C	01,02, 03	6.85	7.95	V
UVLO, fixed	V_{DD}		-55°C to +125°C	01,02, 03	7.05	7.9	V
UVLO, hysteresis	V_{DD}		-55°C to +125°C	01,02, 03	0.46 typical		V

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, T_A = -55°C to +125°C, V_{IN} = 24 V dc, R_T = 90.0 kΩ, I_{KFF} = 150 μA, f_{SW} = 500 kHz, all parameters at zero power dissipation.

3/ I_{KFF} increases with SYNC frequency, I_{KFF} decreases with maximum duty cycle.

4/ Ensured by design. Not production tested.

Case X

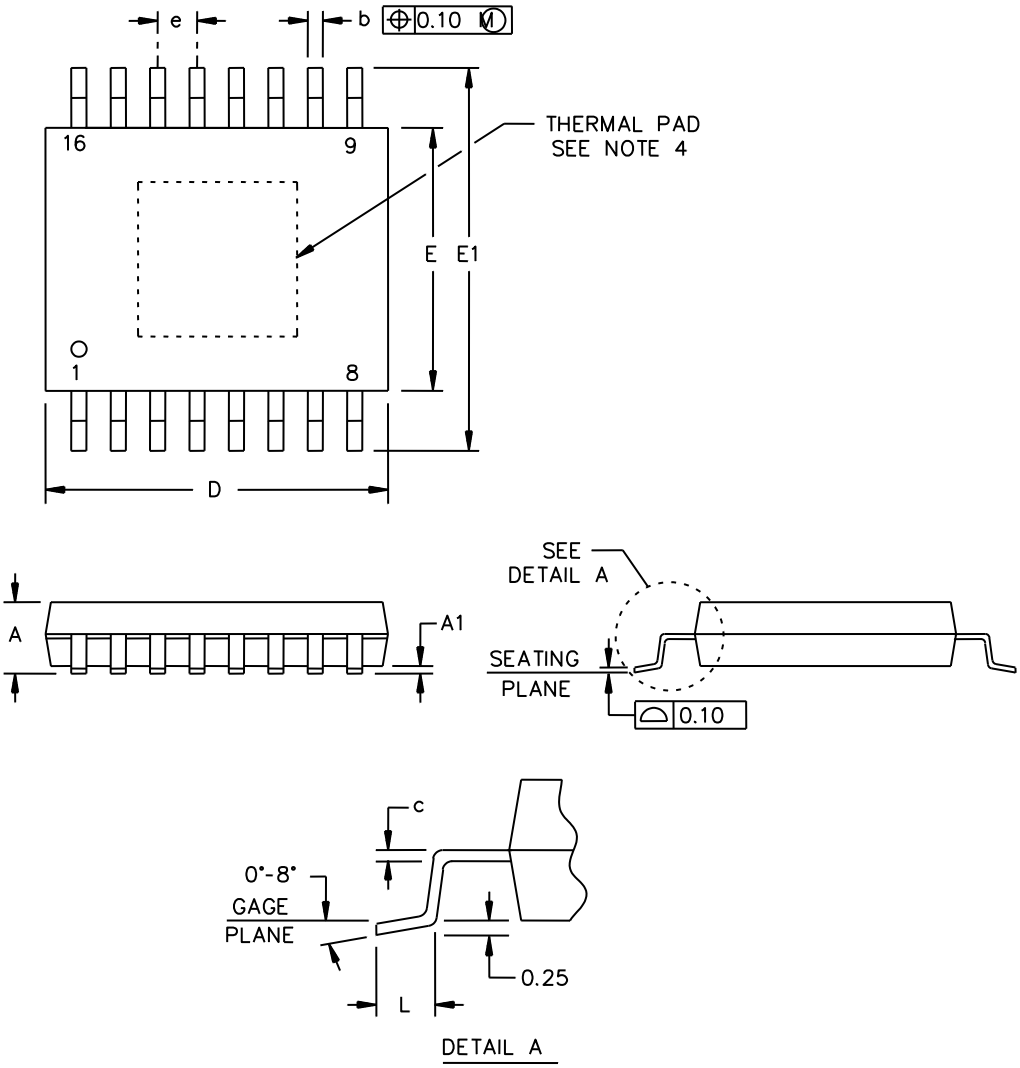

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE **A**	CODE IDENT NO. **16236**	DWG NO. **V62/05617**
		REV B	PAGE 10

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.004	---	1.20
A1	0.001	0.005	0.05	0.15
b	0.007	0.011	0.19	0.30
c	0.005 NOM		0.15 NOM	
D	0.192	0.200	4.90	5.10
E	0.169	0.177	4.30	4.50
E1	0.244	0.259	6.20	6.60
e	0.025 BSC		0.65 BSC	
L	0.019	0.029	0.50	0.75
n	16		16	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed (0.005 inch) 0.15 mm per side.
3. Falls within JEDEC MO-153.
4. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout.

FIGURE 1. Case outline – Continued.

Device types	01, 02, 03		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	KFF	I	A resistor is connected from this pin to V_{IN} to program the amount of voltage feed forward. The current fed into this pin is internally divided and used to control the slope of the PWM ramp.
2	RT	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
3	BP5	O	5 V reference. This pin should be bypassed to ground with a 0.1 μF ceramic capacitor. This pin may be used with an external dc load of 1 mA or less.
4	SYNC	I	Synchronization input for the device. This pin can be used to synchronize the oscillator to an external master frequency. If synchronization is not used, connect this pin to SGND.
5	SGND	---	Signal ground reference for the device.
6	SS/SD	I	Soft start programming pin. A capacitor connected from this pin to ground programs the soft start time. The capacitor is charged with an internal current source 2.3 μA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. The output voltage begins to rise when $V_{SS/SD}$ is approximately 0.85 V. The output continues to rise and reaches regulation when $V_{SS/SD}$ is approximately 1.55 V. The controller is considered shut down when $V_{SS/SD}$ is 125 mV or less. All internal circuitry is inactive. The internal circuitry is enabled when $V_{SS/SD}$ is 210 mV or greater . When $V_{SS/SD}$ is less than approximately 0.85 V, the outputs cease switching and the output voltage (V_{OUT}) decays while the internal circuitry remains active
7	V_{FB}	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage, 0.7 V.
8	COMP	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the V_{FB} pin to compensate the overall loop. The COMP pin is internally clamped above the peak of the ramp to improve large signal transient response.

FIGURE 2. Terminal connections.

Device types	01, 02, 03		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
9	PGND	---	Power ground reference for the device. There should be a low impedance path from this pin to the source(s) of the lower MOSFET(s).
10	LDRV	O	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
11	BP10	O	10 V reference used for gate drive of the N-channel synchronous rectifier. This pin should be bypassed by a 1 μF ceramic capacitor. This pin may be used with an external dc load of 1 mA or less.
12	SW	I	This pin is connected to the switched node of the converter and used for over current sensing. Device types 02 and 03 versions use this pin for zero current sensing as well.
13	HDRV	O	Floating gate driver for the high side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
14	BOOST	O	Gate drive voltage for the high side N channel MOSFET. The BOOST voltage is 9 V greater that the input voltage. A 0.1 μF ceramic capacitor should be connected from this pin to the drain of the lower MOSFET.
15	V_{IN}	I	Supply voltage for the device.
16	ILIM	I	Current limit pin used to set the over current threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor from this pin to V_{CC}. The voltage on this pin is compared to the voltage drop (V_{IN} – SW) across the high side MOSFET during conduction.

FIGURE 2. Terminal connections – Continued.

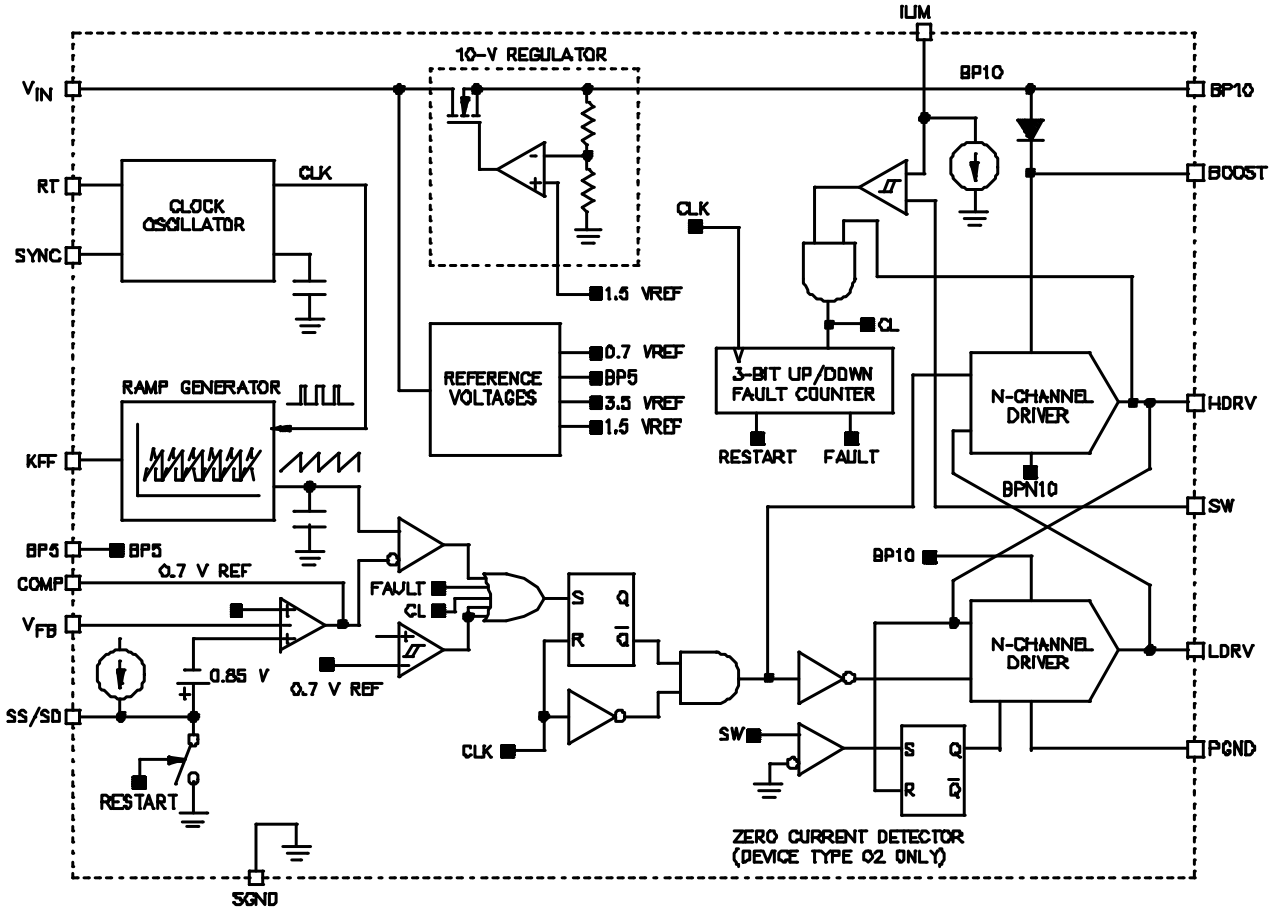

FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package	Application 2/	Vendor part number
V62/05617-01XE	01295	Plastic HTSSOP (PWP)	Source	TPS40055MPWPREP
V62/05617-02XE	3/	Plastic HTSSOP (PWP)	Source / sink	TPS40054MPWPREP
V62/05617-03XE	3/	Plastic HTSSOP (PWP)	Source / sink with prebias	TPS40057MPWPREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ The PWP package is also available taped and reeled. Add an R suffix to the device type (for example, TPS40054PWPR). See the application of the data sheet for power pad drawing and layout information.
3/ Product preview. For additional ordering and product information, please visit http://www.ti.com.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493