REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02. Update boilerplate to current revision. - CFS	06-08-07	Thomas M. Hess
B	Make changes to $I_{O(src)}$, t_{DELAY}, and I_{SU} tests as specified under Table I. - ro	10-09-28	C. SAFFLE
C	Add paragraph 1.5 Dissipation ratings. Add Outputs (OUTA, OUTB limits) limits to paragraph 1.3. Add footnote 2/ to storage temperature limit under paragraph 1.3. Add sentence to CLK/LEB terminal description under figure 2. Update document paragraphs to current requirements. - ro	17-02-07	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**		C	C	C	C	C	C	C	C	C	C	C	C	C						
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 05-08-30	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, HIGH SPEED, PULSE WIDTH MODULATOR CONTROLLER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/05616**
	REV C	**PAGE** 1 **OF** 13

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AMSC N/A

5962-V017-17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high speed, pulse width modulator (PWM) controller microcircuit, with an operating temperature range of -40°C to +125°C for device type 01, and -55° to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	UC2825A-EP	High speed, PWM controller
02	UC2825A-EP	High speed, PWM controller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-013 AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{IN}) (V_C and V_{CC} pins) ..... 22 V
Source or sink current, dc (I_O) (OUTA and OUTB pins) ..... 0.5 A
Source or sink current, pulse 0.5 μs (I_O) (OUTA and OUTB pins) ..... 2.2 A
Analog inputs:
  INV, NI, and RAMP pins ..... -0.3 V to 7 V
  ILIM, and SS pins ..... -0.3 V to 6 V
Power ground (PGND pin) ..... ±0.2 V
Outputs (OUTA, OUTB limits) ..... PGND -0.3 V to V_C +0.3 V
Clock output current (I_{CLK}) (CLK/LEB pins) ..... -5 mA
Error amplifier output current ($I_{O(EA)}$) (EAOUT pin) ..... 5 mA
Soft start sink current (I_{SS}) (SS pin) ..... 20 mA
Oscillator charging current (I_{OSC}) (RT pin) ..... -5 mA
Operating virtual junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature (T_{stg}) ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... -55°C to +150°C
Storage temperature (T_{STG}) ..... -65°C to +150°C 2/
Lead temperature 1.6 mm (1/16 inch) from cases for 10 seconds ..... +300°C

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{IN}) ..... 12 V
Operating free-air temperature range (T_A):
  Device type 01 ..... -40°C to +125°C
  Device type 02 ..... -55°C to +125°C

1.5 Dissipation ratings. Free air temperature.

Package	Air flow (CFM)	Power rating $T_A < 25°C$	Derating factor above $T_A = 25°C$	Power rating $T_A = 70°C$	Power rating $T_A = 85°C$	Power rating $T_A = 125°C$
Case X	0	1.105 W	9.62 mW/°C	673 mW	528 mW	144 mW

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Reference, V_{REF} section							
Output voltage range	V_O	I_O = 1 mA, T_J = 25°C	25°C	All	5.05	5.15	V
Line regulation	LN	12 V ≤ V_{CC} ≤ 20 V	3/	All		15	mV
Load regulation	LD	1 mA ≤ I_O ≤ 10 mA	3/	All		20	mV
Total output variation		Line, load, temperature	3/	All	5.03	5.17	V
Temperature stability 4/		$T_{(min)} < T_A < T_{(max)}$	3/	All		0.4	mV/°C
Output noise voltage 4/		10 Hz < f < 10 kHz	3/	All	50 typical		μV_{RMS}
Long term stability 4/		1000 hours, T_J = 125°C	125°C	All		25	mV
Short circuit current	I_{OS}	V_{REF} = 0 V	3/	All	30	90	mA
Oscillator section							
Initial accuracy 4/	f_{OSC}	T_J = 25°C	25°C	All	375	425	kHz
		R_T = 6.6 kΩ, C_T = 220 pF, T_A = 25°C			0.9	1.1	MHz
Total variation 4/		Line, temperature	3/	All	350	450	kHz
		R_T = 6.6 kΩ, C_T = 220 pF			0.85	1.15	MHz
Voltage stability		12 V < V_{CC} < 20 V	3/	All		1%	
Temperature stability 4/		$T_{(min)} < T_A < T_{(max)}$	3/	All	5% typical		
High level output voltage, clock			3/	All	3.7		V
Low level output voltage, clock			3/	All		0.2	V
Ramp peak	V_{RP}		3/	All	2.6	3	V
Ramp valley	V_{RV}		3/	All	0.7	1.25	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Oscillator section - continued.							
Ramp valley-to-peak			3/	All	1.6	2	V
Oscillator discharge current	I_{OSC}	R_T = open, V_{CT} = 2 V	3/	All	9	11	mA
Error Amplifier section							
Input offset voltage	V_{IO}		3/	All		10	mV
Input bias current	I_{IB}		3/	All		3	µA
Input offset current	I_{IO}		3/	All		1	µA
Open loop gain		1 V < V_O < 4 V	3/	All	60		dB
Common mode rejection ratio	CMRR	1.5 V < V_{CM} < 5.5 V	3/	All	75		dB
Power supply rejection ratio	PSRR	12 V < V_{CC} < 20 V	3/	All	85		dB
Output sink current	$I_{O(sink)}$	V_{EAOUT} = 1 V	3/	All	1		mA
Output source current	$I_{O(src)}$	V_{EAOUT} = 4 V	3/	All		-0.5	mA
High level output voltage	V_{OH}	I_{EAOUT} = -0.5 mA	3/	All	4.5	5	V
Low level output voltage	V_{OL}	I_{EAOUT} = -1 mA	3/	All	0	1	V
Gain bandwidth product		f = 200 kHz	3/	All	6		MHz
Slew rate 4/	SR		3/	All	6		V/µs
PWM Comparator section							
Bias current, RAMP	I_{BIAS}	V_{RAMP} = 0 V	3/	All		-8	µA
Minimum duty cycle			3/	All		0%	
Maximum duty cycle			3/	All	85%		
Leading edge blanking time	t_{LEB}	R_{LEB} = 2 kΩ, C_{LEB} = 470 pF	3/	All	300	450	ns
Leading edge blanking resistance	R_{LEB}	$V_{CL / LEB}$ = 3 V	3/	All	8.5	11.5	kΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
PWM Comparator section - continued							
Zero dc threshold, EAOUT	V_{ZDC}	V_{RAMP} = 0 V	3/	All	1.1	1.4	V
Delay to output time 4/	t_{DELAY}	V_{EAOUT} = 2.1 V, V_{ILIM} = 0 V to 2 V step	3/	All		80	ns
Current Limit/Start Sequence/Fault section							
Soft start charge current	I_{SS}	V_{SS} = 2.5 V	3/	All	8	20	µA
Full soft start threshold voltage	V_{SS}		3/	All	4.3		V
Restart discharge current	I_{DSCH}	V_{SS} = 2.5 V	3/	All	100	350	µA
Restart threshold voltage	I_{SS}		3/	All		0.5	V
ILIM bias current	I_{BIAS}	V_{ILIM} = 0 V to 2 V step	3/	All		15	µA
Current limit threshold voltage	I_{CL}		3/	All	0.95	1.05	V
Overcurrent threshold voltage			3/	All	1.14	1.26	V
Delay to output time, ILIM 4/	t_d	V_{ILIM} = 0 V to 2 V step	3/	All		80	ns
Output section							
Low level output saturation voltage		I_{OUT} = 20 mA	3/	All		0.4	V
		I_{OUT} = 200 mA				2.2	
High level output saturation voltage		I_{OUT} = 20 mA	3/	All		2.9	V
		I_{OUT} = 200 mA				3	
Rise / fall time 4/	t_r, t_f	C_L = 1 nF	3/	All		45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Undervoltage Lockout (UVLO) section							
Start threshold voltage			3/	All	8.4	9.6	V
OVLO hysteresis			3/	All	0.4	1.2	V
Supply Current section							
Startup current	I_{SU}	$V_C = V_{CC} = V_{TH(start)} = -0.5$ V	3/	All		300	μA
Input current	I_{CC}		3/	All		36	mA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{CC} = 12, $T_A = T_J$, R_T = 3.65 kΩ, and C_T = 1 nF.

3/ For device type 01, T_A = -40°C to +125°C. For device type 02, T_A = -55°C to +125°C.

4/ Ensured by design. Not production tested.

Case X

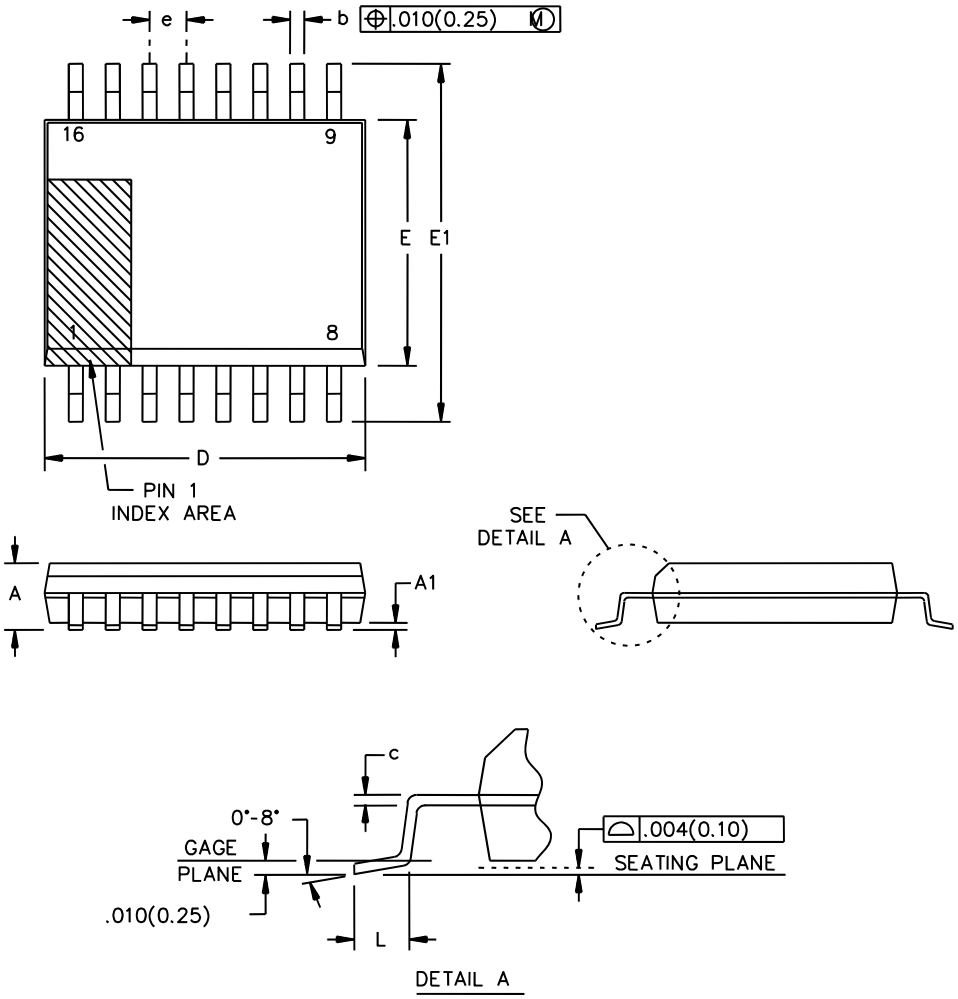

FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.104	---	2.65
A1	0.004	0.012	0.10	0.30
b	0.012	0.020	0.31	0.50
c	0.008	0.013	0.20	0.33
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
E1	0.393	0.419	9.97	10.63
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n		16		16

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inch (0.15 mm).
3. Falls within JEDEC MS-013 variation AA.

FIGURE 1. Case outline - continued.

Device types	01 and 02		
Case outlines	X		
Terminal number	Terminal symbol	I/O	Description
1	INV	I	Inverting input to the error amplifier.
2	NI	I	Non-inverting input to the error amplifier.
3	EAOUT	O	Output of the error amplifier for compensation.
4	CLK/LEB	O	Clock/leading edge blanking. Output of the internal oscillator.
5	R_T	I	Resistor timing. Timing resistor connection pin for oscillator frequency programming.
6	C_T	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
7	RAMP	I	Non-inverting input to the PWM comparator with 1.25 V internal input offset. In voltage mode operation, this serves as the input voltage feed forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
8	SS	I	Soft start input pin which also doubles as the maximum duty cycle clamp.
9	I_{LIM}	I	Input to the current limit comparator.
10	GND	---	Analog ground return pin.
11	OUTA	O	High current totem pole output A of the on-chip drive stage.
12	PGND	---	Ground return pin for the output driver stage.
13	V_C	---	Power supply pin for the output stage. This pin should be bypassed with 0.1 μF monolithic ceramic low equivalent series inductance (ESL) capacitor with minimal trace lengths.
14	OUTB	O	High current totem pole output B of the on-chip drive stage.
15	V_{CC}	---	Power supply pin for the device. This pin should be bypassed with 0.1 μF monolithic ceramic low ESL capacitor with minimal trace lengths.
16	V_{REF}	O	5.1 V reference. For stability, the reference should be bypassed with 0.1 μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

FIGURE 2. Terminal connections.

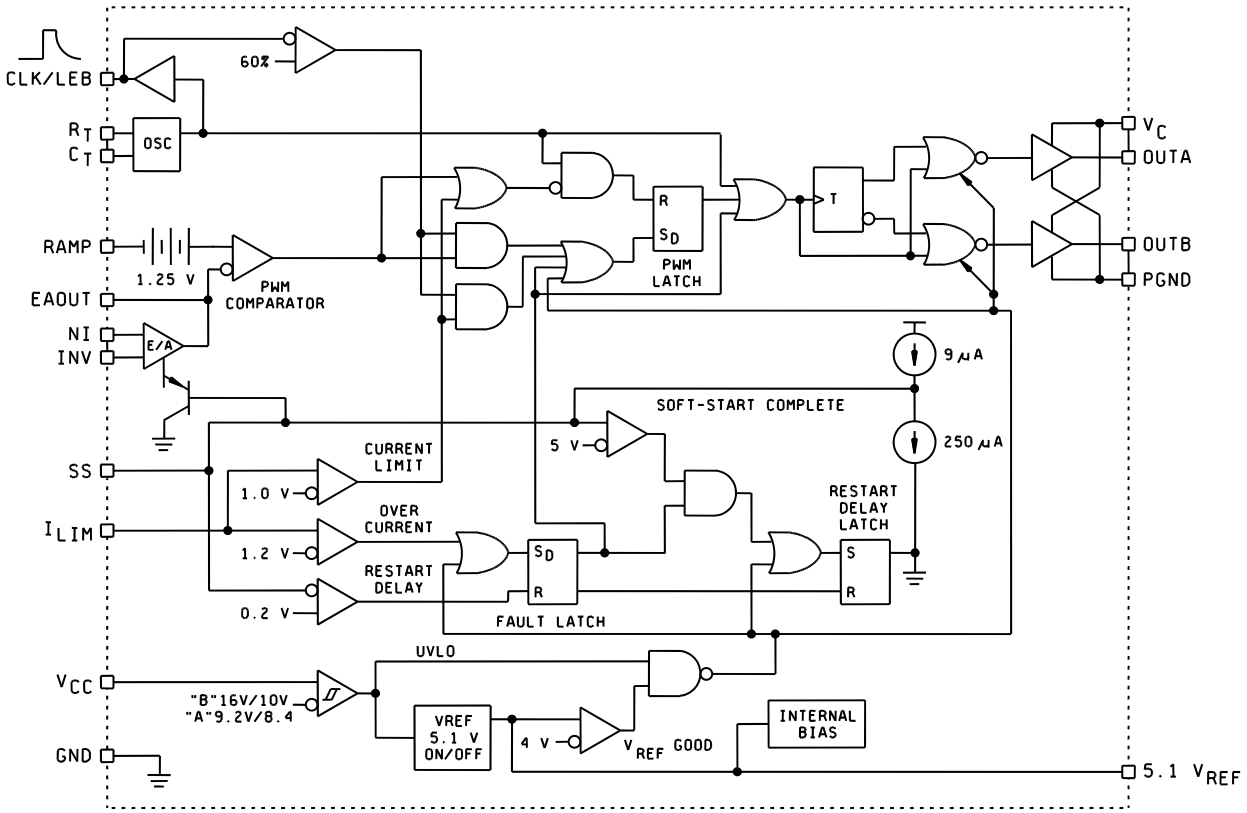

FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Top-Side Marking	Vendor part number
V62/05616-01XE	01295	UC2825AQEP	UC2825AQDWREP
V62/05616-02XE	01295	UC2825AMEP	UC2825AMDWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243