REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	12-01-19	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	21-03-19	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B	B	B					
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 05-08-30	**CHECKED BY** Charles F. Saffle **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, LINEAR, INTERCONNECT EXTENDER CHIPSET WITH LVDS, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/05615
	REV B	**PAGE** 1 **OF** 14

AMSC N/A

5962-V036-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance interconnect extender chipset with LVDS microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05615	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device types.

Device type	Generic	Circuit function
01	SN65LVDT14-EP	Interconnect extender chipset with LVDS, one driver plus four receivers
02	SN65LVDT41-EP	Interconnect extender chipset with LVDS, four drivers plus one receiver

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V to +4 V 2/
Input voltage range:	
D or R	-0.5 V to +6 V
A, B, Y, or Z	-0.5 V to +4 V
Electrostatic discharge:	
Human-body model: 3/	
A, B, Y, Z, and GND	±12 kV
All pins	±8 kV
Charged-device model: 4/	
All pins	±500 V
Continuous power dissipation:	
T_A < 25°C power rating	774 mW
T_A = 85°C power rating	402 mW
T_A = 125°C power rating	154 mW
Operating factor above T_A = 25°C	6.2 mW/°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
3/ Tested in accordance with JEDEC Standard 22, Test Method A114 (JESD 22-A114).
4/ Tested in accordance with JEDEC Standard 22, Test Method C101 (JESD 22-C101).

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +3 V to +3.6 V
Minimum high-level input voltage (V_{IH})..... +2 V
Maximum low-level input voltage (V_{IL}) ..... +0.8 V
Magnitude of differential input voltage ($|V_{ID}|$)..... +0.1 V to +0.6 V
Common-mode input voltage (V_{IC}): 5/
Minimum V_{IC} ..... $|V_{ID}|/2$
Maximum V_{IC} (V_{CC} = 3.0 V to 3.15 V)..... V_{CC} – 0.8 V
Maximum V_{IC} (V_{CC} > 3.15 V)..... 2.4 - $|V_{ID}|/2$
Operating free-air temperature range (T_A)..... -40°C to +125°C

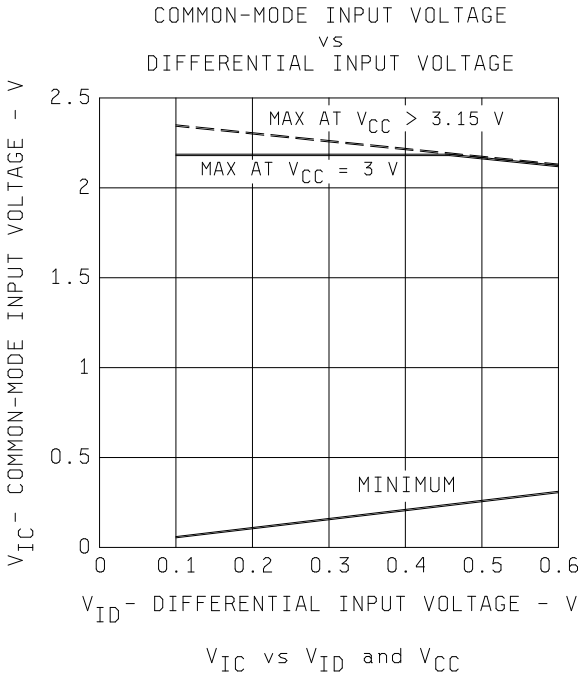


FIGURE 1. V_{IC} vs V_{ID} and V_{CC}.

5/ See figure 1. The minimum V_{IC} relation with V_{ID} is the linear relation $|V_{ID}|/2$ shown at the bottom of figure 1. For maximum V_{IC} values, the relation with V_{ID} depends on the operating V_{CC} condition shown at the top of figure 1.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD 22-A114	-	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
JESD 22-C101	-	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 2.

3.5.2 Logic diagram and function tables. The logic diagram and function tables shall be as shown in figure 3.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.4 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as shown in figures 5a – 5f.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified	Device type	Limits			Unit
				Min	Typ	Max	
Receiver Electrical Characteristics 2/							
Positive-going differential input voltage threshold	V_{ITH+}	See figure 5a.	All			100	mV
Negative-going differential input voltage threshold	V_{ITH-}			-100			mV
High-level output voltage	V_{OH}	I_{OH} = -8 mA		2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 8 mA				0.4	V
Input current (A or B inputs)	I_I	V_I = 0 V and V_I = 2.4 V, Other input open.				±40	µA
Power-off input current (A or B inputs)	$I_{I(OFF)}$	V_{CC} = 0 V, V_I = 2.4 V				±40	µA
Input capacitance, A or B input to GND	C_i	V_I = A sin 2πft + CV			5		pF
Termination impedance	Z_t	V_{ID} = 0.4 sin 2.5E09 t V		88		132	Ω
Driver Electrical Characteristics 2/							
Differential output voltage magnitude	$\|V_{OD}\|$	RL = 100 Ω See figures 5b and 5d.	All	247	340	454	mV
Change in differential output voltage magnitude between logic states	$\Delta\|V_{OD}\|$			-50		50	mV
Steady-state common-mode output voltage	$V_{OC(SS)}$	See figure 5e.		1.125		1.375	V
Change in steady-state common-mode output voltage between logic states	$\Delta V_{OC(SS)}$			-50		50	mV
Peak-to-peak common-mode output voltage	$V_{OC(PP)}$				50		mV
High-level input current	I_{IH}	V_{IH} = 2 V				20	µA
Low-level input current	I_{IL}	V_{IL} = 0.8 V				10	µA
Short-circuit output current	I_{OS}	V_{OY} or V_{OZ} = 0 V				±24	mA
		V_{OD} = 0 V 3/				±12	
Power-off output current	$I_{O(OFF)}$	V_{CC} = 1.5 V, V_O = 2.4 V				±1	µA
Device Electrical Characteristics 2/							
Supply current	I_{CC}	Driver R_L = 100 Ω, Driver V_I = 0.8 V or 2 V, Receiver V_I = ±0.4 V	01			25	mA
			02			35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	Device type	Limits			Unit
				Min	Typ	Max	
Receiver Switching Characteristics 2/							
Propagation delay time, low- to high-level output	t_{PLH}	C_L = 10 pF See figure 5c.	All	1	2.6	4.8	ns
Propagation delay time, high- to low-level output	t_{PHL}			1	2.6	4.8	ns
Output signal rise time	t_r			0.15		1.4	ns
Output signal fall time	t_f			0.15		1.4	ns
Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	$t_{sk(p)}$				150	750	ps
Output skew	$t_{sk(o)}$ 4/				100	550	ps
Part-to-part skew	$t_{sk(pp)}$ 5/					1	ns
Driver Switching Characteristics 2/							
Propagation delay time, low- to high-level output	t_{PLH}	R_L = 100 Ω, C_L = 10 pF See figure 5f.	All				ns
Propagation delay time, high- to low-level output	t_{PHL}						ns
Differential output signal rise time	t_r						ns
Differential output signal fall time	t_f						ns
Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	$t_{sk(p)}$						ps
Output skew	$t_{sk(o)}$ 6/						ps
Part-to-part skew	$t_{sk(pp)}$ 5/						ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All typical (Typ) values are at T_A = 25°C and with a 3.3-V supply. All minimum (Min) values and maximum (Max) values are over the recommended operating full temperature range of -40°C to +125°C, unless otherwise specified.

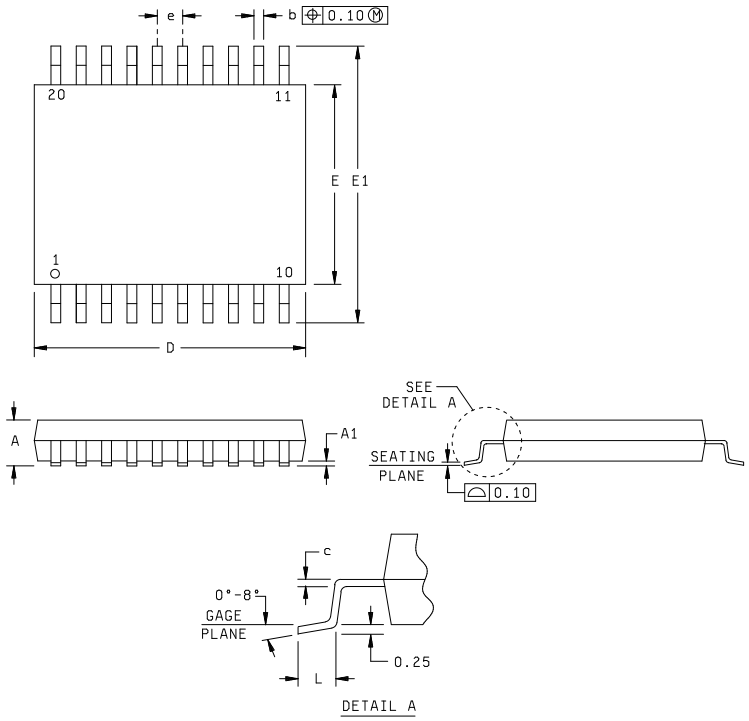
3/ This parameter is guaranteed by design (GBD) over industrial temperature range.

4/ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all the receivers of a single device with all of their inputs connected together.

5/ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6/ $t_{sk(o)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

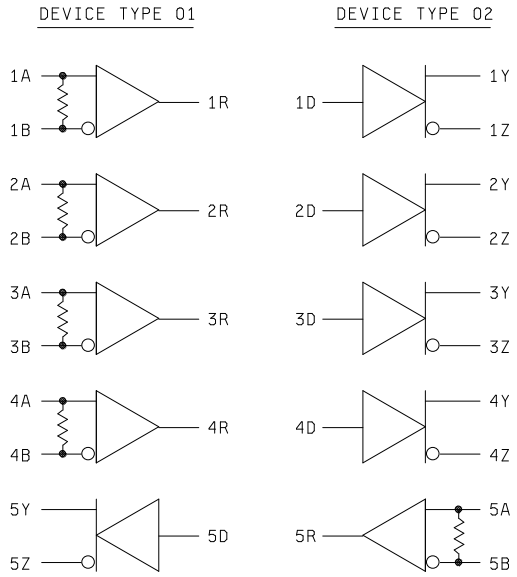
Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 BSC		0.026 BSC	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	6.40	6.60	0.252	0.260					

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 (0.006).
4. Falls within JEDEC MO-153.

FIGURE 2. Case outlines.



Function tables.

Receiver

Device types: 01 and 02	
Inputs	Output
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV < $V_{ID} \leq$ 100 mV	?
$V_{ID} \leq$ -100 Mv	L
Open	H

H = high level, L = low level, ? = indeterminate

Driver

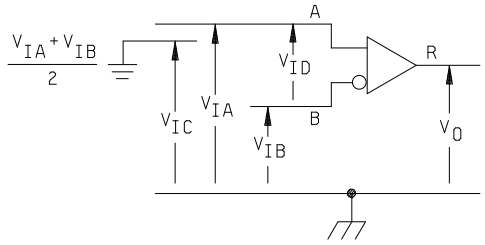
Device types: 01 and 02		
Input	Outputs	
D	Y	Z
H	H	L
L	L	H
Open	L	H

H = high level, L = low level

FIGURE 3. Logic diagram and function tables.

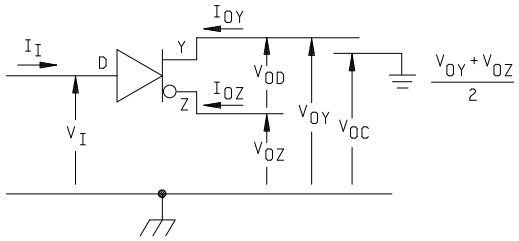
Device type:	01			02			
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A	11	GND	1	1D	11	5B
2	1B	12	5D	2	GND	12	5A
3	2A	13	V_{CC}	3	2D	13	4Z
4	2B	14	4R	4	V_{CC}	14	4Y
5	3A	15	GND	5	3D	15	3Z
6	3B	16	3R	6	GND	16	3Y
7	4A	17	V_{CC}	7	4D	17	2Z
8	4B	18	2R	8	V_{CC}	18	2Y
9	5Y	19	GND	9	5R	19	1Z
10	5Z	20	1R	10	GND	20	1Y

FIGURE 4. Terminal connections.



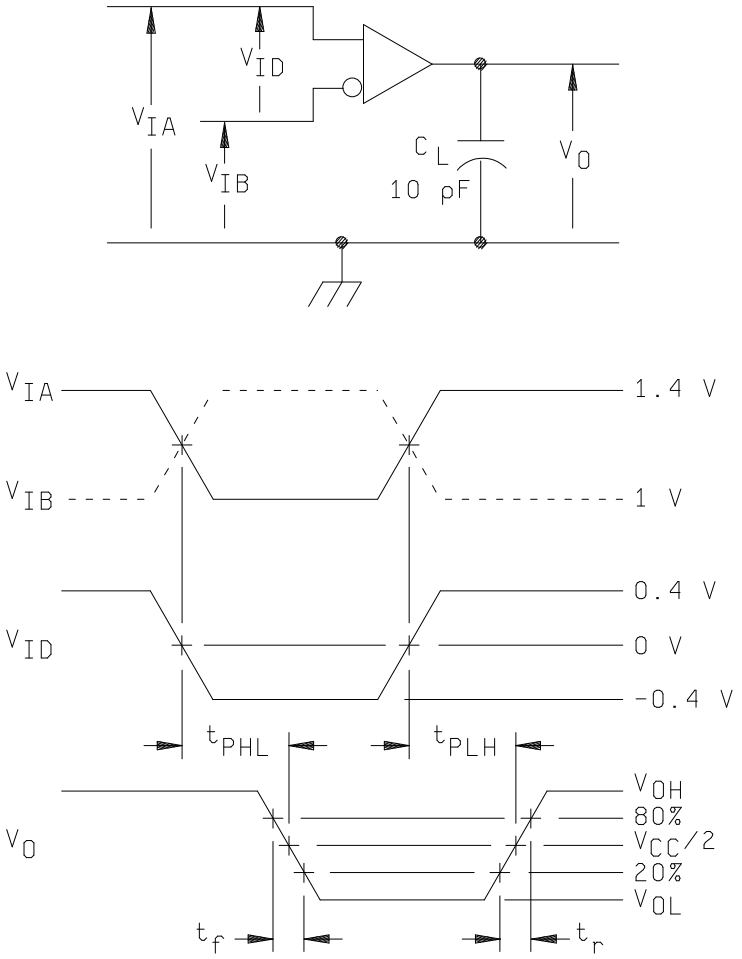
RECEIVER VOLTAGE DEFINITIONS

FIGURE 5a. Switching waveforms and test circuits.



DRIVER VOLTAGE AND CURRENT DEFINITIONS

FIGURE 5b. Switching waveforms and test circuits.



RECEIVER TIMING TEST CIRCUITS AND WAVEFORMS

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 $\pm$0.05 μs. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

FIGURE 5c. Switching waveforms and test circuits.

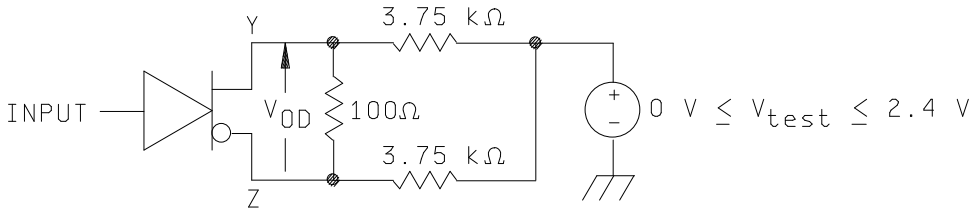
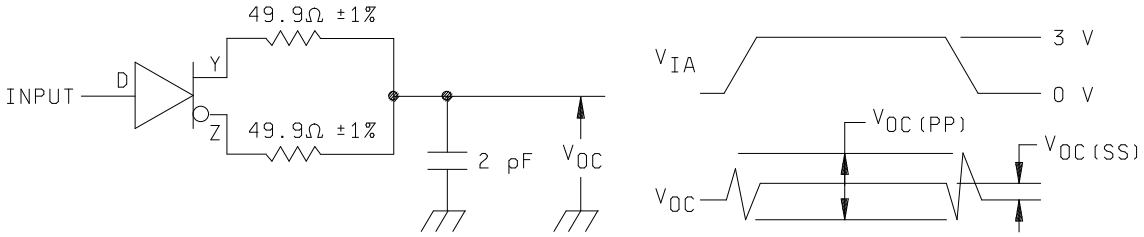


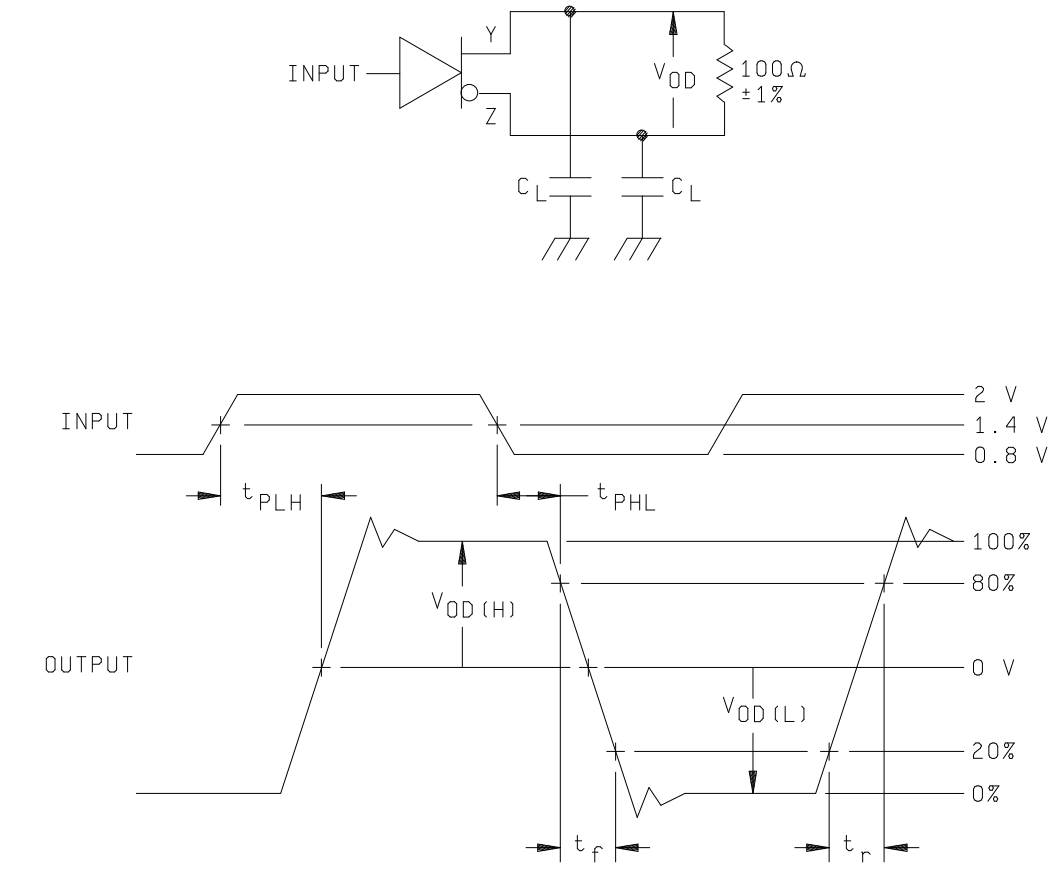
FIGURE 5d. Switching waveforms and test circuits.



TEST CIRCUIT AND DEFINITIONS FOR DRIVER COMMON-MODE OUTPUT VOLTAGE

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 μs. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

FIGURE 5e. Switching waveforms and test circuits.



TEST CIRCUIT,TIMING AND VOLTAGE DEFINITIONS OF DIFFERENTIAL OUTPUT SIGNAL

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ±0.05 μs. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

FIGURE 5f. Switching waveforms and test circuits.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/05615-01XE	01295	SN65LVDT14QPWREP	LVDT14EP
V62/05615-02XE	01295	SN65LVDT41QPWREP	LVDT41EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not available from an approved source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243