REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02 information. Update boilerplate. - CFS	07-05-08	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	13-11-18	Thomas M. Hess
C	Make change to the dimension c minimum limit as specified under Figure 1. Update document paragraphs to current requirements. - ro	20-08-06	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**		C	C	C	C	C	C	C	C	C	C	C	C	C	C					
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 05-10-19	**CHECKED BY** Charles F. Saffle	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, HIGH-SPEED DIFFERENTIAL RECEIVER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/05614**
	REV C	**PAGE** 1 **OF** 14

AMSC N/A

5962-V060-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high-speed differential receiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05614	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65LVDS33-EP	High-speed differential receiver
02	SN65LVDT33-EP	High-speed differential receiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MS-012-AC	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.5 V to +4 V
Voltage range:
  Enables or Y ..... -1 V to +6 V
  A or B ..... -5 V to +6 V
  |VA – VB| (Device 02 only) ..... 1 V
Electrostatic discharge:
  A, B, and GND ..... Class 3, A: 15 kV, B: 500 V 3/
Charged-device mode:
  All pins ..... ±500 V 4/
Continuous power dissipation:
  $T_A \leq 25°C$ power rating ..... 950 mW
  $T_A = 85°C$ power rating ..... 494 mW
  $T_A = 125°C$ power rating ..... 189 mW
  Operating factor above $T_A = 25°C$ ..... 7.6 mW/°C 5/
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... +260°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +3 V to +3.6 V
High-level input voltage (Enables) (V_{IH}) ..... +2 V to +5 V
Low-level input voltage (Enables) (V_{IL}) ..... 0 V to +0.8 V
Magnitude of differential input voltage ($|V_{ID}|$):
  Device type 01 ..... +0.1 V to +3 V
  Device type 02 ..... 0.8 V maximum
Voltage at any bus terminal (separately or common-mode) (V_I or V_{IC}) ..... -4 V to +5 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

_____

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
3/ Tested in accordance with JEDEC Standard 22, Test Method A114 (JESD 22-A114).
4/ Tested in accordance with JEDEC Standard 22, Test Method C101 (JESD 22-C101).
5/ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JESD 22-A114	–	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
JESD 22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Logic diagram and function table. The logic diagram and function table shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as shown in figures 4a, 4b, 4c, 4d, 4e, and 4f.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified	Device type	Limits			Unit
				Min	Typ	Max	
Electrical characteristics 2/							
Positive-going differential input voltage threshold	V_{IT1}	VIB = -4 V or 5 V See figures 4a and 4b.	All			50	mV
Negative-going differential input voltage threshold	V_{IT2}		All	-50			mV
Differential input failsafe voltage threshold	V_{IT3}	See figures 4a and 4e.	All	-32		-100	mW
Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$	$V_{ID(HYS)}$		All		50		mV
High-level output voltage	V_{OH}	I_{OH} = -4 mA	All	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 4 mA	All			0.4	V
Supply current	I_{CC}	G at V_{CC}, No load, Steady state	All		16	25	mA
		G at GND			1.1	6	
Input current (A or B inputs)	I_I	V_I = 0 V, Other input open.	01			±25	µA
		V_I = 2.4 V, Other input open.				±25	
		V_I = -4 V, Other input open.				±80	
		V_I = 5 V, Other input open.				±45	
		V_I = 0 V, Other input open.	02			±50	
		V_I = 2.4 V, Other input open.				±50	
		V_I = -4 V, Other input open.				±180	
		V_I = 5 V, Other input open.				±95	
Differential input current ($I_{IA} – I_{IB}$)	I_{IO}	V_{ID} = 100 mV, V_{IC} = -4 V or 5 V	01			±5	µA
		V_{ID} = 200 mV, V_{IC} = -4 V or 5 V	02	1.55		2.4	mA
Power-off input current (A or B inputs)	$I_{I(OFF)}$	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V	01			±25	µA
		V_A or V_B = -4 V or 5 V, V_{CC} = 0 V				±60	
		V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V	02			±35	
		V_A or V_B = -4 V or 5 V, V_{CC} = 0 V				±120	
High-level input current (Enables)	I_{IH}	V_{IH} = 2 V	All			12	µA
Low-level input current (Enables)	I_{IL}	V_{IL} = 0.8 V	All			12	µA
High-impedance output current	I_{OZ}		All	-10		12	µA
Input capacitance, A or B input to GND	C_I	V_I = 0.4 sin (4E6πt) + 0.5 V	All		5		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	Device type	Limits			Unit
				Min	Typ	Max	
Switching characteristics 2/							
Propagation delay time, low-to-high level output	$t_{PLH(1)}$	See figures 4a and 4c.	All	1.8	4	8	ns
Propagation delay time, high-to-low level output	$t_{PHL(1)}$		All	1.8	4	8	ns
Delay time, failsafe deactivate time	t_{d1}	C_L = 10 pF See figures 4a, 4c, and 4f.	All			11	ns
Delay time, failsafe activate time	t_{d2}		All	0.2		2	µs
Pulse skew ($\lvert t_{PHL(1)} - t_{PLH(1)} \rvert$)	$t_{sk(p)}$	See figures 4a and 4c.	All		200		ps
Output skew	$t_{sk(o)}$ 3/		All		150		ps
Part-to-part skew	$t_{sk(pp)}$ 4/		All			1.2	ns
Output signal rise time	t_r		All		0.8		ns
Output signal fall time	t_f		All		0.8		ns
Propagation delay time, high level-to-high impedance output	t_{PHZ}	See figure 4d.	All		5.5	12	ns
Propagation delay time, low level-to-high impedance output	t_{PLZ}		All		4.4	12	ns
Propagation delay time, high impedance-to-high level output	t_{PZH}		All		3.8	12	ns
Propagation delay time, high impedance-to-low level output	t_{PZL}		All		7	12	ns

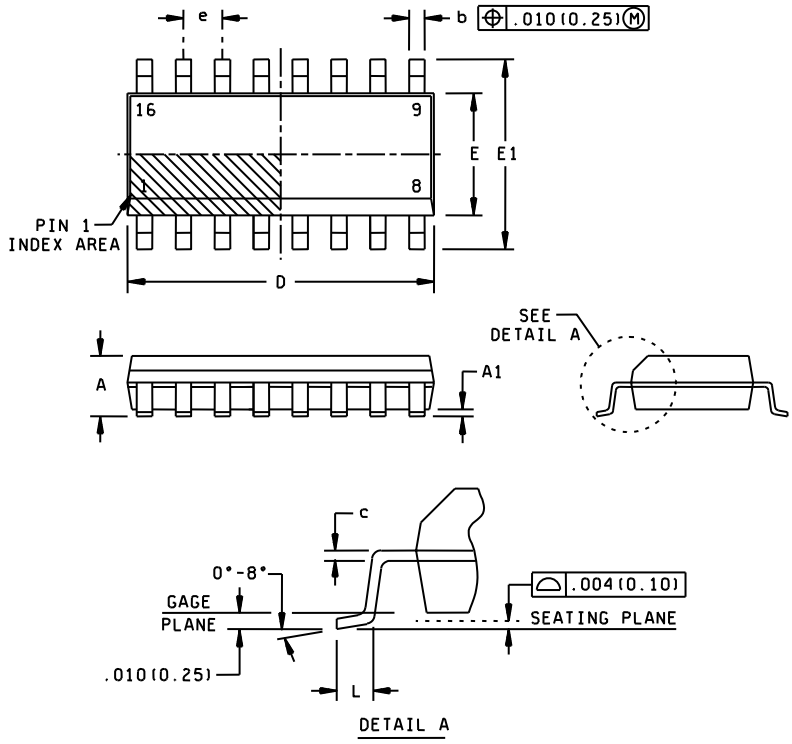
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All typical (Typ) values are at T_A = 25°C and with a 3.3-V supply. All minimum (Min) values and maximum (Max) values are over the recommended operating full temperature range of -55°C to +125°C, unless otherwise specified.

3/ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven together.

4/ $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.069	---	1.75	E	0.150	0.157	3.80	4.00
A1	0.004	0.010	0.10	0.25	E1	0.228	0.244	5.80	6.20
b	0.012	0.020	0.31	0.51	e	0.050 BSC		1.27 BSC	
c	0.005	0.010	0.13	0.25	L	0.016	0.050	0.40	1.27
D	0.386	0.394	9.80	10.00					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. For dimension D, body length does not include mold, flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inch (0.15 mm).
4. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) each side.
5. Falls within JEDEC MS-012 variation AC.

FIGURE 1. Case outline.

Function table.

Device types: 01 and 02			
Differential Input	Enables		Output
$V_{ID} = V_A - V_B$	G	$\overline{G}$	Y
$V_{ID} \geq$ -32 mV	H	X	H
	X	L	H
-100 mV $<$ $V_{ID} \leq$ -32 mV	H	X	?
	X	L	?
$V_{ID} \leq$ -100 mV	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

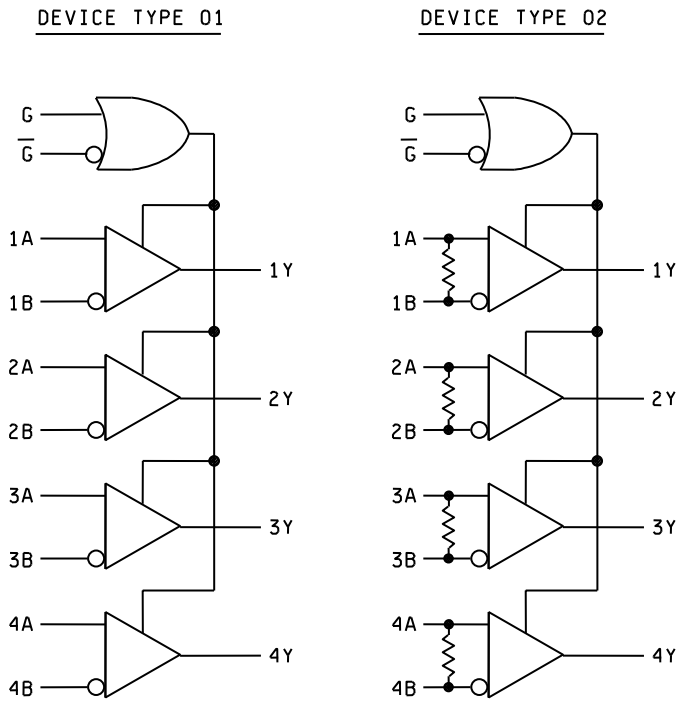
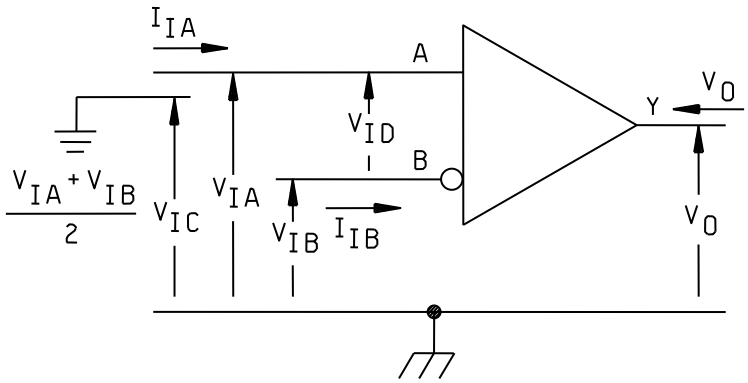


FIGURE 2. Logic diagram and function table.

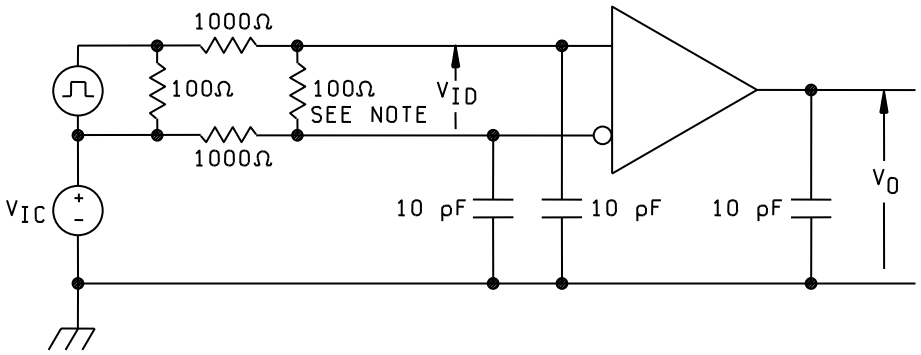
Device types:	01 and 02		
Case outline:	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1B	9	3B
2	1A	10	3A
3	1Y	11	3Y
4	G	12	$\overline{G}$
5	2Y	13	4Y
6	2A	14	4A
7	2B	15	4B
8	GND	16	V_{CC}

FIGURE 3. Terminal connections.

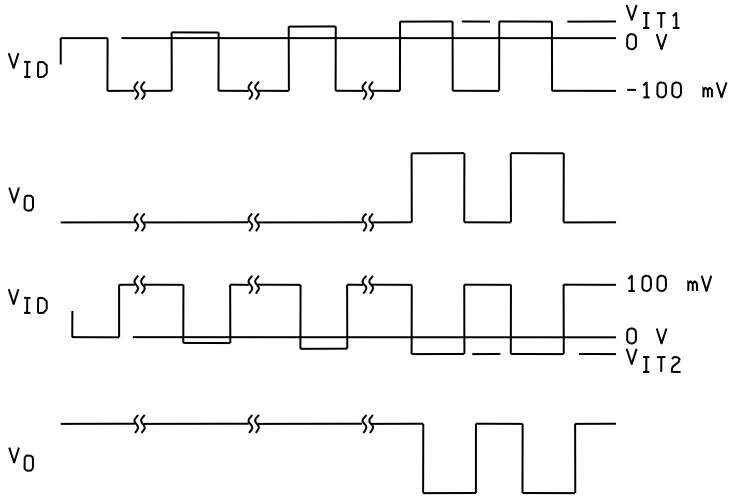


VOLTAGE AND CURRENT DEFINITIONS

FIGURE 4a. Switching waveforms and test circuits.



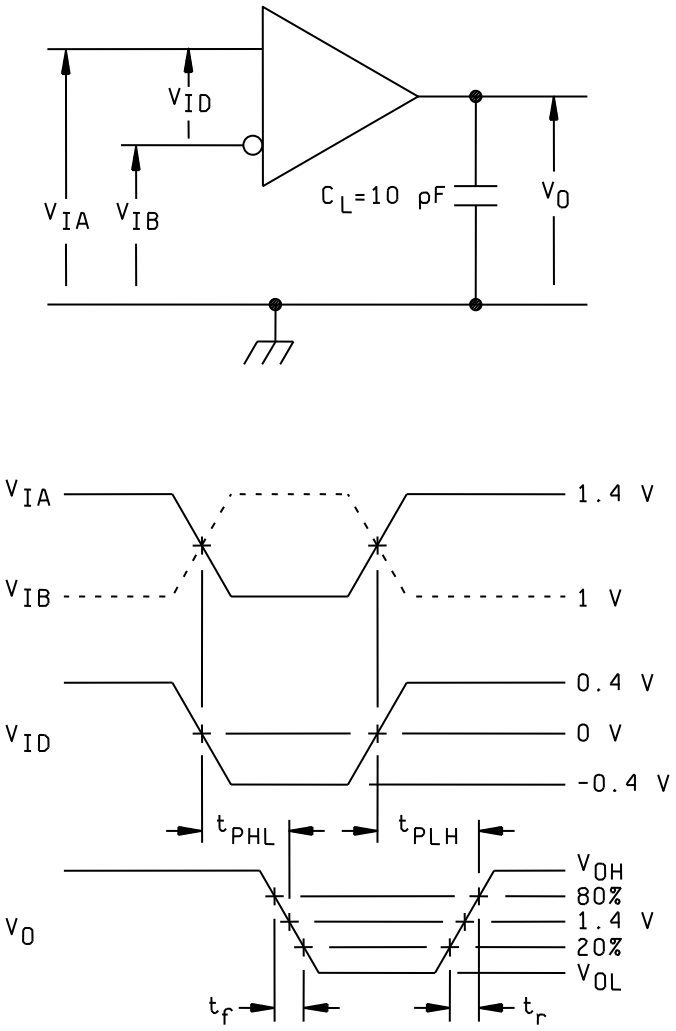
NOTE: REMOVE FOR TESTING LVDT DEVICE



NOTE: INPUT SIGNAL OF 3 Mpps, DURATION OF 167 ns, AND TRANSITION TIME OF < 1 ns

V_{IT1} AND V_{IT2} INPUT VOLTAGE THRESHOLD TEST CIRCUIT AND DEFINITIONS

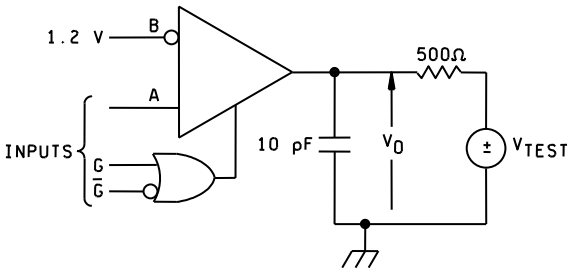
FIGURE 4b. Switching waveforms and test circuits.



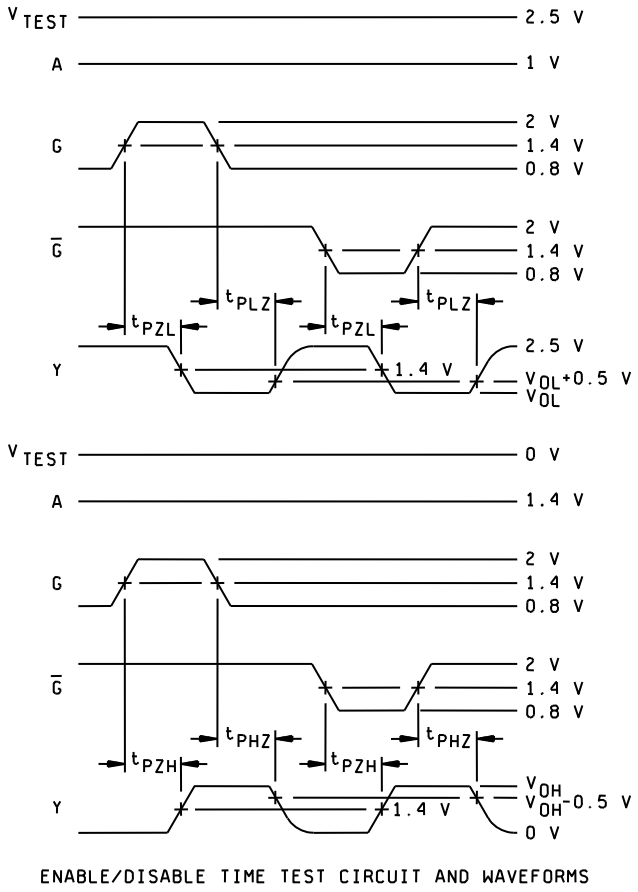
TIMING TEST CIRCUIT AND WAVEFORMS

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ±0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test (DUT).

FIGURE 4c. Switching waveforms and test circuits.



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.



ENABLE/DISABLE TIME TEST CIRCUIT AND WAVEFORMS

FIGURE 4d. Switching waveforms and test circuits.

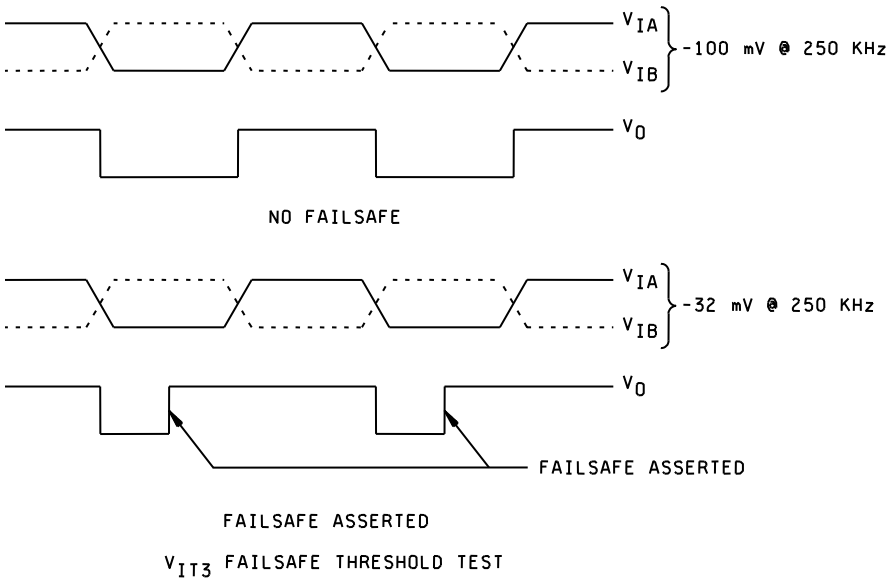


FIGURE 4e. Switching waveforms and test circuits.

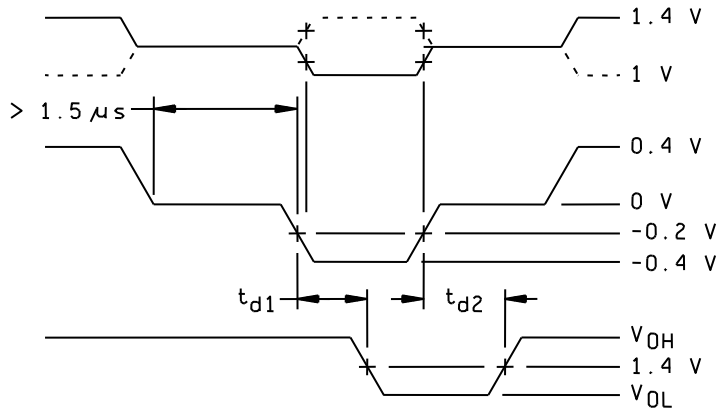


FIGURE 4f. Switching waveforms and test circuits.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/05614-01XE	01295	LVDS33M	SN65LVDS33MDREP
V62/05614-02XE	2/	LVDT33M	SN65LVDT33MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not available from an approved source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243