REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device type 02. Update boilerplate to current revision. - CFS	06-12-15	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	12-02-14	Thomas M. Hess
C	Update boilerplate paragraphs to current requirements. - PHN	21-03-19	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV																						
PAGE																						
REV STATUS OF PAGES	**REV**		C	C	C	C	C	C	C	C	C	C	C	C	C	C						
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14						

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 05-08-15	**CHECKED BY** Charles F. Saffle **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, CMOS, 14-BIT, 125 MSPS ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/05613**
	REV C	**PAGE** 1 **OF** 14

AMSC N/A

5962-V035-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 14-bit, 125 MSPS Analog-to-Digital Converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05613	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device types.

Device type	Generic	Circuit function
01	ADS5500-EP	14-bit, 125 MSPS Analog-to-Digital Converter
02	ADS5500-EP	14-bit, 125 MSPS Analog-to-Digital Converter

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	64	JEDEC MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range:
- AV_{DD} to A_{GND} ..... -0.3 V to +3.7 V
- DRV_{DD} to DR_{GND} ..... -0.3 V to +3.7 V

Supply voltage range:
- A_{GND} to DR_{GND} ..... -0.1 V to +0.1 V

Analog input to A_{GND} ..... -0.15 V to +2.5 V
Logic input to DR_{GND} ..... -0.3 V to DR_{VDD} + 0.3 V
Digital data output to DR_{GND} ..... -0.3 V to DR_{VDD} + 0.3 V
Input current (any input) ..... 30 mA
Operating temperature range ..... -55°C to +125°C
Junction temperature ..... +142°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

Package Thermal Characteristics:
Thermal resistance, junction to ambient (R_{TJA}): 3/ 4/
- Same package form without bond pad ..... 75.83°C/W
- Bond pad not connected to PCB Thermal plane ..... 42.2°C/W
- Bond pad connected to PCB thermal plane ..... 21.47°C/W

Thermal resistance, junction to case (R_{TJC}): 3/ 4/
- Same package form without bond pad ..... 7.8°C/W
- Bond pad not connected to PCB Thermal plane ..... 0.38°C/W
- Bond pad connected to PCB thermal plane ..... 0.38°C/W

1.4 Recommended operating conditions.

Supplies:
Supply voltage range:
- Analog supply voltage (AV_{DD}) ..... +3.0 V to +3.6 V
- Output driver supply voltage (DRV_{DD}) ..... +3.0 V to +3.6 V

Analog Input:
Differential input range (typical) ..... 2.3 V_{PP}
Input common-mode voltage (V_{CM}) ..... +1.5 V to +1.6 V 5/
Digital output:
Maximum output load (typical) ..... 10 pF
Clock Input:
ADCLK input sample rate (sine wave) ($1/t_C$):
- DLL On ..... 60 MSPS to 125 MSPS
- DLL Off ..... 10 MSPS to 80 MSPS

Clock amplitude, sine wave, differential (typical) ..... 3 V_{PP}
Clock duty cycle (typical) 50%
Open free-air temperature range ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Over operating free-air temperature range unless otherwise specified.
3/ Specified with the bond pad on the backside of the package soldered to a 2-oz Cu plate PCB thermal plane.
4/ Airflow is at 0 LFM (no airflow).
5/ Input common-mode should be connected to CM.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figures 4a – 4b.

3.5.5 Terminal functions. The terminal functions shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified		Device type	Limits			Unit
					Min	Typ	Max	
ELECTRICAL CHARATERISTICS 2/								
Resolution				All		14 Tested		Bits
Analog inputs								
Differential input range				All		2.3		V_{PP}
Differential input impedance						6.6		kΩ
Differential input capacitance						4		pF
Total analog input common-mode current						4 3/		mA
Analog input bandwidth		Source impedance = 50 Ω				750		MHz
Conversion Characteristics								
Maximum sample rate				All	4/		125	MSPS
Data latency		See figure 4a.				16.5		Clock cycles
Internal Reference Voltages								
Reference bottom voltage	V_{REFM}			All		0.97		V
Reference top voltage	V_{REFP}					2.11		V
Reference error		25°C			-4		+4	%
		-55°C to +125°C			-5		+5	
Common-mode voltage output	V_{CM}					1.55 ±0.05		V
Dynamic DC Characteristics and Accuracy								
No missing codes				All	Tested			
Differential linearity error	DNL	f_{IN} = 10 MHz			-0.9	±0.75	+1.1	LSB
Integral linearity error	INL	f_{IN} = 10 MHz	25°C		-5		+5	LSB
			-55°C to +125°C		-8		+8	
Offset error						±1.5		mV
Offset temperature coefficient						0.0007		%/°C
Gain error						±0.45		%FS
Gain temperature coefficient						0.01		Δ%/°C
Dynamic AC Characteristics								
Signal-to-noise ratio	SNR	f_{IN} = 10 MHz	25°C	All	70.5	71.5		dBFS
			-55°C to +125°C		68	71.5		
		f_{IN} = 30 MHz				71.5		
		f_{IN} = 55 MHz				71.5		
		f_{IN} = 70 MHz	25°C		70	71.2		
			-55°C to +125°C		66.5	71		
		f_{IN} = 100 MHz				70.5		
		f_{IN} = 150 MHz				70.1		
		f_{IN} = 225 MHz				69.1		
RMS output noise		Input tied to common-mode				1.1		LSB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified		Device type	Limits			Unit
					Min	Typ	Max	
ELECTRICAL CHARATERISTICS - Continued. 2/								
Dynamic AC Characteristics - Continued.								
Spurious-free dynamic range	SFDR	f_{IN} = 10 MHz	25°C	All	82	84		dBc
			-55°C to +125°C		76	84		
		f_{IN} = 30 MHz				84		
		f_{IN} = 55 MHz				79		
		f_{IN} = 70 MHz	25°C		80	83		
			-55°C to +125°C		75	82		
		f_{IN} = 100 MHz				82		
		f_{IN} = 150 MHz				78		
		f_{IN} = 225 MHz				74		
Second-harmonic	HD2	f_{IN} = 10 MHz	25°C		82	91		dBc
			-55°C to +125°C		77	86		
		f_{IN} = 30 MHz				86		
		f_{IN} = 55 MHz				84		
		f_{IN} = 70 MHz	25°C		80	87		
			-55°C to +125°C		75	83		
		f_{IN} = 100 MHz				84		
		f_{IN} = 150 MHz				78		
		f_{IN} = 225 MHz				74		
Third-harmonic	HD3	f_{IN} = 10 MHz	25°C		82	89		dBc
			-55°C to +125°C		77	88		
		f_{IN} = 30 MHz				90		
		f_{IN} = 55 MHz				79		
		f_{IN} = 70 MHz	25°C		80	85		
			-55°C to +125°C		75	82		
		f_{IN} = 100 MHz				82		
		f_{IN} = 150 MHz				80		
		f_{IN} = 225 MHz				76		
Worst-harmonic/spur (other than HD2 and HD3)		f_{IN} = 10 MHz	25°C			88		dBc
		f_{IN} = 70 MHz	25°C			86		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified		Device type	Limits			Unit
					Min	Typ	Max	
ELECTRICAL CHARATERISTICS - Continued. 2/								
Dynamic AC Characteristics - Continued.								
Signal-to-noise + distortion	SINAD	f_{IN} = 10 MHz	25°C	All	69	70		dBc
			-55°C to +125°C		66.5	70		
		f_{IN} = 30 MHz				70		
		f_{IN} = 55 MHz				69.5		
		f_{IN} = 70 MHz	25°C		68.5	69		
			-55°C to +125°C		65	69.5		
		f_{IN} = 100 MHz				69		
		f_{IN} = 150 MHz				69		
		f_{IN} = 225 MHz				66.4		
Total harmonic distortion	THD	f_{IN} = 10 MHz	25°C		80	85		dBc
			-55°C to +125°C		76	83		
		f_{IN} = 30 MHz				82		
		f_{IN} = 55 MHz				77		
		f_{IN} = 70 MHz	25°C		77.5	81		
			-55°C to +125°C		74	79.5		
		f_{IN} = 100 MHz				79		
		f_{IN} = 150 MHz				75		
		f_{IN} = 225 MHz				71.8		
Effective number of bits	ENOB	f_{IN} = 70 MHz				11.3		Bits
Two-tone intermodulation distortion	IMD	f = 10.1 MHz, 15.1 MHz (-7 dBFS each tone)				85		dBc
		f = 30.1 MHz, 35.1 MHz (-7 dBFS each tone)				85		
		f = 50.1 MHz, 55.1 MHz (-7 dBFS each tone)				88		
Power Supply								
Total supply current	I_{CC}	V_{IN} = full-scale, f_{IN} = 55 MHz AV_{DD} = DRV_{DD} = 3.3 V		All		236	265	mA
Analog supply current	I_{AVDD}	V_{IN} = full-scale, f_{IN} = 55 MHz AV_{DD} = DRV_{DD} = 3.3 V				175	190	mA
Output buffer supply current	I_{DRVDD}	V_{IN} = full-scale, f_{IN} = 55 MHz AV_{DD} = DRV_{DD} = 3.3 V				61	75	mA
Power dissipation		Analog only				578	627	mW
		Total power with 10 pF load on digital output to ground.				780	875	
Standby power		With clocks running				181	250	mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	Device type	Limits			Unit
				Min	Typ	Max	
DIGITAL CHARACTERISTICS 2/							
Digital Inputs							
High-level input voltage			All	2.4			V
Low-level input voltage						0.8	V
High-level input current						10	µA
Low-level input current						10	µA
Input current for RESET					-20		µA
Input capacitance					4		pF
Digital Outputs 5/							
Low-level output voltage		f_S = 125 MSPS, C_{LOAD} = 10 pF 6/	All		0.3		V
High-level output voltage		f_S = 125 MSPS, C_{LOAD} = 10 pF 6/			3		V
Output capacitance					3		pF
TIMING CHARACTERISTICS 2/							
Switching Specification							
Aperture delay	t_A	See figure 4a. Input CLK falling edge to data sampling point.	All		1		ns
Aperture jitter (uncertainty)		See figure 4a. Uncertainty in sampling instant.			300		fs
Data setup time	t_{SETUP}	See figure 4a. Data valid to 50% of CLKOUT rising edge.			2		ns
Data hold time	t_{HOLD}	See figure 4a. CLKOUT rising edge to data becoming invalid			1.7		ns
Data latency	$t_{D(Pipe)}$	See figure 4a. Input clock falling edge (on which sampling takes place) to input clock rising edge (on which the corresponding data is given out).			16.5		Clock cycles
Propagation delay	t_{PDI}	See figure 4a. Input clock rising edge to data valid.			7.5		ns
Data rise time		Data out 20% to 80%.			2.5		ns
Data fall time		Data out 20% to 80%.			2.5		ns
Output enable (OE) to output stable delay					2		ms
Serial Programming Interface Timing Characteristics 7/							
SCLK period	t_{SCLK}		All	50			ns
SCLK duty cycle	t_{WSCLK}			25%	50%	75%	
SEN to SCLK setup time	t_{SLOADS}			8			ns
SCLK to SEN hold time	t_{SLOADH}			6			ns
Data setup time	t_{DS}			8			ns
Data hold time	t_{DH}			6			ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Typical (Typ), minimum (min), and maximum (max) values at room temperature is T_A = 25°C, full temperature range is T_{MIN} = -55°C to T_{MAX} = +125°C, sampling rate = 125 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, DLL On, -1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise specified.

3/ 2 mA per input.

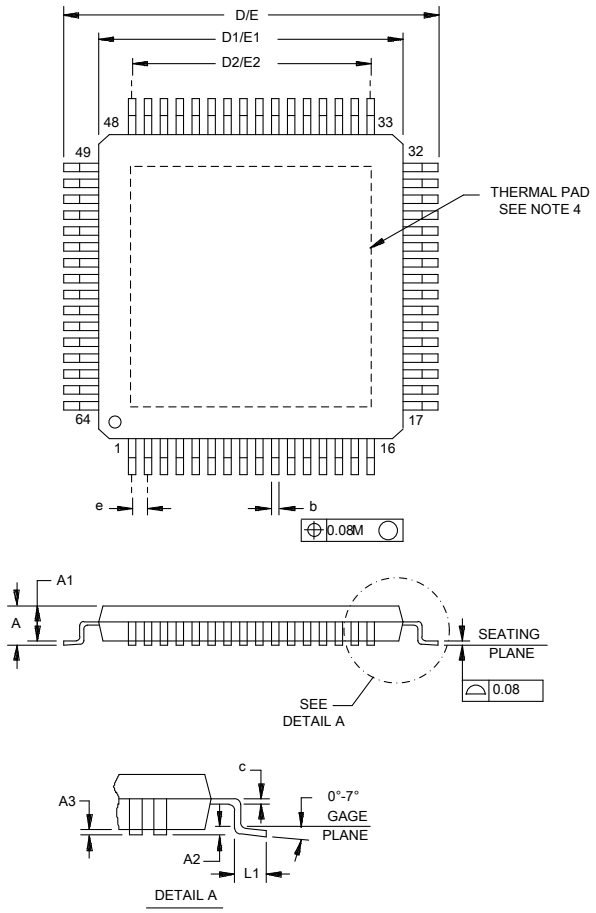
4/ See paragraph 1.4, Recommended operating conditions.

5/ For optimal performance, all digital output lines (D0: D13), including the output clock, should see a similar load.

6/ Equivalent capacitance to ground of (load + parasitics of transmission lines).

7/ Min, Typ, and Max values are characterized, but not production tested.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	D/E	11.80	12.20	0.465	0.480
A1	0.95	1.05	0.037	0.041	D1/E1	9.80	10.20	0.386	0.402
A2	0.25 NOM		0.010 NOM		D2/E2	7.50 TYP		0.295 TYP	
A3	0.05	0.15	0.002	0.006	e	0.50 BSC		0.020 BSC	
b	0.17	0.27	0.007	0.011	L1	0.45	0.75	0.018	0.030
c	0.13 NOM		0.005 NOM						

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion.
4. This package is designed to be soldered to a thermal pad on the board.
5. Falls within JEDEC MS-026.

FIGURE 1. Case outlines.

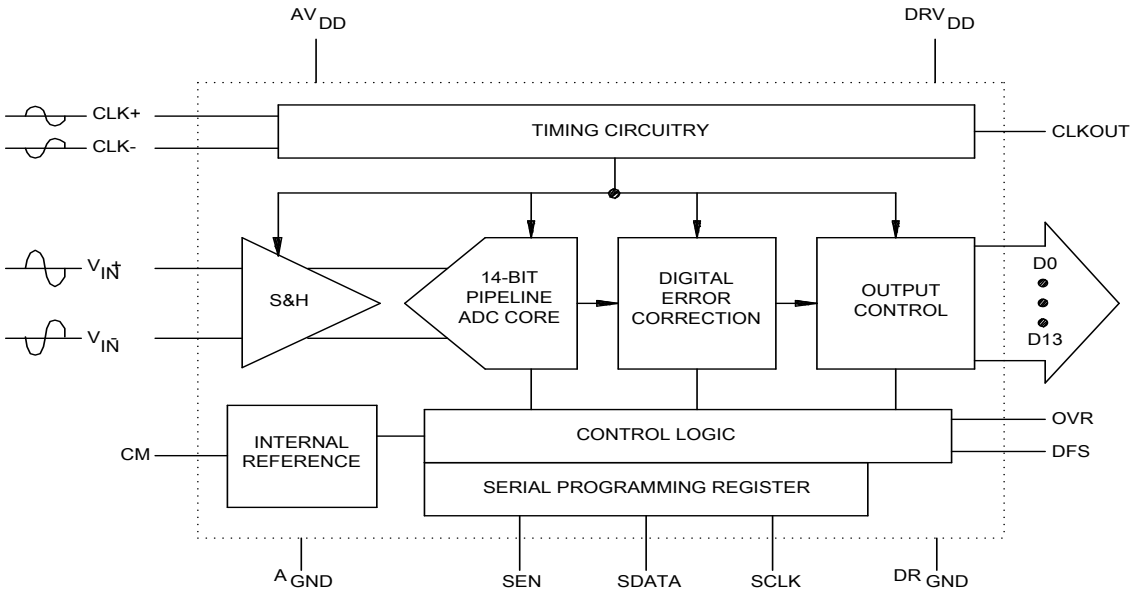
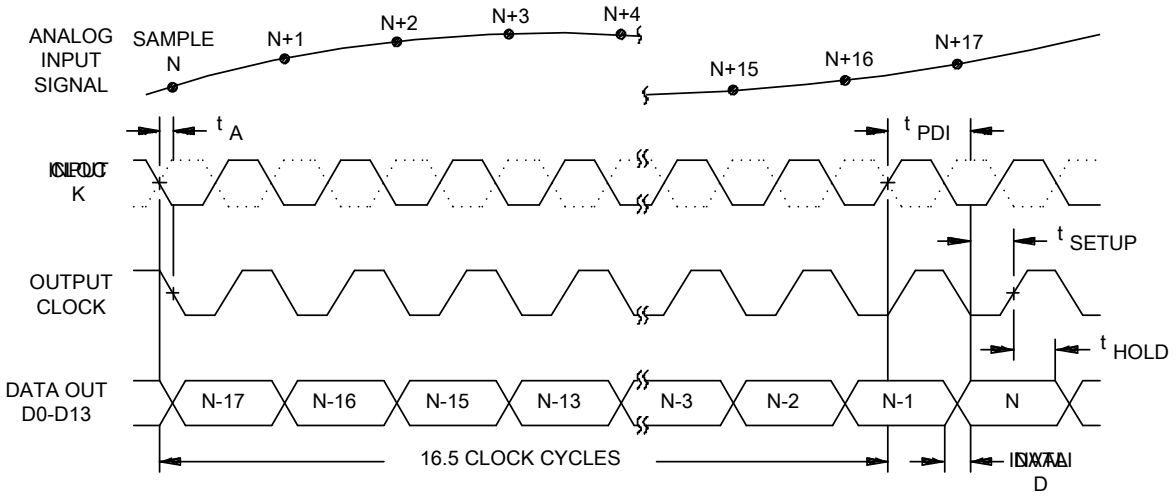


FIGURE 2. Block diagram.

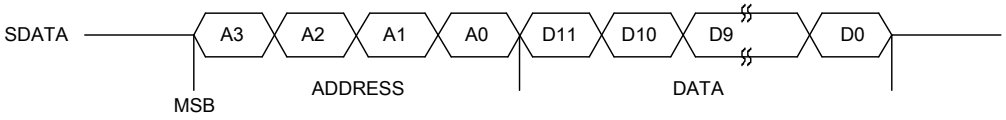
Device type:	All						
Case outline:	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DR_{GND}	17	CM	33	AV_{DD}	49	DRV_{DD}
2	SCLK	18	A_{GND}	34	AV_{DD}	50	DR_{GND}
3	SDATA	19	INP	35	RESET	51	D4
4	SEN	20	INM	36	A_{GND}	52	D5
5	AV_{DD}	21	A_{GND}	37	AV_{DD}	53	D6
6	A_{GND}	22	AV_{DD}	38	A_{GND}	54	D7
7	AV_{DD}	23	A_{GND}	39	AV_{DD}	55	D8
8	A_{GND}	24	AV_{DD}	40	DFS	56	D9
9	AV_{DD}	25	A_{GND}	41	OE	57	DR_{GND}
10	CLKP	26	AV_{DD}	42	DR_{GND}	58	DRV_{DD}
11	CLKM	27	A_{GND}	43	CLKOUT	59	DR_{GND}
12	A_{GND}	28	AV_{DD}	44	D0 (LSB)	60	D10
13	A_{GND}	29	REFP	45	D1	61	D11
14	A_{GND}	30	REFM	46	D2	62	D12
15	AV_{DD}	31	IREF	47	D3	63	D13 (MSB)
16	A_{GND}	32	A_{GND}	48	DR_{GND}	64	OVR

FIGURE 3. Terminal connections.

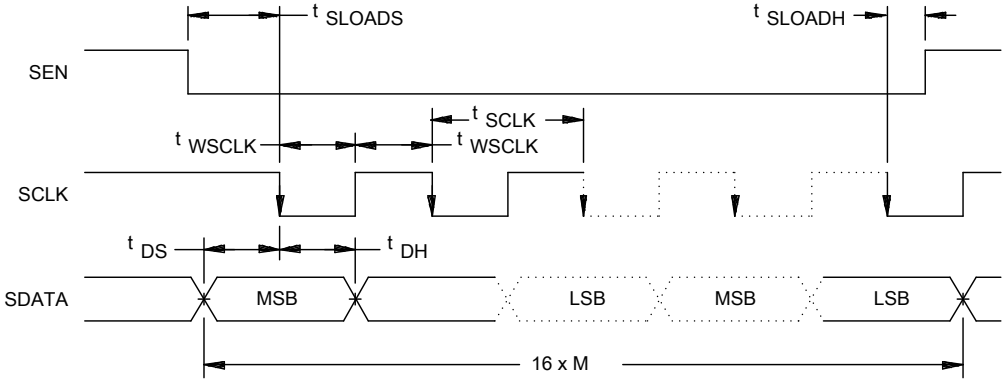


NOTE: It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

FIGURE 4a. Timing waveforms.



DATA COMMUNICATION IS 2-BYTE, MSB FIRST



SERIAL PROGRAMMING INTERFACE TIMING DIAGRAM

FIGURE 4b. Timing waveforms.

TABLE II. Terminal functions.

Terminal name	Type 1/	Description
AV_{DD}	I	Analog power supply.
A_{GND}	I	Analog ground. 2/
DRV_{DD}	I	Output driver power supply.
DR_{GND}	I	Output driver ground.
INP	I	Differential analog input (positive).
INM	I	Differential analog input (negative).
REFP	O	Reference voltage (positive); 0.1-μF capacitor in series with a 1-Ω resistor to GND.
REFM	O	Reference voltage (negative); 0.1-μF capacitor in series with a 1-Ω resistor to GND
IREF	I	Current set; 56-kΩ resistor to GND; do not connect capacitors.
CM	O	Common-mode output voltage.
RESET	I	Reset (active high), 200-kΩ resistor to AV_{DD}.
OE	I	Output enable (active high).
DFS	I	Data format and clock out polarity select. 3/
CLKP	I	Data converter differential input clock (positive).
CLKM	I	Data converter differential input clock (negative).
SEN	I	Serial interface chip select.
SDATA	I	Serial interface data.
SCLK	I	Serial interface clock.
D0 (LSB) – D13 (MSB)	O	Parallel data output.
OVR	O	Over-range indicator bit.
CLKOUT	O	CMOS clock out in sync with data.

1/ I = Input, O = Output
2/ Bond pad is connected to analog ground.
3/ The DFS pin is programmable to four discrete voltage levels: 0, 3/8 AV_{DD}, 5/8 AV_{DD}, and AV_{DD}. The thresholds are centered.

FIGURE 5. Terminal functions.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/05613-01XE	01295	ADS5500MPAPREP	ADS5500M
V62/05613-02XE	01295	ADS5500MPAPEP	ADS5500M

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243