REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02. - CFS	05-10-19	Thomas M. Hess
B	Make corrections to vendor part numbers. For power dissipation capacitance with condition of V_{CCB} = 3.3 V and V_{CCA} = 2.5 V, delete "56 pF" and replace with "55 pF" as specified under Table I. Update boilerplate paragraphs to current requirements. - ro	11-04-12	Charles F. Saffle

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24 Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					
REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 05-07-07	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, 16 BIT 2.5 V TO 3.3 V / 3.3 V TO 5 V LEVEL SHIFTING TRANSCEIVER WITH 3 STATE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/05612**
	REV B	**PAGE** 1 **OF** 17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 bit 2.5 V to 3.3 V / 3.3 V to 5 V level shifting transceiver with 3-state outputs, with an operating temperature range of -40°C to +85°C for device type 01 and an operating temperature range of -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05612	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device types. 1/

Device type	Generic	Circuit function
01	SN74ALVC164245-EP	16 bit 2.5 V to 3.3 V / 3.3 V to 5 V level shifting transceiver with 3-state outputs
02	SN74ALVC164245-EP	16 bit 2.5 V to 3.3 V / 3.3 V to 5 V level shifting transceiver with 3-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MO-118	Plastic small outline package
Y	48	MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

_____

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range:
- (V_{CCA}) ..... -0.5 V to 4.6 V
- (V_{CCB}) ..... -0.5 V to 6.0 V

Input voltage range: (V_I)
- Except I/O ports 4/ ..... -0.5 V to 6.0 V
- I/O port A 5/ ..... -0.5 V to V_{CCA} + 0.5 V
- I/O port B 4/ ..... -0.5 V to V_{CCB} + 0.5 V

Input clamp current, (I_{IK}) ($V_I < 0$) ..... -50 mA

Output clamp current, (I_{OK}) ($V_O < 0$) ..... -50 mA

Continuous output current, (I_O) ..... ±50 mA

Continuous current through each V_{CC} or GND ..... ±100 mA

Package thermal impedance, (θ_{JA}) 6/:
- Case X ..... 63°C/W
- Case Y ..... 70°C/W

Storage temperature range, (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. V_{CCB} at 3.3 V and 5 V. 7/ 8/

Supply voltage, (V_{CCB}) ..... +3.0 V to 5.5 V

Minimum high level input voltage, (V_{IH}) ..... +2.0 V

Maximum low level input voltage, (V_{IL}):
- V_{CCB} = 3.0 V to 3.6 V ..... +0.7 V
- V_{CCB} = 4.5 V to 5.5 V ..... +0.8 V

Input voltage, (V_{IB}) ..... 0 V to V_{CCB}

Output voltage, (V_{OB}) ..... 0 V to V_{CCB}

Maximum high level output current, (I_{OH}) ..... -24 mA

Maximum low level output current, (I_{OL}) ..... 24 mA

Input transition rise or fall rate, ($\Delta t/\Delta v$) ..... 10 ns/V

Operating free air temperature range, (T_A):
- Device type 01 ..... -40°C to +85°C
- Device type 02 ..... -55°C to +125°C

———

2/ For V_{CCB} = 5 V and V_{CCA} = 3.3 V, unless otherwise noted.

3/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4/ This value is limited to 6.0 V maximum.

5/ This value is limited to 4.6 V maximum.

6/ The package thermal impedance is calculated in accordance with JESD 51-7.

7/ All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the manufacturer data for more information.

8/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.5 Recommended operating conditions. V_{CCA} at 2.5 V and 3.3 V. 7/ 8/

Supply voltage, (V_{CCA})	+2.3 V to 3.6 V
Minimum high level input voltage, (V_{IH}):	
V_{CCA} = 2.3 V to 2.7 V	+1.7 V
V_{CCA} = 3.0 V to 3.6 V	+2.0 V
Maximum low level input voltage, (V_{IL}):	
V_{CCA} = 2.3 V to 2.7 V	+0.7 V
V_{CCA} = 3.0 V to 3.6 V	+0.8 V
Input voltage, (V_{IB})	0 V to V_{CCA}
Output voltage, (V_{OB})	0 V to V_{CCA}
Maximum high level output current, (I_{OH}):	
V_{CCA} = 2.3 V	-18 mA
V_{CCA} = 3.0 V	-24 mA
Maximum low level output current, (I_{OL}):	
V_{CCA} = 2.3 V	18 mA
V_{CCA} = 3.0 V	24 mA
Input transition rise or fall rate, ($\Delta t/\Delta v$)	10 ns/V
Operating free air temperature range, (T_A):	
Device type 01	-40°C to +85°C
Device type 02	-55°C to +125°C

7/ All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the manufacturer data for more information.

8/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and in figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram and function table . The logic diagram and function table shall be as shown in figure 3.

3.5.4 Load circuit and voltage waveforms. The load circuit and voltage waveforms be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Test condition 2/ $2.7\ V \le V_{CCA} \le 3.6\ V$ $4.5\ V \le V_{CCB} \le 5.5\ V$ unless otherwise noted	V_{CCA}	V_{CCB}	Device type	Limit		Unit
							Min	Max	
High level output voltage		V_{OH} (B to A)	I_{OH} = -100 μA	2.7 V to 3.6 V		All	V_{CC}-0.2		V
			I_{OH} = -12 mA	2.7 V			2.2		
				3.0 V			2.4		
			I_{OH} = -24 mA	3.0 V			2.0		
High level output voltage		V_{OH} (A to B)	I_{OH} = -100 μA		4.5 V		4.3		
					5.5 V		5.3		
			I_{OH} = -24 mA		4.5 V		3.7		
					5.5 V		4.7		
Low level output voltage		V_{OL} (B to A)	I_{OL} = 100 μA	2.7 V to 3.6 V				0.2	
			I_{OL} = 12 mA	2.7 V				0.4	
			I_{OL} = 24 mA	3.0 V				0.55	
Low level output voltage		V_{OL} (A to B)	I_{OL} = 100 μA		4.5 V to 5.5 V			0.2	
			I_{OL} = 24 mA		4.5 V to 5.5 V			0.55	
Input current	Control inputs	I_I	$V_I = V_{CCA}/V_{CCB}$ or GND	5.5 V	5.5 V			±5	μA
Off state output current	A or B ports	I_{OZ} 3/	$V_O = V_{CCA}/V_{CCB}$ or GND	5.5 V	5.5 V			±10	
Supply current		I_{CC}	$V_I = V_{CCA}/V_{CCB}$ or GND, I_O = 0	5.5 V	5.5 V			40	
Supply current change		ΔI_{CC} 4/	One input at V_{CCA}/V_{CCB} – 0.6 V Other inputs at V_{CCA}/V_{CCB} or GND	3.0 to 3.6 V	4.5 V to 5.5 V			750	
Input capacitance	Control inputs	C_I	$V_I = V_{CCA}/V_{CCB}$ or GND	5.0 V	5.0 V		6.5 typical 5/		pF
I/O capacitance	A or B ports	C_{IO}	$V_O = V_{CCA}/V_{CCB}$ or GND	3.3 V	3.3 V		8.5 typical 5/		

See notes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test		Symbol	Test condition 2/ 2.7 V ≤ V_{CCA} ≤ 3.6 V 4.5 V ≤ V_{CCB} ≤ 5.5 V unless otherwise noted	V_{CCA}	V_{CCB}	Device type	Limit		Unit
							Min	Max	
High level output voltage		V_{OH} (B to A)	I_{OH} = -100 μA	2.3 V to 2.7 V	3.0 V to 3.6 V	All	V_{CCA} -0.2		V
			I_{OH} = -8 mA	2.3 V	3.0 V to 3.6 V		1.7		
			I_{OH} = -12 mA	2.7 V	3.0 V to 3.6 V		1.8		
High level output voltage		V_{OH} (A to B)	I_{OH} = -100 μA	2.3 V to 2.7 V	3.0 V to 3.6 V		V_{CCB} -0.2		
			I_{OH} = -18 mA	2.3 V to 2.7 V	3.0 V		2.2		
Low level output voltage		V_{OL} (B to A)	I_{OL} = 100 μA	2.3 V to 2.7 V	3.0 V to 3.6 V			0.2	
			I_{OL} = 12 mA	2.3 V	3.0 V to 3.6 V			0.6	
Low level output voltage		V_{OL} (A to B)	I_{OL} = 100 μA	2.3 V to 2.7 V	3.0 V to 3.6 V			0.2	
			I_{OL} = 18 mA	2.3 V	3.0 V			0.55	
Input current	Control inputs	I_I	V_I = V_{CCA}/V_{CCB} or GND	2.3 V to 2.7 V	3.0 V to 3.6 V			±5	μA
Off state output current	A or B ports	I_{OZ} 3/	V_O = V_{CCA}/V_{CCB} or GND	2.3 V to 2.7 V	3.0 V to 3.6 V			±10	
Supply current		I_{CC}	V_I = V_{CCA}/V_{CCB} or GND, I_O = 0	2.3 V to 2.7 V	3.0 V to 3.6 V	01		20	
Supply current		I_{CC}	V_I = V_{CCA}/V_{CCB} or GND, I_O = 0	2.3 V to 2.7 V	3.0 V to 3.6 V	02		40	
Supply current change		ΔI_{CC} 4/	One input at V_{CCA}/V_{CCB} – 0.6 V Other inputs at V_{CCA}/V_{CCB} or GND	2.3 V to 2.7 V	3.0 V to 3.6 V	All		750	

See notes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Test condition Over recommended operating free air temperature range unless otherwise noted	V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V				Unit
			V_{CCA} = 2.5 V ±0.2		V_{CCA} = 2.7 V		V_{CCB} = 3.3 V ±0.3 V		
			Min	Max	Min	Max	Min	Max	
Switching characteristics for device type 01.									
Propagation delay time from input A to output B	t_{pd}			7.6		5.9	1	5.8	ns
Propagation delay time from input B to output A				7.6		6.7	1.2	5.8	
Enable time from input $\overline{OE}$ to output B	t_{en}			11.5		9.3	1	8.9	
Disable time from input $\overline{OE}$ to output B	t_{dis}			10.5		9.2	2.1	9.5	
Enable time from input $\overline{OE}$ to output A	t_{en}			12.3		10.2	2	9.1	
Disable time from input $\overline{OE}$ to output A	t_{dis}			9.3		9	2.9	8.6	
Switching characteristics for device type 02.									
Propagation delay time from input A to output B	t_{pd}			8.6		6.9	1	6.8	ns
Propagation delay time from input B to output A				8.6		7.7	1.2	6.8	
Enable time from input $\overline{OE}$ to output B	t_{en}			12.5		10.3	1	9.9	
Disable time from input $\overline{OE}$ to output B	t_{dis}			11.5		10.2	2.1	10.5	
Enable time from input $\overline{OE}$ to output A	t_{en}			14.5		11.2	2	10.1	
Disable time from input $\overline{OE}$ to output A	t_{dis}			11.3		11	2.9	10.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test		Symbol	Test condition Over recommended operating range unless otherwise noted	V_{CCB} = 3.3 V V_{CCA} = 2.5 V Typical	V_{CCB} = 5.0 V V_{CCA} = 3.3 V Typical	Unit
Operating characteristics for device type 01 and device type 02.						
Power dissipation capacitance	Output enabled (B)	C_{pd}	C_L = 50 pF, f = 10 MHz, T_A = 25°C	55	56	pF
	Output disabled (B)			27	6	
	Output enabled (A)			118	56	
	Output disabled (A)			58	6	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

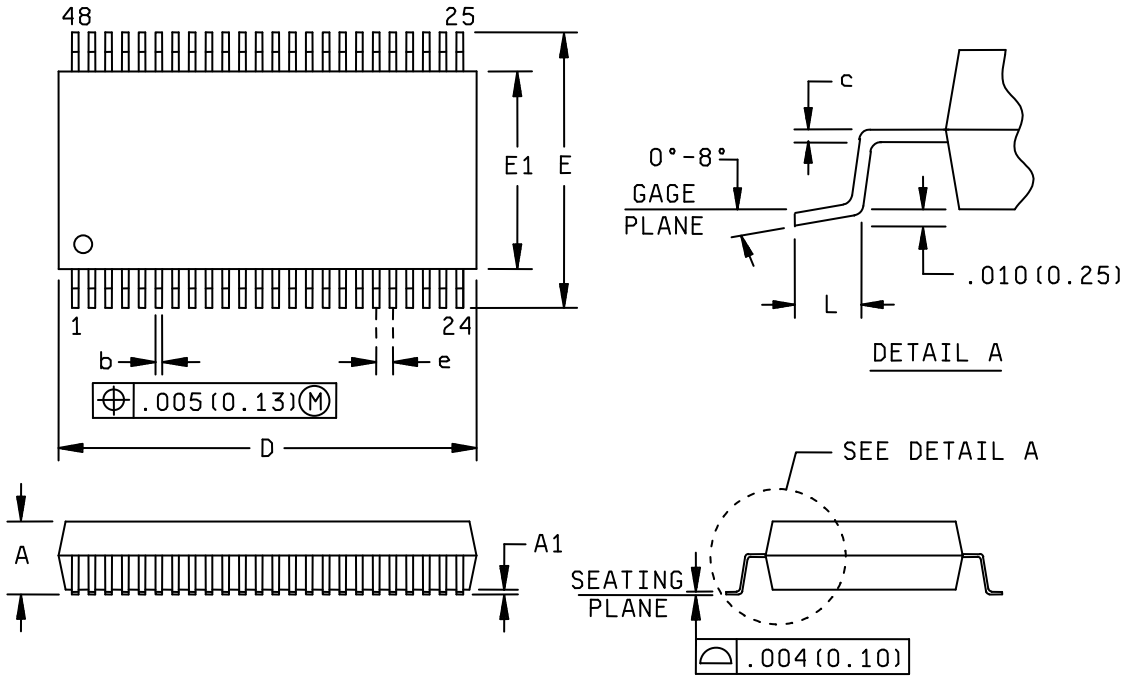
2/ For device type 01, the temperature range is -40°C ≤ T_A ≤ +85°C.
For device type 02, the temperature range is -55°C ≤ T_A ≤ +125°C.

3/ For I/O ports, the parameter I_{OZ} .includes the input leakage current.

4/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated V_{CC}.

5/ Typical values are measured at V_{CCA} = 3.3 V and V_{CCB} = 5 V, T_A = 25°C.

Case X

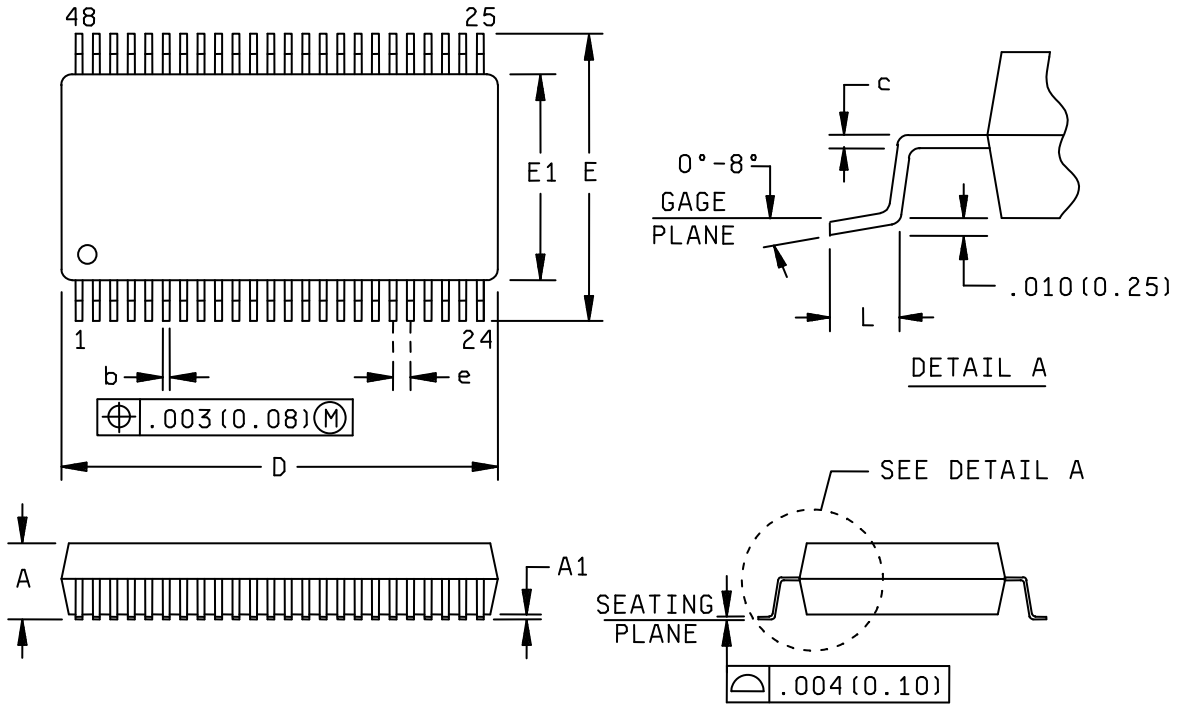


Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		2.79		.110	E	10.03	10.67	.395	.420
A1	0.20		.008		E1	7.39	7.59	.291	.299
b	0.20	0.34	.008	.013	e	0.63 BSC		.002 BSC	
c	0.13	0.25	.005	.010	L	.51	1.02	.020	.040
D	15.75	16.00	.620	.630					

Notes:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MO-118.

FIGURE 1. Case outlines.

Case Y



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	7.90	8.30
A1	0.05	0.15	E1	6.00	6.20
b	0.17	0.27	e	0.50 BSC	
c	0.15 NOM		L	0.50	0.75
D	12.40	12.60			

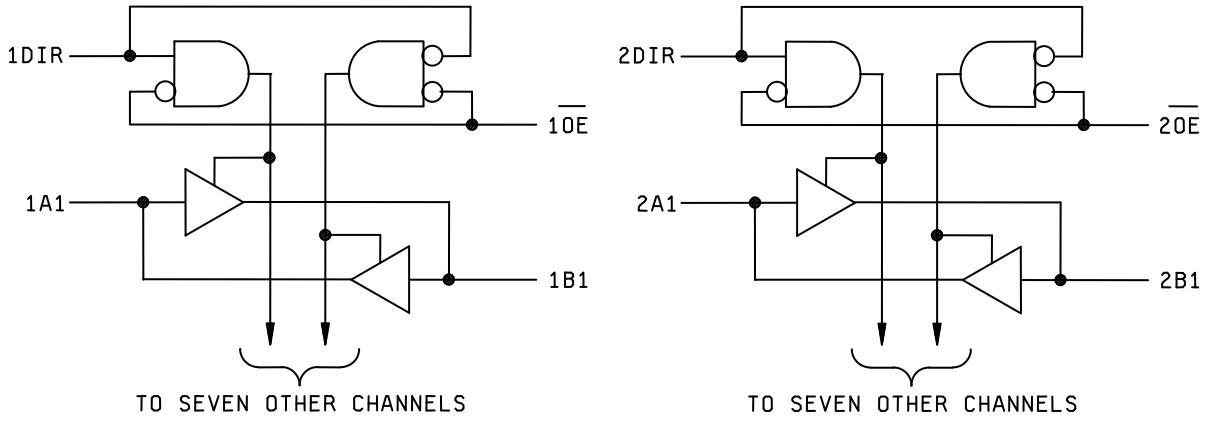
Notes:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 millimeters.
3. Falls within JEDEC MO-153.

FIGURE 1. Case outline - Continued.

Cases X and Y

Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	1DIR	13	2B1	25	$2\overline{OE}$	37	1A8
2	1B1	14	2B2	26	2A8	38	1A7
3	1B2	15	GND	27	2A7	39	GND
4	GND	16	2B3	28	GND	40	1A6
5	1B3	17	2B4	29	2A6	41	1A5
6	1B4	18	V_{CCB}	30	2A5	42	V_{CCA}
7	V_{CCB}	19	2B5	31	V_{CCA}	43	1A4
8	1B5	20	2B6	32	2A4	44	1A3
9	1B6	21	GND	33	2A3	45	GND
10	GND	22	2B7	34	GND	46	1A2
11	1B7	23	2B8	35	2A2	47	1A1
12	1B8	24	2DIR	36	2A1	48	$1\overline{OE}$

FIGURE 2. Terminal connections.



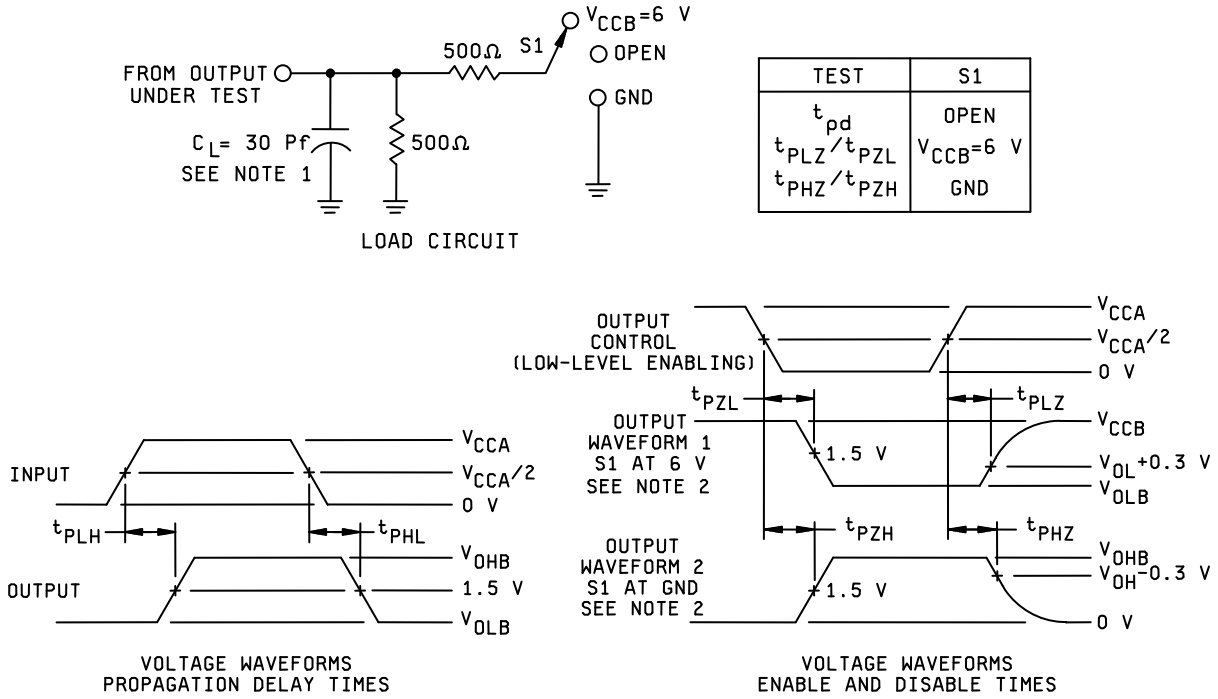
Inputs		Operation
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Function table (each 8 bit section)

FIGURE 3. Logic diagram and function table.

Parameter measurement information

V_{CCA} = 2.5 V ±0.2 V to V_{CCB} = 3.3 V ±0.3 V



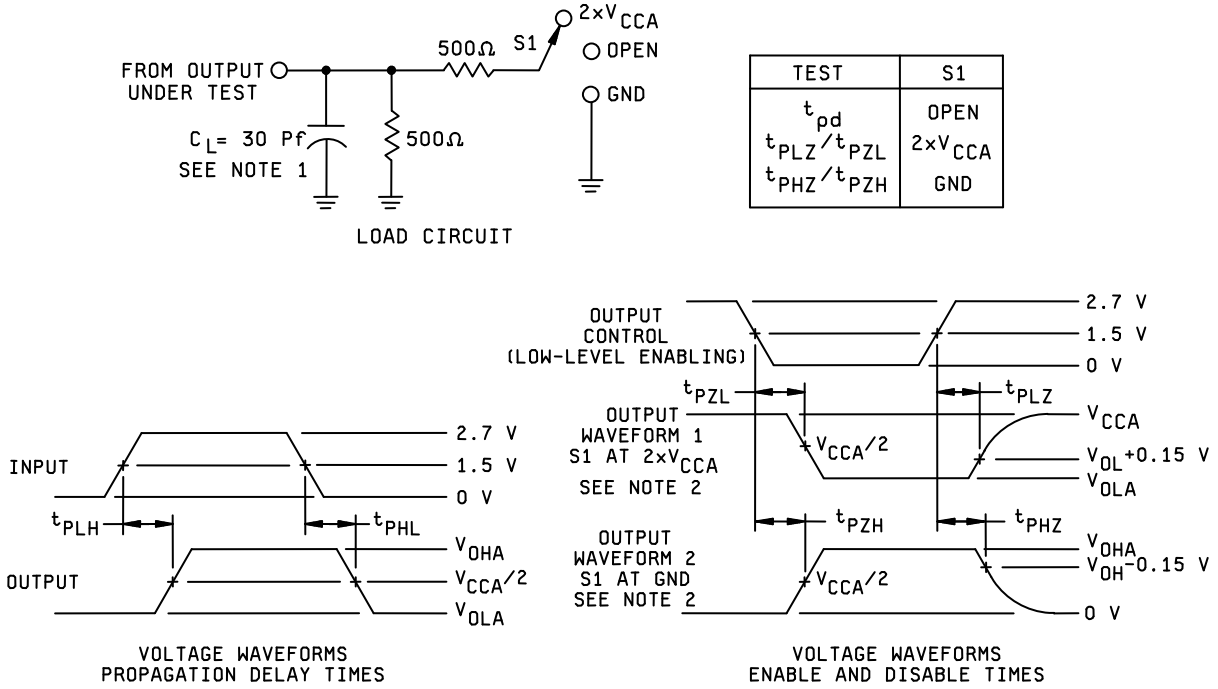
Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
4. The outputs are measured one at a time, with one transaction per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 4. Load circuit and voltage waveforms.

Parameter measurement information

V_{CCB} = 3.3 V ±0.3 V to V_{CCA} = 2.5 V ±0.2 V



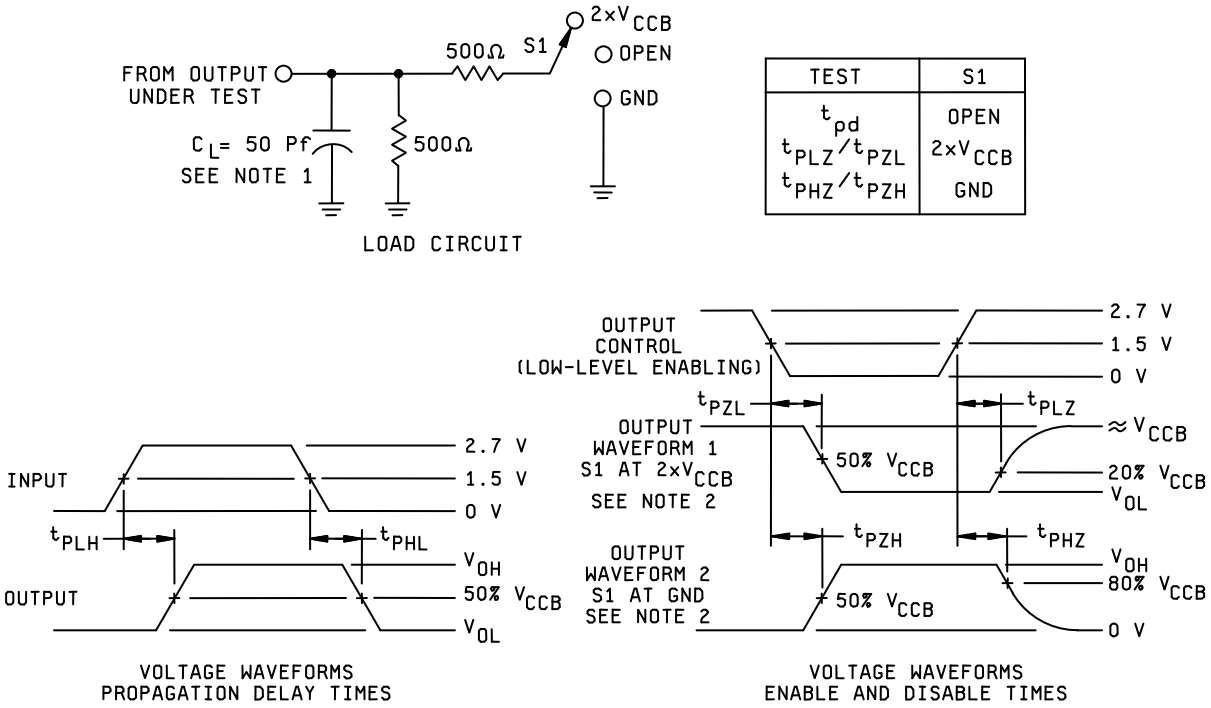
Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
4. The outputs are measured one at a time, with one transaction per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 4. Load circuit and voltage waveforms - Continued.

Parameter measurement information

V_{CCA} = 3.3 V ±0.3 V to V_{CCB} = 5.0 V ±0.5 V



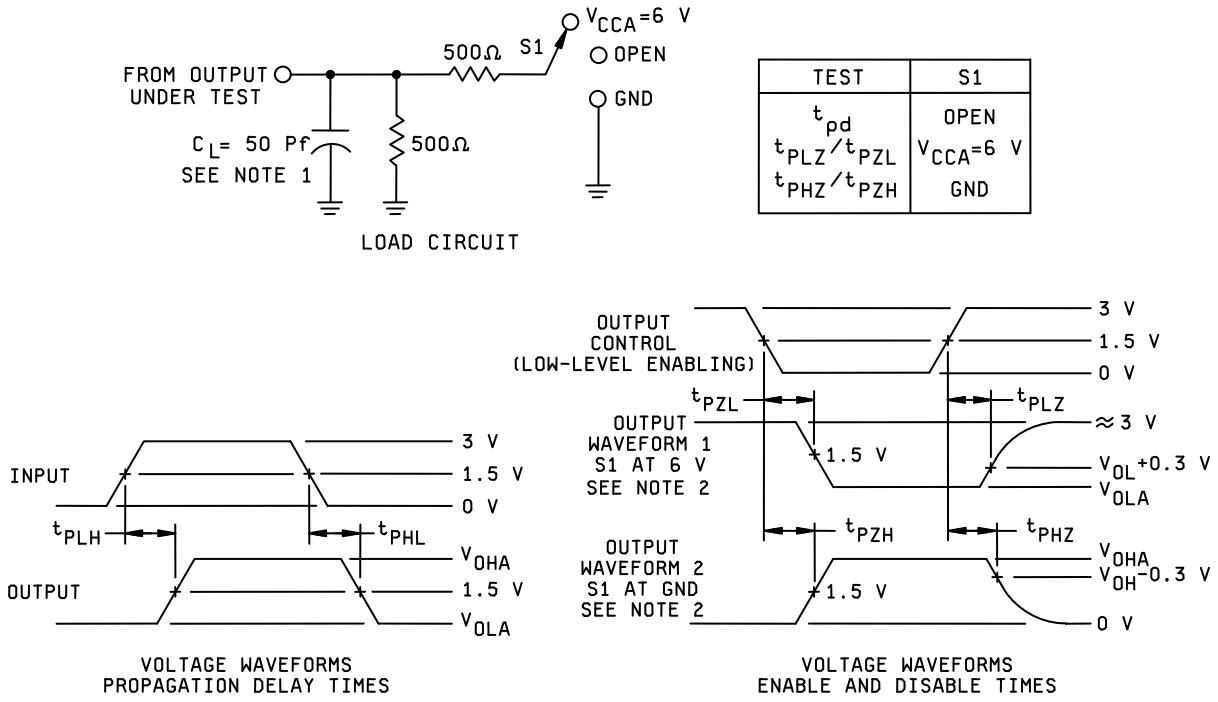
Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
4. The outputs are measured one at a time, with one transaction per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 4. Load circuit and voltage waveforms - Continued.

Parameter measurement information

V_{CCB} = 5.0 V ±0.5 V to V_{CCA} = 2.7 V and 3.3 V ±0.3 V



Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
4. The outputs are measured one at a time, with one transaction per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 4. Load circuit and voltage waveforms - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/05612-01XE	01295	CALVC164245IDLREP 2/	ALVC164245
V62/05612-01YE	01295	CALVC164245IDGGREP 3/	ALVC164245
V62/05612-02YE	01295	CALVC164245MDGGREP 3/	C164245MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ All packages are available taped and reeled of 1000.
3/ All packages are available taped and reeled of 2000.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493