



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1.8 GHz, low distortion, current feedback amplifier, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/05609</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	THS3201-EP	1.8 GHz, low distortion, current feedback amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	JEDEC MS-012	Plastic small outline package
Y <u>2/</u>	8	JEDEC M0-187	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

2/ The manufacture has changed lead frames NiPdAu to NiPdAuAg and location of assembly from their Hana facility to their Shanghai facility. Product with a Lot Trace Code of 1CxxxxH and earlier is a NiPdAu frame from the Hana facility.

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1.3 Absolute maximum ratings. 3/

Supply voltage, (V <sub>S</sub> ) .....	+16.5 V
Input voltage, (V <sub>I</sub> ): .....	±V <sub>S</sub>
Output current, (I <sub>O</sub> ) .....	175 mA
Differential input voltage, (V <sub>ID</sub> ) .....	±3.0 V
Maximum junction temperature, (T <sub>J</sub> ) .....	+150°C <u>4/</u>
Maximum junction temperature, continuous operation, long term reliability, (T <sub>J</sub> ) .....	+125°C <u>5/</u>
Storage temperature range, (T <sub>STG</sub> ) .....	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....	+300°C
ESD ratings:	
HBM .....	+3000 V
CDM .....	+1500 V
MM .....	+100 V
Package dissipation ratings:	

Package	θ <sub>JC</sub> (°C/W)	θ <sub>JA</sub> <u>6/</u> (°C/W)
Case X	38.3	97.5
Case Y <u>7/</u>	4.7	58.4

1.4 Recommended operating conditions.

Supply voltage:	
Maximum dual supply .....	±3.3 V to ±7.5 V
Single supply .....	+6.6 V to +15.0 V
Operating free air temperature range, (T <sub>A</sub> ) .....	-55°C to +125°C

- 3/ Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may affect device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- 4/ The absolute maximum temperature under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may affect device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- 5/ Long term high temperature storage and/or extended used at maximum recommended operating conditions may result in a reduction of overall device life. See figure 3 for additional information on thermal derating.
- 6/ This data was taken using the JEDEC standard high K test PCB.
- 7/ The devices on this drawing may incorporate a thermal pad on the underside of the chip. This act as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. Refer to the manufacturer for more information about utilizing the thermally enhanced package.

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## 2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at <http://www.jedec.org>)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Wirebond life versus temperature. Wirebond life versus temperature shall be as shown in figure 3.

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TABLE I. Electrical performance characteristics. 1/

Test	Test condition $V_S = \pm 7.5\text{ V}$ , $G = +2$ $R_f = 1\text{ k}\Omega$ , $R_L = 100\ \Omega$ unless otherwise noted Device type: All	Limits			Unit	Min/ Typ/ Max
		Typ	Over temperature			
		25°C	25°C	-55°C to +125°C		
<b>AC Performance</b>						
Small signal bandwidth, -3 dB ( $V_O = 200\text{ mV}_{PP}$ )	$G = +1$ , $R_f = 1.2\text{ k}\Omega$	1.8			GHz	Typ
	$G = +2$ , $R_f = 768\ \Omega$	850			MHz	
	$G = +5$ , $R_f = 619\ \Omega$	565				
	$G = +10$ , $R_f = 487\ \Omega$	520				
Bandwidth for 0.1 dB flatness	$G = +2$ , $V_O = 200\text{ mV}_{PP}$ , $R_f = 768\ \Omega$	380			MHz	
Large signal bandwidth	$G = +2$ , $V_O = 2\text{ V}_{PP}$ , $R_f = 715\ \Omega$	880			MHz	
Slew rate	$G = +2$ , $V_O = 5\text{-V step}$ , $R_f = 768\ \Omega$ , Rise/Fall	5400/ 4000			$\text{V}/\mu\text{s}$	
	$G = +2$ , $V_O = 10\text{-V step}$ , $R_f = 768\ \Omega$ , Rise/Fall	9800/ 6700				
Rise and fall time	$G = +2$ , $V_O = 4\text{-V step}$ , $R_f = 768\ \Omega$ , Rise/Fall	0.7/ 0.9			ns	
Setting time to 0.1%	$G = -2$ , $V_O = 2\text{-V step}$	20				
Setting time to 0.01%		60				
Harmonic distortion						
2 <sup>nd</sup> harmonic	$G = +5$ , $f = 10\text{ MHz}$ , $V_O = 2\text{ V}_{PP}$	$R_L = 100\ \Omega$	-64		dBc	
3 <sup>rd</sup> harmonic		$R_L = 100\ \Omega$	-73			
Third order intermodulation distortion (IMD <sub>3</sub> )	$G = +10$ , $f_c = 100\text{ MHz}$ , $\Delta f = 1\text{ MHz}$ , $V_{O(\text{envelope})} = 2\text{ V}_{PP}$		-78			
Noise figure	$G = +10$ , $f_c = 100\text{ MHz}$ , $R_F = 255\ \Omega$ $R_G = 28$	11			dB	
Input voltage noise	$f > 10\text{ MHz}$	1.65			$\text{nV}/\sqrt{\text{Hz}}$	
Input current noise (non inverting)	$f > 10\text{ MHz}$	13.4			$\text{pA}/\sqrt{\text{Hz}}$	
Input current noise (inverting)		20				
Differential gain	$G = +2$ , $R_L = 150\ \Omega$ , $R_f = 768\ \Omega$	NTSC	0.008%			
		PAL	0.004%			
NTSC		0.007°				
PAL		0.011°				

See notes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Test condition $V_S = \pm 7.5\text{ V}$ , $G = +2$ $R_f = 1\text{ k}\Omega$ , $R_L = 100\ \Omega$ Single ended input unless otherwise noted Device type: All	Limits			Unit	Min/ Typ/ Max
		Typ	Over temperature			
		25°C	25°C	-55°C to +125°C		
<b>DC performance</b>						
Open loop transimpedance gain	$V_O = \pm 4\text{ V}$ , $R_L = 1\text{ k}\Omega$	300	200	100	$\text{k}\Omega$	Min
Input offset voltage	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$	$\pm 0.7$	$\pm 4$	$\pm 6$	mV	Max
Average offset voltage drift				$\pm 13$	$\mu\text{V}/^\circ\text{C}$	Typ
Input bias current (inverting)		$\pm 13$	$\pm 65$	$\pm 90$	$\mu\text{A}$	Max
Average bias current drift (-)				$\pm 400$	$\text{nA}/^\circ\text{C}$	Typ
Input bias current (non inverting)		$\pm 14$	$\pm 40$	$\pm 60$	$\mu\text{A}$	Max
Average bias current drift (+)				$\pm 400$	$\text{nA}/^\circ\text{C}$	Typ
<b>Input</b>						
Common mode input range	$R_L = 1\text{ k}\Omega$	$\pm 5.1$	$\pm 5$	$\pm 5$	V	Min
Common mode rejection ratio	$V_{CM} = \pm 3.75\text{ V}$	71	58	53	dB	Min
Inverting input impedance, $Z_{in}$	Open loop	16			$\Omega$	Typ
Input resistance	Non inverting	780			$\text{k}\Omega$	
	Inverting	11			$\Omega$	
Input capacitance	Non inverting	1			pF	
<b>Output</b>						
Voltage output swing	$R_L = 1\text{ k}\Omega$	$\pm 6$	$\pm 5.9$	$\pm 5.7$	V	Min
	$R_L = 100\ \Omega$	$\pm 5.8$	$\pm 5.7$	$\pm 5.35$	V	Min
Current output, sourcing	$R_L = 20\ \Omega$	115	105	100	mA	Min
Current output sinking		100	85	80	mA	Min
Closed loop output impedance	$G = +1$ , $f = 1\text{ MHz}$	0.01			$\Omega$	Typ
<b>Power supply</b>						
Minimum operating voltage			$\pm 3.3$	$\pm 3.3$	V	Min
Maximum operating voltage			$\pm 7.5$	$\pm 7.5$	V	Max
Maximum quiescent current		14	18	22	mA	Max
Power supply rejection (+PSRR)	$V_{S+} = 7\text{ V}$ to $8\text{ V}$ , $R_L = 1\text{ k}\Omega$	69	60	56	dB	Min
Power supply rejection (-PSRR)	$V_{S-} = -7\text{ V}$ to $-8\text{ V}$ , $R_L = 1\text{ k}\Omega$	65	58	55	dB	Min

See notes at end of table.

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TABLE I. Electrical performance characteristics.- Continued. 1/

Test	Test condition $V_S = \pm 5.0\text{ V}$ , $G = +2$ $R_f = 1\text{ k}\Omega$ , $R_L = 100\ \Omega$ Single ended input unless otherwise noted Device type: All	Limits			Unit	Min/ Typ/ Max
		Typ	Over temperature			
		25°C	25°C	-55°C to +125°C		
<b>AC Performance</b>						
Small signal bandwidth, -3 dB ( $V_O = 200\text{ mV}_{PP}$ )	$G = +1$ , $R_f = 1.2\text{ k}\Omega$	1.3			GHz	Typ
	$G = +2$ , $R_f = 715\ \Omega$	725			MHz	
	$G = +5$ , $R_f = 576\ \Omega$	540				
	$G = +10$ , $R_f = 464\ \Omega$	480				
Bandwidth for 0.1 dB flatness	$G = +2$ , $V_O = 200\text{ mV}_{PP}$ , $R_f = 715\ \Omega$	170			MHz	
Large signal bandwidth	$G = +2$ , $V_O = 2\text{ V}_{PP}$ , $R_f = 715\ \Omega$	900			MHz	
Slew rate	$G = +2$ , $V_O = 5\text{-V step}$ , $R_f = 715\ \Omega$ , Rise/Fall	5200/ 4000			V/ $\mu\text{s}$	
Rise and fall time	$G = +2$ , $V_O = 4\text{-V step}$ , $R_f = 715\ \Omega$ , Rise/Fall	0.7/ 0.9			ns	
Setting time to 0.1%	$G = -2$ , $V_O = 2\text{-V step}$	20				
Setting time to 0.01%		60				
Harmonic distortion						
2 <sup>nd</sup> harmonic	$G = +5$ , $f = 10\text{ MHz}$ , $V_O = 2\text{ V}_{PP}$	$R_L = 100\ \Omega$	-69			dBc
3 <sup>rd</sup> harmonic		$R_L = 100\ \Omega$	-75			
Third order intermodulation distortion (IMD <sub>3</sub> )	$G = +10$ , $f_c = 20\text{ MHz}$ , $\Delta f = 1\text{ MHz}$ , $V_{O(\text{envelope})} = 2\text{ V}_{PP}$	-81				
Noise figure	$G = +10$ , $f_c = 100\text{ MHz}$ , $R_F = 255\ \Omega$ $R_G = 28$	11			dB	
Input voltage noise	$f > 10\text{ MHz}$	1.65			nV/ $\sqrt{\text{Hz}}$	
Input current noise (non inverting)	$f > 10\text{ MHz}$	13.4			pA/ $\sqrt{\text{Hz}}$	
Input current noise (inverting)		20				
Differential gain	$G = +2$ , $R_L = 150\ \Omega$ , $R_f = 768\ \Omega$	NTSC	0.006%			
		PAL	0.004%			
Differential phase		NTSC	0.03°			
		PAL	0.04°			

See notes at end of table.

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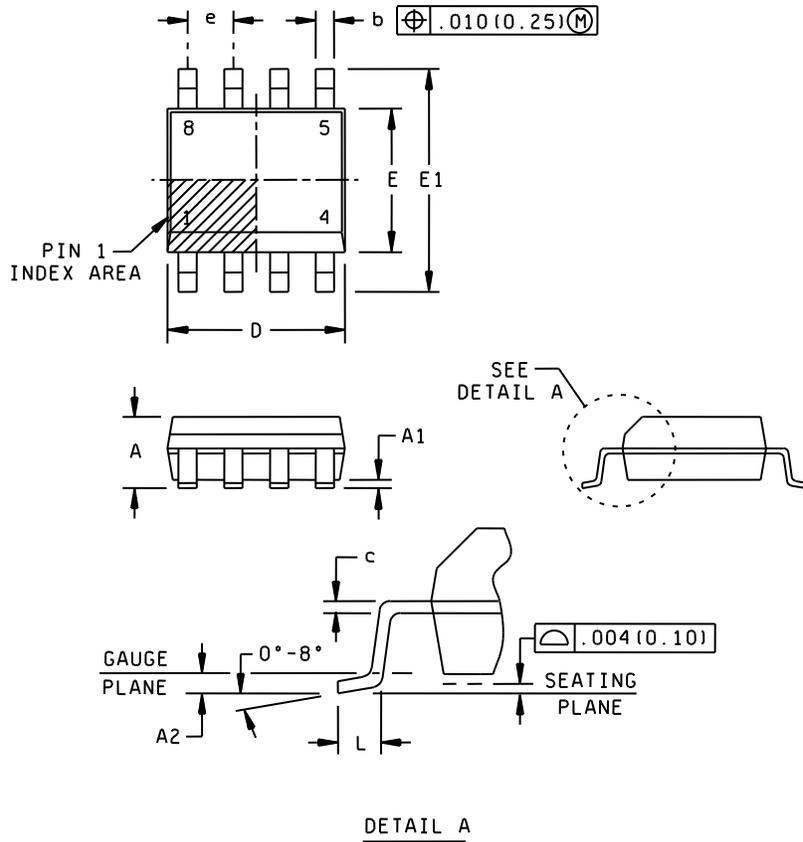
TABLE I. Electrical performance characteristics – Continued. 1/

Test	Test condition $V_S = \pm 5.0\text{ V}$ , $G = +2$ $R_f = 1\text{ k}\Omega$ , $R_L = 100\ \Omega$ Single ended input unless otherwise noted Device type: All	Limits			Unit	Min/ Typ/ Max
		Typ	Over temperature			
		25°C	25°C	-55°C to +125°C		
<b>DC performance</b>						
Open loop transimpedance gain	$V_O = \pm 2\text{ V}$ , $R_L = 1\text{ k}\Omega$	300	200	100	$\text{k}\Omega$	Min
Input offset voltage	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$	$\pm 0.7$	$\pm 3$	$\pm 5.5$	mV	Max
Average offset voltage drift				$\pm 13$	$\mu\text{V}/^\circ\text{C}$	Typ
Input bias current (inverting)		$\pm 13$	$\pm 65$	$\pm 90$	$\mu\text{A}$	Max
Average bias current drift (-)				$\pm 400$	$\text{nA}/^\circ\text{C}$	Typ
Input bias current (non inverting)		$\pm 14$	$\pm 40$	$\pm 60$	$\mu\text{A}$	Max
Average bias current drift (+)				$\pm 400$	$\text{nA}/^\circ\text{C}$	Typ
<b>Input</b>						
Common mode input range	$R_L = 1\text{ k}\Omega$	$\pm 2.6$	$\pm 2.5$	$\pm 2.5$	V	Min
Common mode rejection ratio	$V_{CM} = \pm 2.5\text{ V}$	71	56	50	dB	Min
Inverting input impedance, $Z_{in}$	Open loop, $R_L = 1\text{ k}\Omega$	17.5			$\Omega$	Typ
Input resistance	Non inverting	780			$\text{k}\Omega$	
	Inverting	11			$\Omega$	
Input capacitance	Non inverting	1			pF	
<b>Output</b>						
Voltage output swing	$R_L = 1\text{ k}\Omega$	$\pm 3.65$	$\pm 3.5$	$\pm 3.4$	V	Min
	$R_L = 100\ \Omega$	$\pm 3.45$	$\pm 3.33$	$\pm 3.2$	V	Min
Current output, sourcing	$R_L = 20\ \Omega$	115	105	90	mA	Min
Current output sinking		100	80	75	mA	Min
Closed loop output impedance	$G = +1$ , $f = 1\text{ MHz}$	0.01			$\Omega$	Typ
<b>Power supply</b>						
Minimum operating voltage			$\pm 3.3$	$\pm 3.3$	V	Min
Maximum operating voltage			$\pm 7.5$	$\pm 7.5$	V	Max
Maximum quiescent current		14	16.8	20.5	mA	Max
Power supply rejection (+PSRR)	$V_{S+} = 4.5\text{ V to } 5.5\text{ V}$ , $R_L = 1\text{ k}\Omega$	69	60	56	dB	Min
Power supply rejection (-PSRR)	$V_{S-} = -4.5\text{ V to } -5.5\text{ V}$ , $R_L = 1\text{ k}\Omega$	65	58	55	dB	Min

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		1.75		.069	D	4.80	5.00	.189	.197
A1	0.10	0.25	.004	.010	E	3.80	4.00	.150	.157
A2	0.25 BSC		.010 BSC		E1	5.80	6.20	.228	.244
b	0.31	0.51	.012	.020	e	1.27 BSC		.050 BSC	
c	0.13	0.25	.005	.010	L	0.40	1.27	.016	.050

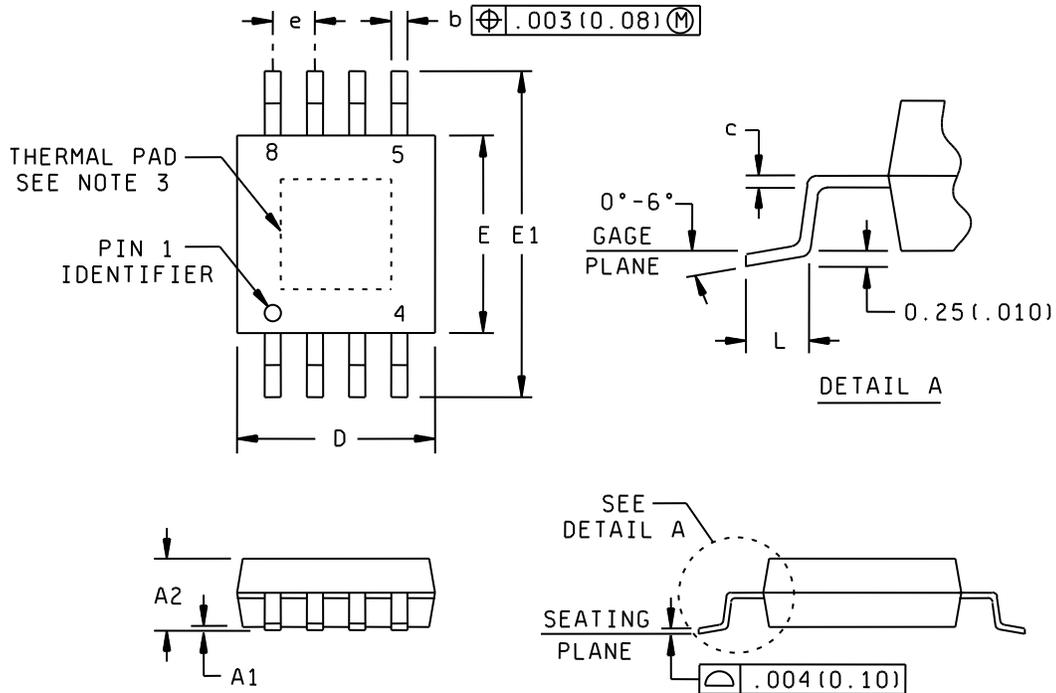
Notes:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) each side.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) each side.
4. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outlines.

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Case Y



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A1	0.05	0.15	.001	.005	E	2.90	3.10	.114	.122
A2	---	1.10	---	.043	E1	4.75	5.05	.187	.198
b	0.25	0.38	.009	.014	e	0.65	BSC	.025	BSC
c	0.13	0.23	.005	.009	L	0.40	0.70	.015	.027
D	2.90	3.10	.114	.122	---	---	---	---	---

Notes:

- Controlling dimensions are millimeter, inch dimensions are given for reference only.
- Body dimensions do not include mold flash or protrusion.
- This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer literature number SLMA002 for information regarding recommended board layout. The vendor datasheet is available from the manufacturer.
- Falls with JEDEC MO-187 variation AA-T.

FIGURE 1. Case outline - Continued.

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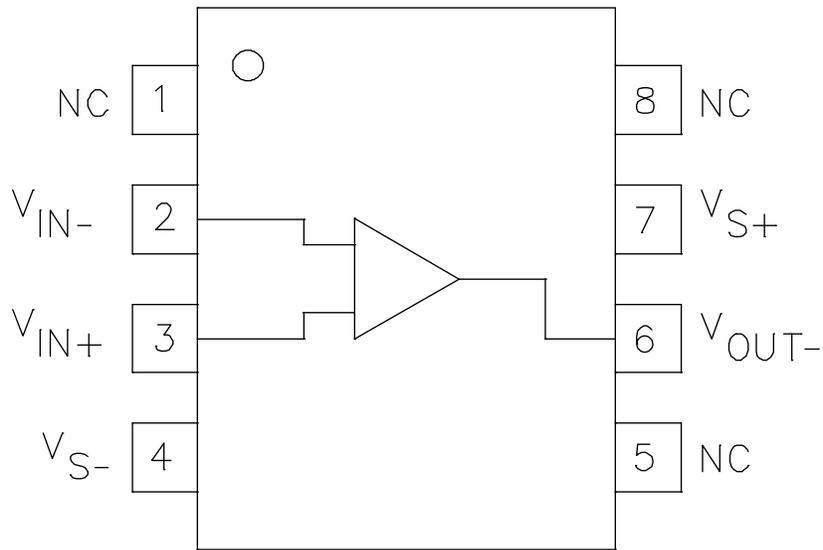


FIGURE 2. Terminal connections.

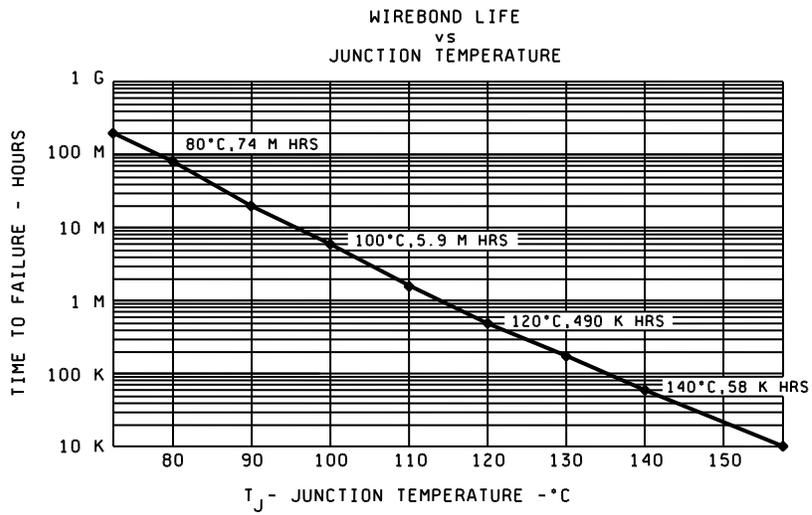


FIGURE 3. Wirebond life versus temperature.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Package marking
V62/05609-01XE	<u>2/</u>	THS3201MDREP <u>3/</u>	—
V62/05609-01YE	01295	THS3201MDGNREP <u>3/ 4/</u>	BLM

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ Not yet available from a source of supplied.
- 3/ The package is available taped and reel. The R suffix standard quality is 2500 (e.g., THS3201MDGNREP).
- 4/ The manufacture has changed lead frames NiPdAu to NiPdAuAg and location of assembly from their Hana facility to their Shanghai facility. Product with a Lot Trace Code of 1CxxxxH and earlier is a NiPdAu frame from the Hana facility.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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