

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct lead finish for device 03 on last page. Update boilerplate. - CFS	05-12-02	Thomas M. Hess
B	Correct operating case temperature for all device types in section 1.3 and 1.4. Add device type 04 to the table in section 6.3. - PHN	06-04-04	Thomas M. Hess
C	Update boilerplate paragraphs to current requirements. - PHN	11-11-29	Thomas M. Hess
D	Add device type 05 and 06 and case outline Y. - PHN	13-05-14	Thomas M. Hess

**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor item drawing

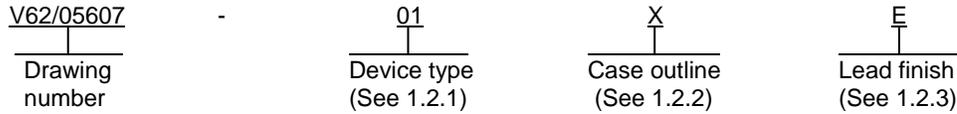
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REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
REV STATUS OF PAGES	REV		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17			

PMIC N/A	PREPARED BY Phu H. Nguyen		DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990																		
Original date of drawing YY MM DD 050607	CHECKED BY Phu H. Nguyen		TITLE MICROCIRCUIT, DIGITAL, FIXED POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON																		
	APPROVED BY Thomas M. Hess																				
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/05607																		
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Fixed-Point Digital Signal Processor microcircuit, with an operating temperature range of -40°C to +105°C (devices 01-03 and 05), -40°C to +85°C (device 04 and 06).

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Clock Rate</u>	<u>Circuit function</u>
01	SM32C6416T-EP	600 MHz	Fixed Point Digital Signal Processor 2/
02	SM32C6416T-EP	720 MHz	Fixed Point Digital Signal Processor 2/
03	SM32C6416T-EP	850 MHz	Fixed Point Digital Signal Processor 2/
04	SM32C6416T-EP	1 GHz	Fixed Point Digital Signal Processor 2/
05	SM32C6416TB-EP	850 MHz	Fixed Point Digital Signal Processor 2/
06	SM32C6416TB-EP	1 GHz	Fixed Point Digital Signal Processor 2/

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>Package style</u>
X	532	Plastic ball grid array
Y	532	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.

2/ Device type 01-04 are no longer available.

Device type 05 should have similar specifications and same temperature range as the 03 device.

Device type 06 should have similar specifications and same temperature range as the 04 device.

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1.3 Absolute maximum ratings. 3/

Supply voltage ranges: (CV _{DD})	-0.5 V to +1.5 V	4/
(DV _{DD})	-0.5 V to +4.4 V	4/
Input voltage ranges: (V _I), (except PCI)	-0.5 V to +4.4 V	
(V _{IP}), (PCI)	-0.5 V to DV _{DD} + 0.5 V	
Output voltage ranges: (V _O) (except PCI)	-0.5 V to +4.4 V	
(V _{OP}), (PCI)	-0.5 V to DV _{DD} + 0.5 V	
Operating case temperature ranges, (T _C):		
Device type 01-03,05	-40°C to +105°C	
Device type 04, 06	-40°C to +85°C	
Storage temperature range, (T _{STG})	-65°C to +150°C	

1.4 Recommended operating conditions.

Supply voltage, core (CV _{DD}) (device type 01)	+1.05 V to +1.16 V	5/
Supply voltage, core (CV _{DD}) (device type 02-04)	+1.16 V to +1.24 V	5/ 6/
Supply voltage, I/O (DV _{DD})	+3.14 V to +3.46 V	
Supply ground, (V _{SS})	0 V	
Minimum high level input voltage, (V _{IH}) (except PCI)	+2.0 V	
Maximum low level input voltage, (V _{IL}) (except PCI)	+0.8 V	
Input voltage, (V _{IP}) (PCI)]	-0.5 V to DV _{DD} + 0.5 V	
High level input voltage (V _{IHP}) (PCI)	0.5DV _{DD} to DV _{DD} + 0.5 V	
Low level input voltage, (V _{ILP}) (PCI)	-0.5 V to 0.3DV _{DD}	
Operating case temperature (T _C):		
Device type 01-03, 05:	-40°C to +105°C	
Device type 04, 06:	-40°C to +85°C	

3/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4/ All voltage values are with respect to V_{SS}.

5/ Future variants of these devices may operate at voltage ranging from 1.0 V to 1.2 V to provide a range of system power/performance options. Manufacturer highly recommends that users design in a supply that can handle multiple voltages within this range (with ±3% tolerances) by implementing simple board changes such as reference resistor values or input pin configuration modifications. Not incorporating a flexible supply may limit the system's ability to easily adapt future versions of these devices.

6/ Device type 01 and 02 are product preview devices.

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1.4 Recommended operating conditions - Continued.

Thermal resistance characteristics case X:

		Air Flow (m/s) <u>7/</u>	°C/W <u>8/</u>	°C/W (with heat sink <u>9/</u>)
1	Junction to case, R Θ_{JC}	N/A	3.11	3.11
2	Junction to board, R Θ_{JB}	N/A	9.95	9.95
3	Junction to free air, R Θ_{JA}	0.00	19.6	14.4
4	Junction to free air, R Θ_{JA}	0.5	17.3	11.5
5	Junction to free air, R Θ_{JA}	1.0	15.6	9.3
6	Junction to free air, R Θ_{JA}	2.0	14.7	8.0
7	Junction to package top, Psi $_{JT}$	N/A	0.83	0.83
8	Junction to board Psi $_{JB}$	N/A	7.88	7.88

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

7/ m/s = meter per second

8/ Numbers are based on simulation

9/ When operating at 1 GHz, a heat sink is required to reduce the thermal resistance characteristics of the package. See manufacturer data for more information.

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3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 Timing reference. The timing reference circuit for AC timing measurements shall be as specified in figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figures 5-40.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test condition At recommended operating ranges unless otherwise noted	Device type	Limits		Unit
				Min	Max	
High level output voltage (except PCI)	V _{OH}	DV _{DD} = Min, I _{OH} = Max	All	2.4		V
High level output voltage (PCI)	V _{OHP}	I _{OHP} = -0.5 mA, DV _{DD} = 3.3 V		0.9DV _{DD} 2/		
Low level output voltage (except PCI)	V _{OL}	DV _{DD} = Min, I _{OL} = Max			0.4	
Low level output voltage (PCI)	V _{OLP}	I _{OLP} = 1.5 mA, DV _{DD} = 3.3 V			0.1DV _{DD} 2/	
Input current (except PCI)[dc]	I _I	V _I = V _{SS} to DV _{DD} no opposing internal resistor			±1	µA
		V _I = V _{SS} to DV _{DD} opposing internal pullup resistor 3/	-200	-50		
		V _I = V _{SS} to DV _{DD} no opposing internal pulldown resistor 3/	50	200		
Input leakage current (PCI)[dc] 4/	I _{IP}	0 < V _{IP} < DV _{DD} = 3.3 V,			±10	
High level output current [dc]	I _{OH}	EMIF, CLKOUT4, CLKOUT6, EMUx			-8	mA
		Timer, UTOPIA, TDO, GPIO (Excluding GP[15:9, 2, 1]), McBSP			-4	
		PCI/HPI			-0.5 2/	
Low level output current [dc]	I _{OL}	EMIF, CLKOUT4, CLKOUT6, EMUx			8	
		Timer, UTOPIA, TDO, GPIO (Excluding GP[15:9, 2, 1]), McBSP			4	
		PCI/HPI			1.5 2/	
Off state output current [dc]	I _{OZ}	V _O = DV _{DD} or 0 V			±20	µA
Core supply current 5/	I _{CDD}	CV _{DD} = 1.2 V, CPU clock = 720 MHz 6/			713 Typ	mA
		CV _{DD} = 1.2 V, CPU clock = 850 MHz			824 Typ	
		CV _{DD} = 1.2 V, CPU clock = 1GHz 6/			952 Typ	
		CV _{DD} = 1.1 V, CPU clock = 600 MHz 6/			558 Typ	
I/O supply current 5/	I _{DDD}	DV _{DD} = 3.3 V, CPU clock = 600 MHz 6/			151 Typ	
Input capacitance	C _I				2	pF
Output capacitance	C _O				3	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted	Limits								Unit
				PLL Mode x20		PLL Mode x12		PLL Mode x6		x1 (Bypass)		
				Min	Max	Min	Max	Min	Max	Min	Max	

INPUT AND OUTPUT CLOCKS

Timing requirements for CLKIN for device type 01 7/ 8/ 9/

1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	33.3	40	20	23.8	13.3	23.8	0	10	ns	
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.4C		0.4C		0.45C			
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.4C		0.4C		0.45C			
4	Transition time, CLKIN	$t_t(CLKIN)$			5		5		5				1
5	Period jitter, CLKIN	$t_j(CLKIN)$			0.02C		0.02C		0.02C				0.02C

Timing requirements for CLKIN for device type 02 7/ 8/ 9/

1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	27.7	40	16	23.8	13.3	23.8	0	10	ns	
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.4C		0.4C		0.45C			
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.4C		0.4C		0.45C			
4	Transition time, CLKIN	$t_t(CLKIN)$			5		5		5				1
5	Period jitter, CLKIN	$t_j(CLKIN)$			0.02C		0.02C		0.02C				0.02C

Timing requirements for CLKIN for device type 03, 05 7/ 8/ 9/

1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	23.5	40	14	23.8	13.3	23.8	0	10	ns	
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.4C		0.4C		0.45C			
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.4C		0.4C		0.45C			
4	Transition time, CLKIN	$t_t(CLKIN)$			5		5		5				1
5	Period jitter, CLKIN	$t_j(CLKIN)$			0.02C		0.02C		0.02C				0.02C

Timing requirements for CLKIN for device type 04, 06 7/ 8/ 9/

1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	23.5	40	14	23.8	13.3	23.8	0	10	ns	
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.4C		0.4C		0.45C			
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.4C		0.4C		0.45C			
4	Transition time, CLKIN	$t_t(CLKIN)$			5		5		5				1
5	Period jitter, CLKIN	$t_j(CLKIN)$			0.02C		0.02C		0.02C				0.02C

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No.	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit	
				CLKMODE = X1, X6, X12, X20			
				Min	Max		
INPUT AND OUTPUT CLOCKS (CONTINUED)							
Switching characteristics for CLKOUT4 <u>10/</u> <u>11/</u> <u>12/</u>							
1	Period jitter, CLKOUT4	$t_{j(CKO4)}$	See figure 7	0	± 175	ps	
2	Pulse duration, CLKOUT4 high	$t_{w(CKO4H)}$		2P-0.7	2P+0.7	ns	
3	Pulse duration, CLKOUT4 low	$t_{w(CKO4L)}$		2P-0.7	2P+0.7		
4	Transaction time, CLKOUT4	$t_{t(CKO4)}$			1		
Switching characteristics for CLKOUT6 <u>10/</u> <u>11/</u> <u>12/</u>							
1	Period jitter, CLKOUT6	$t_{j(CKO6)}$	See figure 7	0	± 175	ps	
2	Pulse duration, CLKOUT6 high	$t_{w(CKO6H)}$		3P-0.7	3P+0.7	ns	
3	Pulse duration, CLKOUT6 low	$t_{w(CKO6L)}$		3P-0.7	3P+0.7		
4	Transaction time, CLKOUT6	$t_{t(CKO6)}$			1		
Timing requirements for ECLKIN for EMIFA and EMIFB <u>7/</u> <u>12/</u> <u>13/</u>							
1	Cycle time, ECLKIN	$t_{c(EKI)}$	See figure 8	CV _{DD} = 1.2 V	6 <u>15/</u>	16P	ns
				CV _{DD} = 1.1 V	7.5 <u>15/</u>	16P	
2	Pulse duration, ECLKIN high	$t_{w(EHIH)}$			2.7		
3	Pulse duration, ECLKIN low	$t_{w(EKIL)}$			2.7		
4	Transaction, ECLKIN	$t_{t(EKI)}$			2		
Switching characteristics for ECLKOUT1 for EMIFA and EMIFB modules <u>10/</u> <u>13/</u> <u>14/</u> <u>16/</u>							
1	Period jitter, ECLKOUT1	$t_{j(EKO1)}$	See figure 8	0	± 175 <u>17/</u>	ps	
2	Pulse duration, ECLKOUT1 high	$t_{w(EKO1H)}$		EH-0.7	EH+0.7	ns	
3	Pulse duration, ECLKOUT1 low	$t_{w(EKO1L)}$		EL-0.7	EL+0.7		
4	Transition time, ECLKOUT1	$t_{t(EKO1)}$			1		
5	Delay time, ECLKIN high to ECLKOUT1 high	$t_{d(EKIH-EKO1L)}$			0.8	8	
6	Delay time, ECLKIN low to ECLKOUT1 low	$t_{d(EKIL-EKO1L)}$			0.8	8	
Switching characteristics for ECLKOUT2 for EMIFA and EMIFB modules <u>10/</u> <u>13/</u> <u>18/</u>							
1	Period jitter, ECLKOUT2	$t_{j(EKO2)}$	See figure 8	0	± 175 <u>17/</u>	ps	
2	Pulse duration, ECLKOUT2 high	$t_{w(EKO2H)}$		0.5NE-0.7	0.5NE+0.7	ns	
3	Pulse duration, ECLKOUT2 low	$t_{w(EKO2L)}$		0.5NE-0.7	0.5NE+0.7		
4	Transition time, ECLKOUT2	$t_{t(EKO2)}$			1		
5	Delay time, ECLKIN high to ECLKOUT2 high	$t_{d(EKIH-EKO2L)}$			3	8	
6	Delay time, ECLKIN low to ECLKOUT2 low	$t_{d(EKIL-EKO2L)}$			3	8	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit
				Min	Max	
ASYNCHRONOUS MEMORY TIMING						
Timing requirements for asynchronous memory cycles for EMIFA module 13/ 19/ 20/						
3	Setup time, EDx valid before \overline{ARE} high	$t_{su}(EDV-AREH)$	See figure 9 and 10	6.5		ns
4	Hold time, EDx valid after \overline{ARE} high	$t_h(AREH-EDV)$		1		
6	Setup time, ARDY valid before ECLKOUTx high	$t_{su}(ARDY-EKO1H)$		3		
7	Hold time, ARDY valid after ECLKOUTx high	$t_h(EKO1H-ARDY)$		1		
Switching characteristics for asynchronous memory cycles for EMIFA module 13/ 20/ 21/ 22/						
1	Output setup time, select signals valid to \overline{ARE} low	$t_{osu}(SELV-AREL)$	See figure 9 and 10	RS*E-1.5		ns
2	Output hold time, \overline{ARE} high to select signals invalid	$t_{oh}(AREH-SELIV)$		RH*E-1.9		
5	Delay time, ECLKOUTx high to \overline{ARE} valid	$t_d(EKO1H-AREV)$		1	7	
8	Output setup time, select signals valid to \overline{AWE} low	$t_{osu}(SELV-AWEL)$		WS*E-1.7		
9	Output hold time, \overline{AWE} high to select signals invalid	$t_{oh}(AWEH-SELIV)$		WH*E-1.8		
10	Delay time, ECLKOUTx high to \overline{AWE} valid	$t_d(EKO1H-AWEV)$		1.3	7.1	
Timing requirements for asynchronous memory cycles for EMIFB module 13/ 19/ 20/						
3	Setup time, EDx valid before \overline{ARE} high	$t_{su}(EDV-AREH)$	See figure 9 and 10	6.2		ns
4	Hold time, EDx valid after \overline{ARE} high	$t_h(AREH-EDV)$		1		
6	Setup time, ARDY valid before ECLKOUT1 high	$t_{su}(ARDY-EKO1H)$		3		
7	Hold time, ARDY valid after ECLKOUT1 high	$t_h(EKO1H-ARDY)$		1.2		
Switching characteristics for asynchronous memory cycles for EMIFB module 13/ 20/ 21/ 22/						
1	Output setup time, select signals valid to \overline{ARE} low	$t_{osu}(SELV-AREL)$	See figure 9 and 10	RS*E-1.6		ns
2	Output hold time, \overline{ARE} high to select signals invalid	$t_{oh}(AREH-SELIV)$		RH*E-1.7		
5	Delay time, ECLKOUTx high to \overline{ARE} valid	$t_d(EKO1H-AREV)$		0.8	6.6	
8	Output setup time, select signals valid to \overline{AWE} low	$t_{osu}(SELV-AWEL)$		WS*E-1.9		
9	Output hold time, \overline{AWE} high to select signals invalid	$t_{oh}(AWEH-SELIV)$		WH*E-1.7		
10	Delay time, ECLKOUTx high to \overline{AWE} valid	$t_d(EKO1H-AWEV)$		0.9	6.7	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit		
				Min	Max			
PROGRAMMABLE SYNCHRONOUS INTERFACE TIMING								
Timing requirements for programmable synchronous interface cycles for EMIFA module 23/								
6	Setup time, read EDx valid before ECLKOUTx high	$t_{su}(EDV-EKOxH)$	See figure 11	2		ns		
7	Hold time, read EDx valid after ECLKOUTx high	$t_h(EKOxH-EDV)$		1.5				
Switching characteristics for programmable synchronous interface cycles for EMIFA module 23/ 24/								
1	Delay time, ECLKOUTx high to \overline{CEx} valid	$t_d(EKOxH-CEV)$	See figure 11-13	1.3	4.9	ns		
2	Delay time, ECLKOUTx high to \overline{BEx} valid	$t_d(EKOxH-BEV)$			4.9			
3	Delay time, ECLKOUTx high to \overline{BEx} invalid	$t_d(EKOxH-BEIV)$		1.3				
4	Delay time, ECLKOUTx high to EAx valid	$t_d(EKOxH-EAV)$			4.9			
5	Delay time, ECLKOUTx high to EAx invalid	$t_d(EKOxH-EAIV)$		1.3				
8	Delay time, ECLKOUTx high to $\overline{SADS/SRE}$ valid	$t_d(EKOxH-ADSV)$		1.3	4.9			
9	Delay time, ECLKOUTx high to \overline{SOE} valid	$t_d(EKOxH-OEV)$		1.3	4.9			
10	Delay time, ECLKOUTx high to \overline{EDx} valid	$t_d(EKOxH-EDV)$			4.9			
11	Delay time, ECLKOUTx high to \overline{EDx} invalid	$t_d(EKOxH-EDIV)$		1.3				
12	Delay time, ECLKOUTx high to \overline{SWE} invalid	$t_d(EKOxH-WEV)$		1.3	4.9			
Timing requirements for programmable synchronous interface cycles for EMIFB module 23/								
6	Setup time, read EDx valid before ECLKOUTx high	$t_{su}(EDV-EKOxH)$		See figure 11	3.1			ns
7	Hold time, read EDx valid after ECLKOUTx high	$t_h(EKOxH-EDV)$	1.5					
Switching characteristics for programmable synchronous interface cycles for EMIFB module 23/ 24/								
1	Delay time, ECLKOUTx high to \overline{CEx} valid	$t_d(EKOxH-CEV)$	See figure 11-13	1.3	6.4	ns		
2	Delay time, ECLKOUTx high to \overline{BEx} valid	$t_d(EKOxH-BEV)$			6.4			
3	Delay time, ECLKOUTx high to \overline{BEx} invalid	$t_d(EKOxH-BEIV)$		1.3				
4	Delay time, ECLKOUTx high to EAx valid	$t_d(EKOxH-EAV)$			6.4			
5	Delay time, ECLKOUTx high to EAx invalid	$t_d(EKOxH-EAIV)$		1.3				
8	Delay time, ECLKOUTx high to $\overline{SADS/SRE}$ valid	$t_d(EKOxH-ADSV)$		1.3	6.4			
9	Delay time, ECLKOUTx high to \overline{SOE} valid	$t_d(EKOxH-OEV)$		1.3	6.4			
10	Delay time, ECLKOUTx high to \overline{EDx} valid	$t_d(EKOxH-EDV)$			6.4			
11	Delay time, ECLKOUTx high to \overline{EDx} invalid	$t_d(EKOxH-EDIV)$		1.3				
12	Delay time, ECLKOUTx high to \overline{SWE} invalid	$t_d(EKOxH-WEV)$		1.3	6.4			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit		
				Min	Max			
SYNCHRONOUS DRAM TIMING								
Timing requirements for synchronous DRAM cycles for EMIFA module 25/								
6	Setup time, read EDx valid before ECLKOUTx high	$t_{su(EDV-EKO1H)}$	See figure 14	0.6		ns		
7	Hold time, read EDx valid after ECLKOUTx high	$t_{h(EKO1H-EDV)}$		CV _{DD} = 1.2 V	1.8			
			CV _{DD} = 1.1 V	2.0				
Switching characteristics for synchronous DRAM cycles for EMIFA module 25/								
1	Delay time, ECLKOUTx high to \overline{CEx} valid	$t_d(EKO1H-CEV)$	See figure 14-21	1.3	4.9	ns		
2	Delay time, ECLKOUTx high to \overline{BEx} valid	$t_d(EKO1H-BEV)$					4.9	
3	Delay time, ECLKOUTx high to \overline{BEx} invalid	$t_d(EKO1H-BEIV)$			1.3			
4	Delay time, ECLKOUTx high to EAx valid	$t_d(EKO1H-EAV)$					4.9	
5	Delay time, ECLKOUTx high to EAx invalid	$t_d(EKO1H-EAIV)$			1.3			
8	Delay time, ECLKOUTx high to \overline{SDCAS} valid	$t_d(EKO1H-CASV)$			1.3		4.9	
9	Delay time, ECLKOUTx high to \overline{EDx} valid	$t_d(EKO1H-EDV)$					4.9	
10	Delay time, ECLKOUTx high to \overline{EDx} invalid	$t_d(EKO1H-EDIV)$			1.3			
11	Delay time, ECLKOUTx high to \overline{SDWE} valid	$t_d(EKO1H-WEV)$			1.3		4.9	
12	Delay time, ECLKOUTx high to \overline{SDRAS} valid	$t_d(EKO1H-RAS)$			1.3		4.9	
13	Delay time, ECLKOUTx high to \overline{ASDCKE} valid (EMIFA only)	$t_d(EKO1H-ACKEV)$			1.3		4.9	
14	Delay time, ECLKOUTx high to \overline{PDT} valid	$t_d(EKO1H-PDTV)$			1.3		4.9	
Timing requirements for synchronous DRAM cycles for EMIFB module 24/								
6	Setup time, read EDx valid before ECLKOUTx high	$t_{su(EDV-EKO1H)}$		See figure 14	2.1			ns
7	Hold time, read EDx valid after ECLKOUTx high	$t_{h(EKO1H-EDV)}$	2.5					
Switching characteristics for synchronous DRAM cycles for EMIFB module 25/								
1	Delay time, ECLKOUTx high to \overline{CEx} valid	$t_d(EKO1H-CEV)$	See figure 14-21	1.3	6.4	ns		
2	Delay time, ECLKOUTx high to \overline{BEx} valid	$t_d(EKO1H-BEV)$					6.4	
3	Delay time, ECLKOUTx high to \overline{BEx} invalid	$t_d(EKO1H-BEIV)$			1.3			
4	Delay time, ECLKOUTx high to EAx valid	$t_d(EKO1H-EAV)$					6.4	
5	Delay time, ECLKOUTx high to EAx invalid	$t_d(EKO1H-EAIV)$			1.3			
8	Delay time, ECLKOUTx high to \overline{SDCAS} valid	$t_d(EKO1H-CASV)$			1.3		6.4	
9	Delay time, ECLKOUTx high to \overline{EDx} valid	$t_d(EKO1H-EDV)$					6.4	
10	Delay time, ECLKOUTx high to \overline{EDx} invalid	$t_d(EKO1H-EDIV)$			1.3			
11	Delay time, ECLKOUTx high to \overline{SDWE} valid	$t_d(EKO1H-WEV)$			1.3		6.4	
12	Delay time, ECLKOUTx high to \overline{SDRAS} valid	$t_d(EKO1H-RAS)$			1.3		6.4	
13	Delay time, ECLKOUTx high to \overline{ASDCKE} valid (EMIFA only)	$t_d(EKO1H-ACKEV)$			1.3		6.4	
14	Delay time, ECLKOUTx high to \overline{PDT} valid	$t_d(EKO1H-PDTV)$			1.3		6.4	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit
				Min	Max	

HOLD/HOLDA TIMING

Timing requirements for the $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ cycles for EMIFA and EMIFB modules 26/

3	Hold time, $\overline{\text{HOLD}}$ low after $\overline{\text{HOLDA}}$ low	$t_{oh}(\overline{\text{HOLDAL}}-\overline{\text{HOLDL}})$	See figure 22	E		ns
---	---	--	---------------	---	--	----

Switching characteristics for the $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ cycles for EMIFA and EMIFB modules 26/ 27/ 28/

1	Delay time, $\overline{\text{HOLD}}$ low to EMIF bus high impedance	$t_{d}(\overline{\text{HOLDL}}-\text{EMHZ})$	See figure 22	2E	<u>29/</u>	ns
2	Delay time, EMIF bus high to $\overline{\text{HOLDA}}$ low	$t_{d}(\text{EMHZ}-\overline{\text{HOLDAL}})$		0	2E	
4	Delay time, $\overline{\text{HOLD}}$ high to EMIF bus low impedance	$t_{d}(\overline{\text{HOLDH}}-\text{EMLZ})$		2E	7E	
5	Delay time, EMIF bus low impedance to $\overline{\text{HOLDA}}$ low	$t_{d}(\text{EMLZ}-\overline{\text{HOLDAL}})$		0	2E	
6	Delay time, $\overline{\text{HOLD}}$ low to ECLKOUTx high impedance	$t_{d}(\overline{\text{HOLDL}}-\text{EKOHZ})$		2E	<u>29/</u>	
7	Delay time, $\overline{\text{HOLD}}$ high to ECLKOUTx low impedance	$t_{d}(\overline{\text{HOLDH}}-\text{EKOLZ})$		2E	7E	

BUSREQ TIMING

Switching characteristics for BUSREQ cycles for EMIFA and EMIFB modules

1	Delay time, AECLKOUTx high to ABUSREQ valid	$t_{d}(\text{AEKO1H}-\text{ABUSRV})$	See figure 23	1	5.5	ns
2	Delay time, AECLKOUTx high to BBUSREQ valid	$t_{d}(\text{AEKO1H}-\text{BBUSRV})$		0.9	5.5	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit
				Min	Max	
RESET TIMING						
Timing requirements for reset 12/						
1	Width of the $\overline{\text{RESET}}$ pull (PLL stable) 30/	$t_{w(\text{RST})}$	See figure 24	250		μs
	Width of the $\overline{\text{RESET}}$ pull (PLL needs to sync up) 31/			250		
16	Setup time, boot configuration bits valid before $\overline{\text{RESET}}$ high 32/	$t_{\text{su}(\text{boot})}$		4E or 4C 33/		ns
17	Hold time, boot configuration bits valid after $\overline{\text{RESET}}$ high 32/	$t_{\text{h}(\text{boot})}$		4P		
18	Setup time, PCLK active before $\overline{\text{RESET}}$ high 34/	$t_{\text{su}(\text{PCLK-RSTH})}$		32N		
Switching characteristics during reset 12/ 26/ 35/						
2	Delay time, $\overline{\text{RESET}}$ low to ECLKIN synchronized internally	$t_{\text{d}(\text{RSTL-ECKI})}$	See figure 24	2E	3P+20E	ns
3	Delay time, $\overline{\text{RESET}}$ high to ECLKIN synchronized internally	$t_{\text{d}(\text{RSTH-ECKI})}$		2E	16 070P	
4	Delay time, $\overline{\text{RESET}}$ low to ECLKOUT1 high impedance	$t_{\text{d}(\text{RSTL-ECKO1HZ})}$		2E		
5	Delay time, $\overline{\text{RESET}}$ high to ECLKOUT1 valid	$t_{\text{d}(\text{RSTH-ECKO1V})}$			16 070P	
6	Delay time, $\overline{\text{RESET}}$ low to EMIF Z high impedance	$t_{\text{d}(\text{RSTL-EMIFZH})}$		2E	3P+4E	
7	Delay time, $\overline{\text{RESET}}$ high to EMIF Z valid	$t_{\text{d}(\text{RSTH-EMIFZV})}$		16E	16 070P	
8	Delay time, $\overline{\text{RESET}}$ low to EMIF high group invalid	$t_{\text{d}(\text{RSTL-EMIFHV})}$		2E		
9	Delay time, $\overline{\text{RESET}}$ high to EMIF high group valid	$t_{\text{d}(\text{RSTH-EMIFHV})}$			16 070P	
10	Delay time, $\overline{\text{RESET}}$ low to EMIF low group invalid	$t_{\text{d}(\text{RSTL-EMIFLV})}$		2E		
11	Delay time, $\overline{\text{RESET}}$ high to EMIF low group valid	$t_{\text{d}(\text{RSTH-EMIFLV})}$			16 070P	
12	Delay time, $\overline{\text{RESET}}$ low to low to low group invalid	$t_{\text{d}(\text{RSTL-LOWIV})}$		0		
13	Delay time, $\overline{\text{RESET}}$ high to low to low group valid	$t_{\text{d}(\text{RSTH-LOWV})}$			16 070P	
14	Delay time, $\overline{\text{RESET}}$ low to Z group high impedance	$t_{\text{d}(\text{RSTL-ZHZ})}$		0		
15	Delay time, $\overline{\text{RESET}}$ high to Z group valid	$t_{\text{d}(\text{RSTH-ZV})}$		2P	16 070P	
EXTERNAL INTERRUPT TIMING						
Timing requirements for external interrupts 12/						
1	Width of the NMI interrupt pulse low	$t_{w(\text{LOW})}$	See figure 25	4P		ns
	Width of the EXT_INT interrupt pulse low			8P		
2	Width of the NMI interrupt pulse high	$t_{w(\text{HIGH})}$		4P		
	Width of the EXT_INT interrupt pulse high			8P		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit
				Min	Max	
HOST PORT INTERFACE (HPI) TIMING						
Timing requirements for host port interface cycles <u>12/ 36/</u>						
1	Setup time, select signals <u>37/</u> valid before $\overline{\text{HSTROBE}}$ low	$t_{su}(\text{SELV-HSTBL})$	See figure 26-29	5		ns
2	Hold time, select signals <u>37/</u> valid after $\overline{\text{HSTROBE}}$ low	$t_h(\text{HSTBL-SELV})$		2.4		
3	Pulse duration, time, $\overline{\text{HSTROBE}}$ low	$t_w(\text{HSTBL})$		4P <u>38/</u>		
4	Pulse duration, time, $\overline{\text{HSTROBE}}$ high between consecutive accesses	$t_w(\text{HSTBH})$		4P		
10	Setup time, select signals <u>37/</u> valid before $\overline{\text{HAS}}$ low	$t_{su}(\text{SELV-HASL})$		5		
11	Hold time, select signals <u>37/</u> valid after $\overline{\text{HAS}}$ low	$t_h(\text{HASL-SELV})$		2		
12	Setup time, host data valid before $\overline{\text{HSTROBE}}$ low	$t_{su}(\text{HDV-HSTBH})$		5		
13	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high	$t_h(\text{HSTBH-HDV})$		2.8		
14	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.	$t_h(\text{HRDYL-HSTBL})$		2		
18	Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low	$t_{su}(\text{HASL-HSTBL})$		2		
19	Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low	$t_h(\text{HSTBL-HASL})$	2.1			
Switching characteristics during host port interface cycles <u>12/ 36/</u>						
6	Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ high <u>39/</u>	$t_d(\text{HSTBL-HRDYH})$	See figure 26-29	1.3	4P+9	ns
7	Delay time, $\overline{\text{HSTROBE}}$ low to HD low impedance for an HPI read	$t_d(\text{HSTBL-HDLZ})$		2		
8	Delay time, HD valid to $\overline{\text{HRDY}}$ low	$t_d(\text{HDV-HRDYL})$		-3		
9	Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high	$t_{oh}(\text{HSTBH-HDV})$		1.5		
15	Delay time, $\overline{\text{HSTROBE}}$ high to HD high impedance	$t_d(\text{HSTBH-HDHZ})$			12	
16	Delay time, $\overline{\text{HSTROBE}}$ low to HD valid (HPI16 mode, second half-word only)	$t_d(\text{HSTBL-HDV})$			4P+8	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit
				Min	Max	
PERIPHERAL COMPONENT INTERCONNECTION (PCI) TIMING						
Timing requirements for PCLK 12/ 40/						
1	Cycle time, PCLK	$t_c(\text{PCLK})$	See figure 30	30 (or 8P 41/)		ns
2	Pulse duration, PCLK high	$t_w(\text{PCLKH})$		11		
3	Pulse duration, PCLK low	$t_w(\text{PCLKL})$		11		
4	$\Delta v/\Delta t$ slew rate, PCLK	$t_{sr}(\text{PCLK})$		1	4	V/ns
Timing requirements for PCI reset						
1	Pulse duration, PRST	$t_w(\text{PRST})$	See figure 30	1		ms
2	Setup time, PCLK active before PRST high	$t_{su}(\text{PCLKA-PRSTH})$		100		μs
Timing requirements for PCI inputs						
5	Setup time, input valid before PCLK high	$t_{su}(\text{IV-PCLKH})$	See figure 31	7		ns
6	Hold time, input valid after PCLK high	$t_h(\text{IV-PCLKH})$		0		
Switching characteristics for PCI outputs						
1	Delay time, PCLK high to output valid	$t_d(\text{PCLKH-OV})$	See figure 31		11	ns
2	Delay time, PCLK high to output invalid	$t_d(\text{PCLKH-OIV})$		2		
3	Delay time, PCLK high to output low impedance	$t_d(\text{PCLKH-OLZ})$		2		
4	Delay time, PCLK high to output high impedance	$t_d(\text{PCLKH-OHZ})$			28	
Timing requirements for serial EEPROM interface						
8	Setup time, XSP_DI valid before XSP_CLK high	$t_{su}(\text{DIV-CLKH})$	See figure 32	50		ns
9	Hold time, XSP_DI valid after XSP_CLK high	$t_h(\text{CLKH-DIV})$		0		
Switching characteristics for serial EEPROM interface 12/						
1	Pulse duration, XSP_CS low	$t_w(\text{CSL})$	See figure 32	4092P Typ		ns
2	Delay time, XSP_CLK low to XSP_CS low	$t_d(\text{CLKL-CSL})$		0		
3	Delay time, XSP_CS high to XSP_CLK high	$t_d(\text{CSH-CLKH})$		2046P Typ		
4	Pulse duration, XSP_CLK high	$t_w(\text{CLKH})$		2046P Typ		
5	Pulse duration, XSP_CLK low	$t_w(\text{CLKL})$		2046P Typ		
6	Output setup time, XSP_DO valid after XSP_CLK high	$t_{osu}(\text{DOV-CLKH})$		2046P Typ		
7	Output hold time, XSP_DO valid after XSP_CLK high	$t_{oh}(\text{CLKH-DOV})$		2046P Typ		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit		
				Min	Max			
MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING - CONTINUED								
Timing requirements for McBSP <u>12/ 42/</u>								
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 33	CLKR/X ext	4P or 6.67 <u>43/ 44/</u>	ns		
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext	$0.5t_{c(CKRX)} - 1$ <u>45/</u>			
5	Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR ext	9			
				CLKR int	1.3			
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR ext	6			
				CLKR int	3			
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR ext	8			
				CLKR int	0.9			
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR ext	3			
				CLKR int	3.1			
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKR ext	9			
			CLKR int	1.3				
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-FXH)}$	CLKR ext	6				
			CLKR int	3				
Switching characteristics for McBSP <u>42/ 46/</u>								
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	$t_{d(CKSH-CKRXH)}$	See figure 33		1.4	10	ns	
2	Cycle time, CLKR/X	$t_{c(CKRX)}$		CLKR/X int	4P or 6.67 <u>43/ 44/</u>			
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X int	C-1 <u>47/</u>	C+1 <u>47/</u>		
4	Delay time, CLKR/X high or CLKR/X low	$t_{d(CKRH-FRV)}$		CLKR int	-2.1	3		
9	Delay time, CLKX high to internal FSX valid	$t_{d(CKXH-FXV)}$		CLKX int	-1.7	3		
				CLKX ext	1.7	9		
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{d(CKXH-DXHZ)}$		CLKX int	-3.9	4		
				CLKX ext	-2.1	9		
13	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		CLKX int	-3.9+D1 <u>48/</u>	4+D2 <u>48/</u>		
				CLKX ext	2.0+D1 <u>48/</u>	9+D2 <u>48/</u>		
14	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	$t_{d(FXH-DXV)}$		FSX int	-2.3+D1 <u>49/</u>	5.6+D2 <u>49/</u>		
				FSX ext	1.9+D1 <u>49/</u>	9+D2 <u>49/</u>		
Timing requirements for FSR when GSYNC = 1								
1	Setup time, FSR high before CLKS high	$t_{su(FRH-CKSH)}$		See figure 34		4		ns
2	Hold time, FSR high after CLKS high	$t_{h(CKSH-FRH)}$			4			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	

MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING - CONTINUED

Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 12/ 50/

4	Setup time, DR valid before CLKX low	$t_{su}(DRV-CKXL)$	See figure 35	12		2-12P		ns
5	Hold time, DR valid after CLKX low	$t_h(CKXL-DRV)$		4		5+24P		

Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 12/ 50/

1	Hold time, FSX low after CLKX low <u>51/</u>	$t_h(CKXL-FXL)$	See figure 35	T-2	T+3			ns
2	Delay time, FSX low to CLKX high <u>52/</u>	$t_d(FXL-CKXH)$		L-2	L+3			
3	Delay time, CLKX high to DX valid	$t_d(CKXH-DXV)$		-2	4	12P+2.8	20P+17	
6	Disable time, DX high impedance following last data bit for CLKX low	$t_{dis}(CKXL-DXHZ)$		L-2	L+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis}(FXH-DXHZ)$				4P+3	12P+17	
8	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$				8P+1.8	16P+17	

Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 12/ 50/

4	Setup time, DR valid before CLKX high	$t_{su}(DRV-CKXH)$	See figure 35	12		2-12P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		5+24P		

Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 12/ 50/

1	Hold time, FSX low after CLKX low <u>51/</u>	$t_h(CKXL-FXL)$	See figure 35	L-2	L+3			ns
2	Delay time, FSX low to CLKX high <u>52/</u>	$t_d(FXL-CKXH)$		T-2	T+3			
3	Delay time, CLKX low to DX valid	$t_d(CKXL-DXV)$		-2	4	12P+2.8	20P+17	
6	Disable time, DX high impedance following last data bit for CLKX low	$t_{dis}(CKXL-DXHZ)$		-2	4	12P+3	20P+17	
7	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$		H-2	H+4	8P+2	16P+17	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	

MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING - CONTINUED

Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 12/ 50/

4	Setup time, DR valid before CLKX high	$t_{su}(DRV-CKXH)$	See figure 36	12		2-12P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		5+24P		

Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 11/ 45/

1	Hold time, FSX low after CLKX high <u>51/</u>	$t_h(CKXH-FXL)$	See figure 36	T-2	T+3			ns
2	Delay time, FSX low to CLKX low <u>52/</u>	$t_d(FXL-CKXL)$		H-2	H+3			
3	Delay time, CLKX low to DX valid	$t_d(CKXL-DXV)$		-2	4	12P+2.8	20P+17	
6	Disable time, DX high impedance following last data bit for CLKX high	$t_{dis}(CKXH-DXHZ)$		H-2	H+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis}(FXH-DXHZ)$				4P+3	12P+17	
8	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$				8P+2	16P+17	

Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 12/ 50/

4	Setup time, DR valid before CLKX high	$t_{su}(DRV-CKXH)$	See figure 36	12		2-12P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		5+24P		

Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 12/ 50/

1	Hold time, FSX low after CLKX high <u>51/</u>	$t_h(CKXH-FXL)$	See figure 36	H-2	H+3			ns
2	Delay time, FSX low to CLKX low <u>52/</u>	$t_d(FXL-CKXL)$		T-2	T+1			
3	Delay time, CLKX high to DX valid	$t_d(CKXH-DXV)$		-2	4	12P+2.8	20P+17	
6	Disable time, DX high impedance following last data bit for CLKX high	$t_{dis}(CKXH-DXHZ)$		-2	4	12P+3	20P+17	
7	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$		L-2	L+4	8P+2	16P+17	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit
				Min	Max	
UTOPIA SLAVE TIMING [C6415 AND 6416 ONLY]						
Timing requirements for UXCLK 7/						
1	Cycle time, UXCLK	$t_c(\text{UXCK})$	See figure 37	20		ns
2	Pulse duration, UXCLK high	$t_w(\text{UXCKH})$		0.4 $t_c(\text{UXCK})$	0.6 $t_c(\text{UXCK})$	
3	Pulse duration, UXCLK low	$t_w(\text{UXCKL})$		0.4 $t_c(\text{UXCK})$	0.6 $t_c(\text{UXCK})$	
4	Transition time, UXCLK	$t_t(\text{UXCK})$			2	
Timing requirements for URCLK 7/						
1	Cycle time, URCLK	$t_c(\text{URCK})$	See figure 37	20		ns
2	Pulse duration, URCLK high	$t_w(\text{URCKH})$		0.4 $t_c(\text{URCK})$	0.6 $t_c(\text{URCK})$	
3	Pulse duration, URCLK low	$t_w(\text{URCKL})$		0.4 $t_c(\text{URCK})$	0.6 $t_c(\text{URCK})$	
4	Transition time, URCLK	$t_t(\text{URCK})$			2	
Timing requirements for UTOPIA Slave transmit						
2	Setup time, UXADDR valid before UXCLK high	$t_{su}(\text{UXAV-UXCH})$	See figure 38	4		ns
3	Hold time, UXADDR valid after UXCLK high	$t_h(\text{UXCH-UXAV})$		1		
8	Setup time, $\overline{\text{UXENB}}$ low before UXCLK high	$t_{su}(\text{UXENBL-UXCH})$		4		
9	Hold time, $\overline{\text{UXENB}}$ low after UXCLK high	$t_h(\text{UXCH-UXENBL})$		1		
Switching characteristics for UTOPIA Slave transmit						
1	Delay time, UXCLK high to UXDATA valid	$t_d(\text{UXCH-UXDV})$	See figure 38	3	12	ns
4	Delay time, UXCLK high to UXCLAV driven active value	$t_d(\text{UXCH-UXCLAV})$		3	12	
5	Delay time, UXCLK high to UXCLAV driven inactive low	$t_d(\text{UXCH-UXCLAVL})$		3	12	
6	Delay time, UXCLK high to UXCLAV going Hi-Z	$t_d(\text{UXCH-UXCLAVHZ})$		9	18.5	
7	Pulse duration (low), UXCLAV low to UXCLAV Hi-Z	$t_w(\text{UXCLAVL-UXCLAVHZ})$		3		
10	Delay time, UXCLK high to UXSOC valid	$t_d(\text{UXCH-UXSV})$		3	12	

See notes at end of table.8

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit		
				Min	Max			
UTOPIA SLAVE TIMING [C6415 AND 6416 ONLY] – CONTINUED								
Timing requirements for UTOPIA Slave receive								
1	Setup time, URDATA valid before URCLK high	$t_{su}(URDV-URCH)$	See figure 39	4		ns		
2	Hold time, URDATA valid after URCLK high	$t_h(URCH-URDV)$		1				
3	Setup time, URADDR valid before URCLK high	$t_{su}(URAV-URCH)$		4				
4	Hold time, URADDR valid after URCLK high	$t_h(URCH-URAV)$		1				
9	Setup time, \overline{URENB} low before URCLK high	$t_{su}(URENBL-URCH)$		4				
10	Hold time, \overline{URENB} low after URCLK high	$t_h(URCH-URENBL)$		1				
11	Setup time, URSOC high before URCLK high	$t_{su}(URSH-URCH)$		4				
12	Hold time, URSOC high after URCLK high	$t_h(URCH-URSH)$		1				
Switching characteristics for UTOPIA Slave receive								
5	Delay time, URCLK high to URCLAV driven active low	$t_d(URCH-URCLAV)$		See figure 39	3		12	ns
6	Delay time, URCLK high to URCLAV driven inactive low	$t_d(URCH-URCLAVL)$			3		12	
7	Delay time, URCLK high to URCLAV going Hi-Z	$t_d(URCH-URCLAVHZ)$			9		18.5	
8	Pulse duration (low), URCLAV low to URCLAV Hi-Z	$t_w(URCLAVL-URCLAVHZ)$	3					
Timer timing								
Timing requirements for time input 12/								
1	Pulse duration, TINP high	$t_w(TINPH)$	See figure 40	8P		ns		
2	Pulse duration, TINP low	$t_w(TINPL)$		8P				
Switching characteristics for timer outputs 12/								
3	Pulse duration, TOUT high	$t_w(TOUTH)$	See figure 40	8P-3		ns		
4	Pulse duration, TOUT low	$t_w(TOUTL)$		8P-3				

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1

No	Test	Symbol	Test condition At recommended operating ranges unless otherwise noted Device types: All	Limits		Unit
				Min	Max	
GENERAL PURPOSE INPUT/OUTPUT (GPIO) PORT TIMING						
Timing requirements for GPIO inputs <u>12/</u> <u>53/</u>						
1	Pulse duration, GPIx high	$t_{w(GPIH)}$	See figure 40	8P		ns
2	Pulse duration, GPIx low	$t_{w(GPIL)}$		8P		
Switching characteristics for GPIO outputs <u>12/</u>						
3	Pulse duration, GPOx high	$t_{w(GPOH)}$	See figure 40	24P-8 <u>54/</u>		ns
4	Pulse duration, GPOx low	$t_{w(GPOL)}$		24P-8 <u>54/</u>		
JTAG TEST PORT TIMING						
Timing requirements for JTAG test port						
1	Cycle time, TCK	$t_c(TCK)$	See figure 40	35		ns
3	Setup time, TDI/TMS/ \overline{TRST} valid before TCK high	$t_{su}(TDIV-TCKH)$		10		
4	Hold time, TDI/TMS/ \overline{TRST} valid after TCK high	$t_h(TCKH-TDIV)$		9		
Switching characteristics for JTAG test port						
2	Delay time, TCK low to TDO valid	$t_d(TCKL-TDOV)$	See figure 40	0	18	ns

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ These rated numbers are from peripheral component interconnection (PCI) specification. The DC specification and AC specification are defined in manufacturer data.
- 3/ Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
- 4/ PCI input leakage currents include Hi-Z output leakage for all bidirectional buffers with 3-state outputs.
- 5/ Measured with average activity (50% high/50% low power). The actual current draw is highly application dependent. For more details on core and I/O activity, refer to the manufacturer Power Consumption Summary application report.
- 6/ Product preview device.
- 7/ The reference points for the rise and fall transactions are measured at V_{IL} Max and V_{IH} Min.
- 8/ For more details on the PLL multiplier factor (x6, x12, x20), see the Clock PLL section from the manufacturer information data.
- 9/ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 50 MHz, use $C = 20$ ns.
- 10/ The reference points for the rise and fall transactions are measured at V_{OL} Max and V_{OH} Min.
- 11/ PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.
- 12/ $P = 1/\text{CPU clock frequency}$ in nanoseconds (ns). For example, when running parts at 500 MHz, use $P = 2$ ns.
- 13/ All device type in this drawing have two EMIFs (64 bit EMIFA and 16 bit EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
- 14/ E = the EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) period in ns for EMIFA or EMIFB.
- 15/ Minimum ECLKIN cycle times must be met, even when ECLKIN is generated by an internal clock source. Minimum ECLKIN times are based on internal logic speed; the maximum useable speed of the EMIF may be lower due to AC timing requirements. On the devices, 133 MHz operation is achievable if the requirements of the EMIF device speed section are met.
- 16/ EH is the high period of E (EMIF input clock period) in ns and EL is the low period of E (EMIF input clock period) in ns for EMIFA or EMIFB.
- 17/ This cycle to cycle jitter specification was measured with CPU/4 or CPU/6 as the source of the EMIF input clock.
- 18/ E = the EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) period in ns for EMIFA or EMIFB.
 N = the EMIF input clock divider; $N = 1, 2, \text{ or } 4$.
- 19/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = $2E$) to ensure setup and hold time is met.
- 20/ RS = read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.
- 21/ E = ECLKOUT1 period in ns for EMIFA or EMIFB.
- 22/ Select signals for EMIFA include: \overline{ACEx} , $\overline{ABE}[7:0]$, $\overline{AEA}[22:3]$, \overline{AAOE} ; and for EMIFA writes, include $\overline{AED}[63:0]$.
Select signals for EMIFB include: \overline{BCEx} , $\overline{BBE}[1:0]$, $\overline{BEA}[20:1]$, \overline{BAOE} ; and for EMIFB writes, include $\overline{BED}[15:0]$.
- 23/ All device type in this drawing have two EMIFs (64 bit EMIFA and 16 bit EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the programmable synchronous interface access signals are shown as generic (\overline{SADS} / \overline{SRE} , \overline{SOE} , and \overline{SWE}) instead of \overline{ASADS} / \overline{ASRE} , \overline{ASOE} , and \overline{ASWE} (for EMIFA) and \overline{BSADS} / \overline{BSRE} , \overline{BSOE} , and \overline{BSWE} (for EMIFB)].

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TABLE I. Electrical performance characteristics - Continued.

- 24/ The following parameters are programmable via the EMIF CE Space Secondary Control register (CExSEC):
- Read latency (SYNCRL):0-, 1-, 2-, or 3-cycle read latency
 - Write latency (SYNCWL):0-, 1-, 2-, or 3-cycle write latency
 - $\overline{\text{CEx}}$ assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{CEx}}$ goes inactive after final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, $\overline{\text{CEx}}$ is active when $\overline{\text{SOE}}$ is active (CEEXT = 1)
 - Function of $\overline{\text{SADS}}/\overline{\text{SRE}}$ (RENEN): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{SADS}}/\overline{\text{SRE}}$ acts as $\overline{\text{SADS}}$ with deselect cycles (RENEN = 0). For FIFO interface, $\overline{\text{SADS}}/\overline{\text{SRE}}$ acts as $\overline{\text{SRE}}$ with NO deselect cycles (RENEN = 1).
 - Synchronization clock (SNCKLK): Synchronized to ECLKOUT1 or ECLKOUT2.
- 25/ All device type in this drawing have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, the prefix "A" or "B" may be omitted [e.g., the synchronous DRAM memory access signals are shown as generic ($\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$) instead of $\overline{\text{ASDCAS}}$, $\overline{\text{ASDWE}}$, and $\overline{\text{ASDRAS}}$ (for EMIFA) and $\overline{\text{BSDCAS}}$, $\overline{\text{BSDWE}}$, and $\overline{\text{BSDRAS}}$ (for EMIFB).
- 26/ E = the EMIF input clock (ECLKIN, CPU/4 clock, or CPU/6 clock) period in ns for EMIFA or EMIFB.
- 27/ For EMIFA, EMIF bus consists of: $\overline{\text{ACE}}[3:0]$, $\overline{\text{ABE}}[7:0]$, $\overline{\text{AED}}[63:0]$, $\overline{\text{AEA}}[22:3]$, $\overline{\text{AARE}}/\overline{\text{ASDCAS}}/\overline{\text{ASADS}}/\overline{\text{ASRE}}$, $\overline{\text{AAOE}}/\overline{\text{ASDRAS}}/\overline{\text{ASOE}}$, and $\overline{\text{AAWE}}/\overline{\text{ASDWE}}/\overline{\text{ASWE}}$, $\overline{\text{ASDCKE}}$, $\overline{\text{ASOE}}$, and $\overline{\text{ADPT}}$.
- For EMIFB, EMIF bus consists of: $\overline{\text{BCE}}[3:0]$, $\overline{\text{BBE}}[1:0]$, $\overline{\text{BED}}[15:0]$, $\overline{\text{BEA}}[20:1]$, $\overline{\text{BARE}}/\overline{\text{BSDCAS}}/\overline{\text{BSADS}}/\overline{\text{BSRE}}$, $\overline{\text{BAOE}}/\overline{\text{BSDRAS}}/\overline{\text{BSOE}}$, and $\overline{\text{BAWE}}/\overline{\text{BSDWE}}/\overline{\text{BSWE}}$, $\overline{\text{BSOE}}$, and $\overline{\text{BDPT}}$.
- 28/ The EKxHZ bits in EMIF Global Control register (GBLCTL) determine the state of the ECLKOUTx signals during $\overline{\text{HOLDA}}$. If EKxHZ = 0, ECLKOUTx continues clocking during Hold mode. If EKxHZ = 1, ECLKOUTx goes to high impedance during Hold mode, as shown in figure 22.
- 29/ All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.
- 30/ This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x6, x12, x20 when CLKIN and PLL are stable.
- 31/ This parameter applies to CLKMODE x6, x12, x20 only (it does not apply to CLKMODE x1). The $\overline{\text{RESET}}$ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 μs to stabilize following device power up or after PLL configuration has been changed. During that time, $\overline{\text{RESET}}$ must be asserted to ensure proper device operation. See manufacturer the clock PLL section for PLL clock time.
- 32/ EMIFB address pins BEA[20:13, 11, 9:7] are the boot configuration pins during device reset.
- 33/ E = 1/AECLKIN clock frequency in ns. C = 1/CLKIN clock frequency in ns. Select whichever value is larger for MIN parameter.
- 34/ N = the PCI input clock (PCLK) period in ns. When PCI is enabled (PCI_EN = 1), this parameter must be met.

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TABLE I. Electrical performance characteristics - Continued.

- 35/ EMIF Z group consists of: $\overline{AEA[22:3]}$, $\overline{BEA[20:1]}$, $\overline{AED[63:0]}$, $\overline{BED[15:0]}$, $\overline{CE[3:0]}$, $\overline{ABE[7:0]}$, $\overline{BBE[1:0]}$, \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} , $\overline{SOE3}$, \overline{ASDCKE} , and \overline{DPT} .
- EMIF high group consists of: \overline{AHOLDA} and \overline{BHOLDA} (when the corresponding \overline{HOLD} input is high)
- EMIF low group consists of: $\overline{ABUSREQ}$ and $\overline{BBUSREQ}$; \overline{AHOLDA} and \overline{BHOLDA} (when the corresponding \overline{HOLD} input is low)
- Low group consists of: $\overline{XSP_CS}$, $\overline{CLKX2/XSP_CLK}$, and $\overline{DX2/XSP_DO}$; all of which apply only when PCI EEPROM (BEA13) is enabled (with $\overline{PCI_EN} = 1$ and $\overline{MCBSP2_EN} = 0$). Otherwise, the $\overline{CLKX2/XSP_DO}$ pins are in the Z group. For more details on the PCI configuration pins, see the device configurations section from the manufacturer data sheet.
- Z group consists of: $\overline{HD[31:0]/AD[31:0]}$, $\overline{CLKX0}$, $\overline{CLKX1/URADDR4}$, $\overline{CLKX2/XSP_CLK}$, $\overline{FSX0}$, $\overline{FSX1/UXADDR3}$, $\overline{FSX2}$, $\overline{DX0}$, $\overline{DX1/UXADDR4}$, $\overline{DX2/XSP_DO}$, $\overline{CLKR0}$, $\overline{CLKR1/URADDR2}$, $\overline{CLKR2}$, $\overline{FSR0}$, $\overline{FSR1/UXADDR2}$, $\overline{FSR2}$, $\overline{TOUT0}$, $\overline{TOUT1}$, $\overline{TOUT2}$, $\overline{GP[8:0]}$, $\overline{GP10/PCBE3}$, $\overline{HR/\overline{W}/PCBE2}$, $\overline{HDS2/PCBE1}$, $\overline{PCBE0}$, $\overline{GP13/PINTA}$, $\overline{GP11/PREQ}$, $\overline{HDS1/PSERR}$, $\overline{HCS/PPERR}$, $\overline{HCNTL1/PDEVSEL}$, $\overline{HAS/PPAR}$, $\overline{HCNTL0/PSTOP}$, $\overline{HHWIL/PTRDY}$ (16 bit HPI mode only), $\overline{HRDY/PIRDY}$, $\overline{HINT/PFRAME}$, $\overline{UXDATA[7:0]}$, \overline{UXSOC} , \overline{UXCLAV} , and \overline{URCLAV} .
- 36/ $\overline{HSTROBE}$ refers to the following logical operation on \overline{HCS} , $\overline{HDS1}$, and $\overline{HDS2}$: $[\overline{NOT}(\overline{HDS1} \text{ XOR } \overline{HDS2})] \text{ OR } \overline{HCS}$.
- 37/ Select signals include: $\overline{HCNTL[1:0]}$ and $\overline{HR/\overline{W}}$. For HPI16 mode only, select signals also include \overline{HHWIL} .
- 38/ Select the parameter value of 4P or 12.5 ns, whichever is greater.
- 39/ This parameter is used during HPID read and writes. For reads, at the beginning of a word transfer (HPI32) or the first half word transfer (HPI16) on the falling edge of $\overline{HSTROBE}$, the HPI sends the request to the EDMA internal address generation hardware, and \overline{HRDY} remain high until the EDMA internal address generation hardware loads the requested data into HPID. For writes, \overline{HRDY} goes high if the internal write buffer is full.
- 40/ For 3.3 V operation, the reference points for the rise and fall transactions are measured at $V_{L \text{ Max}}$ and $V_{IHP \text{ Min}}$.
- 41/ Select parameter value of 30 ns or 8P, whichever is greater.
- 42/ $\overline{CLKRP} = \overline{CLKXP} = \overline{FSRP} = \overline{FSXP} = 0$. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- 43/ Use whichever value is greater.
- 44/ Minimum $\overline{CLKR/X}$ cycle times must be met, even when $\overline{CLKR/X}$ is generated by an internal clock source. Minimum $\overline{CLKR/X}$ cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
- 45/ This parameter applies to the maximum McBSP frequency. Operate serial clock ($\overline{CLKR/X}$) in the resonance range of 40/60 duty cycle.
- 46/ minimum delay times also represent minimum output hold times.
- 47/ C = H or L
 S = Sample rate generator input clock = 4P if $\overline{CLKSM} = 1$ (P = 1/CPU clock frequency)
 = Sample rate generator input clock = P_clks if $\overline{CLKSM} = 0$ (P_clks = CLK period)
 T = CLKX period = $(1 + \overline{CLKGDV}) * S$
 H = CLKX high pulse width = $(\overline{CLKGDV}/2 + 1) * S$ if \overline{CLKGDV} is even
 = $(\overline{CLKGDV} + 1)/2 * S$ if \overline{CLKGDV} is odd or zero
 L = CLKX low pulse width = $(\overline{CLKGDV}/2) * S$ if \overline{CLKGDV} is even
 = $(\overline{CLKGDV} + 1)/2 * S$ if \overline{CLKGDV} is odd or zero
 CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see 40/ above).

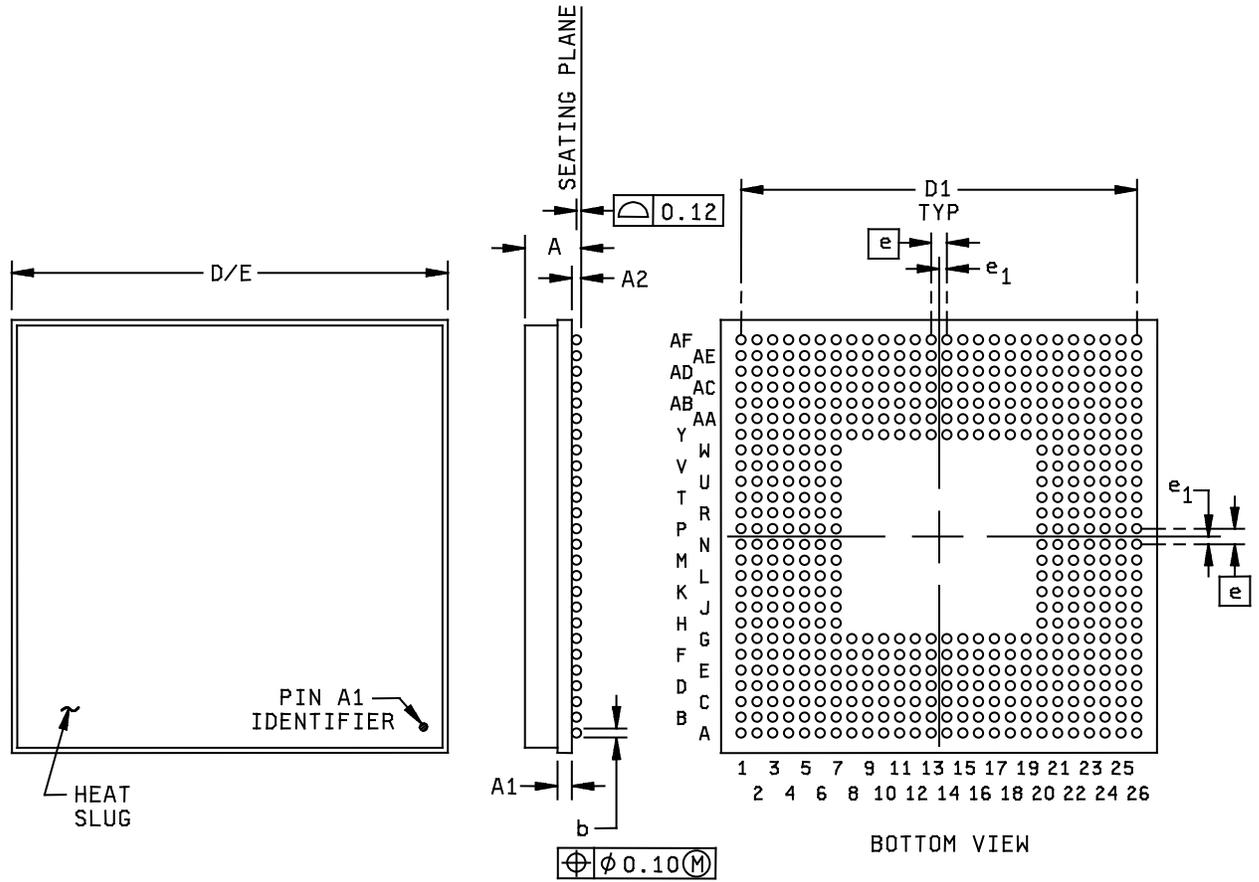
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TABLE I. Electrical performance characteristics - Continued.

- 48/ Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
 If DXENA = 0, then D1 = D2 = 0
 If DXENA = 1, then D1 = 4P, D2 = 8P
- 49/ Extra delay from FSX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
 If DXENA = 0, then D1 = D2 = 0
 If DXENA = 1, then D1 = 4P, D2 = 8P
- 50/ For all SPI Slave mode, CLKG is programmed as ¼ of the CPU clock by setting CLKSM = CLKGDV = 1
- 51/ FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active low slave enable output. As a Slave, the active low signal input on FSX and FSR is inverted before being used internally.
 CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP
 CLKXM = CLKRM = FSXM = FSRM = 0 for Slave McBSP
- 52/ FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).
- 53/ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have DSP recognize the GPIx changes through software polling of the HGPIO register, the GPIx duration must be extended to at least 12P to allow DSP enough time to access the GPIO register through CFGBUS.
- 54/ This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.

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Case X



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		3.30		.130	D/E	22.90	23.10	.902	.909
A1	1.00 Nom		.039 Nom		D1/E1	20.00 Typ		.787 Typ	
A2	0.35	0.45	.014	.018	e	0.80 Typ		.031 Typ	
b	0.45	0.55	.018	.022	e1	0.40 Typ		.016 Typ	

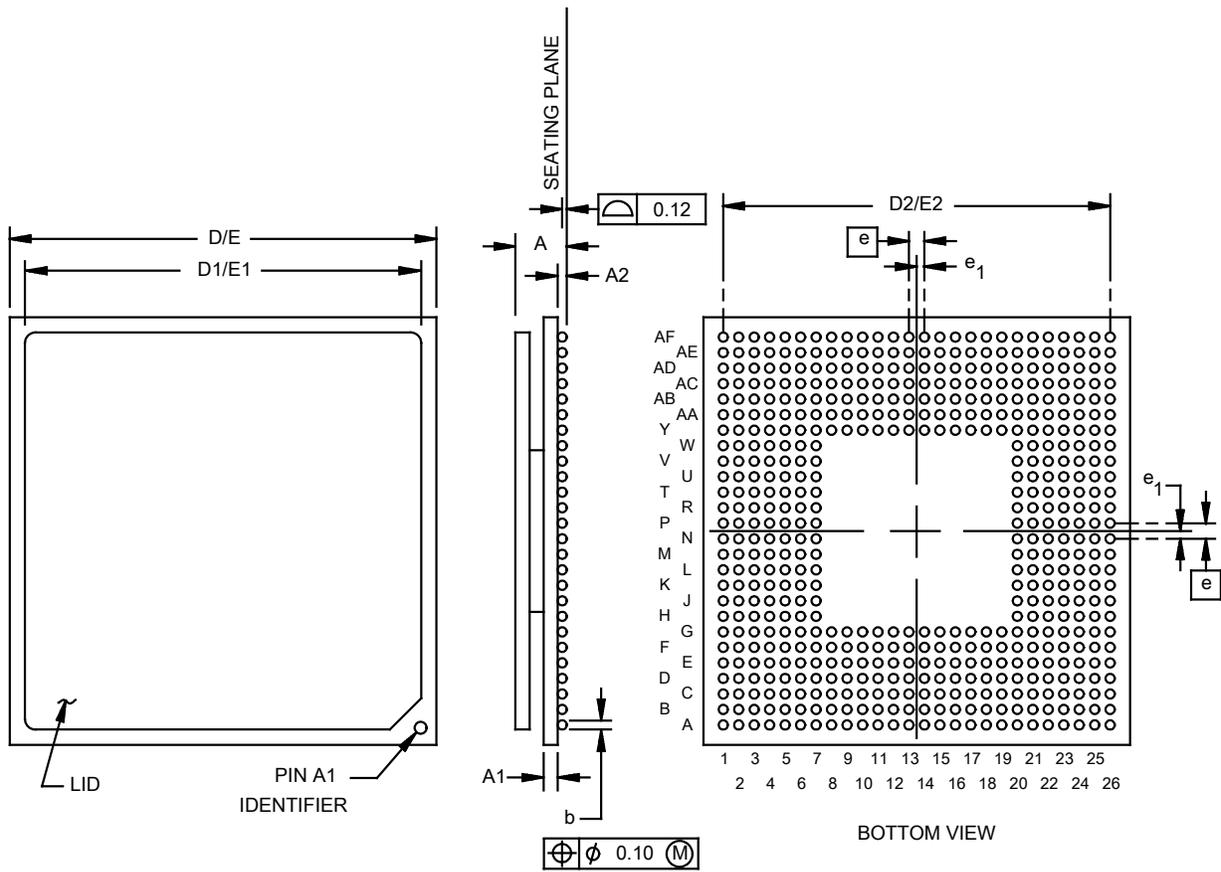
Notes:

1. This drawing is subject to change without notice.
2. Thermally enhanced plastic package with heat slug (HSL).
3. Flip chip application only.

FIGURE 1. Case outline.

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Case Y



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		3.25	D1/E1	20.90	21.10
A1	1.08 NOM		D2/E2	20.00 TYP	
A2	0.35	0.45	e	0.80 BSC	
b	0.45	0.55	e1	0.40 BSC	
D/E	22.90	23.10			

Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Thermally enhanced plastic package with a lead.
4. Flip chip application only.

FIGURE 1. Case outline - Continued.

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Case X and Y

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
A1	CV _{DD}	B1	DV _{DD}	C1	FSR0	D1	CLKR0	E1	CLKX0
A2	DV _{DD}	B2	CV _{DD}	C2	V _{SS}	D2	DR0	E2	DX0
A3	RSV	B3	V _{SS}	C3	CV _{DD}	D3	V _{SS}	E3	FSX0
A4	TOUT2	B4	NMI	C4	V _{SS}	D4	CV _{DD}	E4	V _{SS}
A5	TINP1	B5	TOUT1	C5	TINP2	D5	V _{SS}	E5	CV _{DD}
A6	BED12	B6	BED14	C6	TINP0	D6	TOUT0	E6	V _{SS}
A7	BED8	B7	BED10	C7	BED13	D7	BED15	E7	DV _{DD}
A8	V _{SS}	B8	BED6	C8	BED9	D8	BED11	E8	DV _{DD}
A9	BED2	B9	BED4	C9	BED7	D9	BED5	E9	V _{SS}
A10	$\overline{\text{BARE}}$ / $\overline{\text{BSDCAS}}$ / $\overline{\text{BSADS}} / \overline{\text{BSRE}}$	B10	BED0	C10	BED3	D10	BED1	E10	DV _{DD}
A11	BECLKIN	B11	$\overline{\text{BAOE}}$ / $\overline{\text{BSDRAS}}$ / $\overline{\text{BSOE}}$	C11	$\overline{\text{BAWE}}$ / $\overline{\text{BSDWE}}$ / $\overline{\text{BSWE}}$	D11	BECLKOUT2	E11	BARDY
A12	$\overline{\text{BCE0}}$	B12	$\overline{\text{BCE1}}$	C12	$\overline{\text{BCE2}}$	D12	BECLKOUT1	E12	$\overline{\text{BPDT}}$
A13	$\overline{\text{BCE3}}$	B13	V _{SS}	C13	$\overline{\text{BBE0}}$	D13	$\overline{\text{BBE1}}$	E13	$\overline{\text{BHOLDA}}$
A14	BEA1	B14	DV _{DD}	C14	BEA2	D14	BEA3	E14	BBUSREQ
A15	BEA4	B15	BEA5	C15	BEA6	D15	BEA7	E15	$\overline{\text{BSOE3}}$
A16	BEA8	B16	BEA9	C16	BEA10	D16	BEA11	E16	BEA20
A17	BEA12	B17	BEA13	C17	BEA14	D17	BEA15	E17	DV _{DD}
A18	BEA16	B18	BEA17	C18	BEA18	D18	BEA19	E18	V _{SS}
A19	V _{SS}	B19	$\overline{\text{BHOLD}}$	C19	AED15	D19	AED14	E19	DV _{DD}
A20	AED13	B20	AED11	C20	AED10	D20	AED12	E20	DV _{DD}
A21	AED9	B21	AED7	C21	AED6	D21	AED8	E21	V _{SS}
A22	AED5	B22	AED3	C22	AED4	D22	V _{SS}	E22	CV _{DD}
A23	AED1	B23	AED2	C23	V _{SS}	D23	CV _{DD}	E23	V _{SS}
A24	AED0	B24	V _{SS}	C24	CV _{DD}	D24	V _{SS}	E24	AED27
A25	DV _{DD}	B25	CV _{DD}	C25	V _{SS}	D25	AED29	E25	AED28
A26	CV _{DD}	B26	DV _{DD}	C26	AED31	D26	AED30	E26	AED26

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 28

Case X and Y – Continued.

Pin No.	Signal name								
F1	GP11/PREQ	G1	CLKMODE1	Y1	HD5/AD5	AA1	HD1/AD1	AB1	CLKR2
F2	GP14/PCLK	G2	RSV	Y2	HD3/AD3	AA2	DX2/XSP_D0	AB2	FSX2
F3	DV _{DD}	G3	GP15/PRST	Y3	HD4/AD4	AA3	HD0/AD0	AB3	DR2/XSP_DI
F4	CLKS0	G4	GP13/PINTA	Y4	HD2/AD2	AA4	PCI_EN	AB4	V _{SS}
F5	V _{SS}	G5	DV _{DD}	Y5	DV _{DD}	AA5	V _{SS}	AB5	CV _{DD}
F6	CV _{DD}	G6	CV _{DD}	Y6	CV _{DD}	AA6	CV _{DD}	AB6	V _{SS}
F7	CV _{DD}	G7	CV _{DD}	Y7	CV _{DD}	AA7	CV _{DD}	AB7	DV _{DD}
F8	V _{SS}	G8	CV _{DD}	Y8	CV _{DD}	AA8	V _{SS}	AB8	DV _{DD}
F9	DV _{DD}	G9	V _{SS}	Y9	V _{SS}	AA9	DV _{DD}	AB9	V _{SS}
F10	V _{SS}	G10	CV _{DD}	Y10	CV _{DD}	AA10	V _{SS}	AB10	DV _{DD}
F11	V _{SS}	G11	CV _{DD}	Y11	CV _{DD}	AA11	V _{SS}	AB11	DX1/UXADDR4
F12	DV _{DD}	G12	V _{SS}	Y12	V _{SS}	AA12	DV _{DD}	AB12	CLKX1/URADDR4
F13	V _{SS}	G13	CV _{DD}	Y13	RSV	AA13	V _{SS}	AB13	FSX1/UXADDR3
F14	V _{SS}	G14	RSV	Y14	CV _{DD}	AA14	V _{SS}	AB14	URSOC
F15	DV _{DD}	G15	V _{SS}	Y15	V _{SS}	AA15	DV _{DD}	AB15	TRST
F16	V _{SS}	G16	CV _{DD}	Y16	CV _{DD}	AA16	V _{SS}	AB16	TMS
F17	V _{SS}	G17	CV _{DD}	Y17	CV _{DD}	AA17	V _{SS}	AB17	DV _{DD}
F18	DV _{DD}	G18	V _{SS}	Y18	V _{SS}	AA18	DV _{DD}	AB18	V _{SS}
F19	V _{SS}	G19	CV _{DD}	Y19	CV _{DD}	AA19	V _{SS}	AB19	DV _{DD}
F20	CV _{DD}	G20	CV _{DD}	Y20	CV _{DD}	AA20	CV _{DD}	AB20	DV _{DD}
F21	CV _{DD}	G21	CV _{DD}	Y21	CV _{DD}	AA21	CV _{DD}	AB21	V _{SS}
F22	V _{SS}	G22	DV _{DD}	Y22	DV _{DD}	AA22	V _{SS}	AB22	CV _{DD}
F23	AED23	G23	AED19	Y23	AED44	AA23	AED40	AB23	V _{SS}
F24	AED25	G24	AED21	Y24	AED42	AA24	AED38	AB24	AED36
F25	AED24	G25	AED20	Y25	AED43	AA25	AED39	AB25	AED35
F26	AED22	G26	AED18	Y26	AED45	AA26	AED41	AB26	AED37

FIGURE 2. Terminal connections - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 29

Case X and Y – Continued.

Pin No.	Signal name								
AC1	FSR2	AD1	XSP_CS	AE1	DV _{DD}	AF1	CV _{DD}	H1	V _{SS}
AC2	CLKX2/XSP_CLK	AD2	V _{SS}	AE2	CV _{DD}	AF2	DV _{DD}	H2	CLKMODE0
AC3	V _{SS}	AD3	CV _{DD}	AE3	V _{SS}	AF3	MCBSP2_EN	H3	RSV
AC4	CV _{DD}	AD4	V _{SS}	AE4	CLKS2/GP8	AF4	GP7/EXT_INT7	H4	CLKIN
AC5	V _{SS}	AD5	GP6/EXT_INT6	AE5	GP5/EXT_INT5	AF5	GP4/EXT_INT4	H5	DV _{DD}
AC6	GP3	AD6	CLKOUT6/GP2	AE6	CLKOUT4/GP1	AF6	GP0	H6	V _{SS}
AC7	RESET	AD7	UXDATA0	AE7	UXDATA1	AF7	UXDATA2	H7	RSV
AC8	CLKS1/URADDR3	AD8	UXDATA5	AE8	UXDATA4	AF8	V _{SS}	H20	CV _{DD}
AC9	FSR1/UXADDR2	AD9	UXDATA6	AE9	UXADDR0	AF9	UXDATA3	H21	V _{SS}
AC10	CLKR1/URADDR2	AD10	UXDATA7	AE10	URADDR0	AF10	URADDR1	H22	DV _{DD}
AC11	URDATA4	AD11	UXCLK	AE11	URDATA6	AF11	DR1/UXADDR1	H23	AED17
AC12	URDATA3	AD12	URCLK	AE12	URDATA2	AF12	URDATA7	H24	AED16
AC13	UXSOC	AD13	URDATA0	AE13	DV _{DD}	AF13	URDATA5	H25	AECLKIN
AC14	UXCLAV	AD14	URDATA1	AE14	V _{SS}	AF14	URCLAV	H26	V _{SS}
AC15	EMU1	AD15	URENB	AE15	UXENB	AF15	EMU0	J1	HD29/AD29
AC16	EMU4	AD16	EMU3	AE16	EMU2	AF16	TCK	J2	HD31/AD31
AC17	EMU8	AD17	EMU6	AE17	EMU5	AF17	EMU7	J3	GP12/P _{GN} T
AC18	EMU11	AD18	EMU10	AE18	EMU9	AF18	TDI	J4	RSV
AC19	AED49	AD19	AED48	AE19	TDO	AF19	V _{SS}	J5	V _{SS}
AC20	AED51	AD20	AED53	AE20	AED52	AF20	AED50	J6	PLLV
AC21	AED55	AD21	AED57	AE21	AED56	AF21	AED54	J7	V _{SS}
AC22	V _{SS}	AD22	AED59	AE22	AED60	AF22	AED58	J20	V _{SS}
AC23	CV _{DD}	AD23	V _{SS}	AE23	AED61	AF23	AED62	J21	DV _{DD}
AC24	V _{SS}	AD24	CV _{DD}	AE24	V _{SS}	AF24	AED63	J22	V _{SS}
AC25	AED33	AD25	V _{SS}	AE25	CV _{DD}	AF25	DV _{DD}	J23	AECLKOUT2
AC26	AED34	AD26	AED32	AE26	DV _{DD}	AF26	CV _{DD}	J24	A _{AOE} / A _{SDRAS} / A _{SOE}
								J25	A _{AARE} / A _{SDCAS} / A _{SDAS} / A _{SRE}
								J26	AECLKOUT1

FIGURE 2. Terminal connections - Continued.

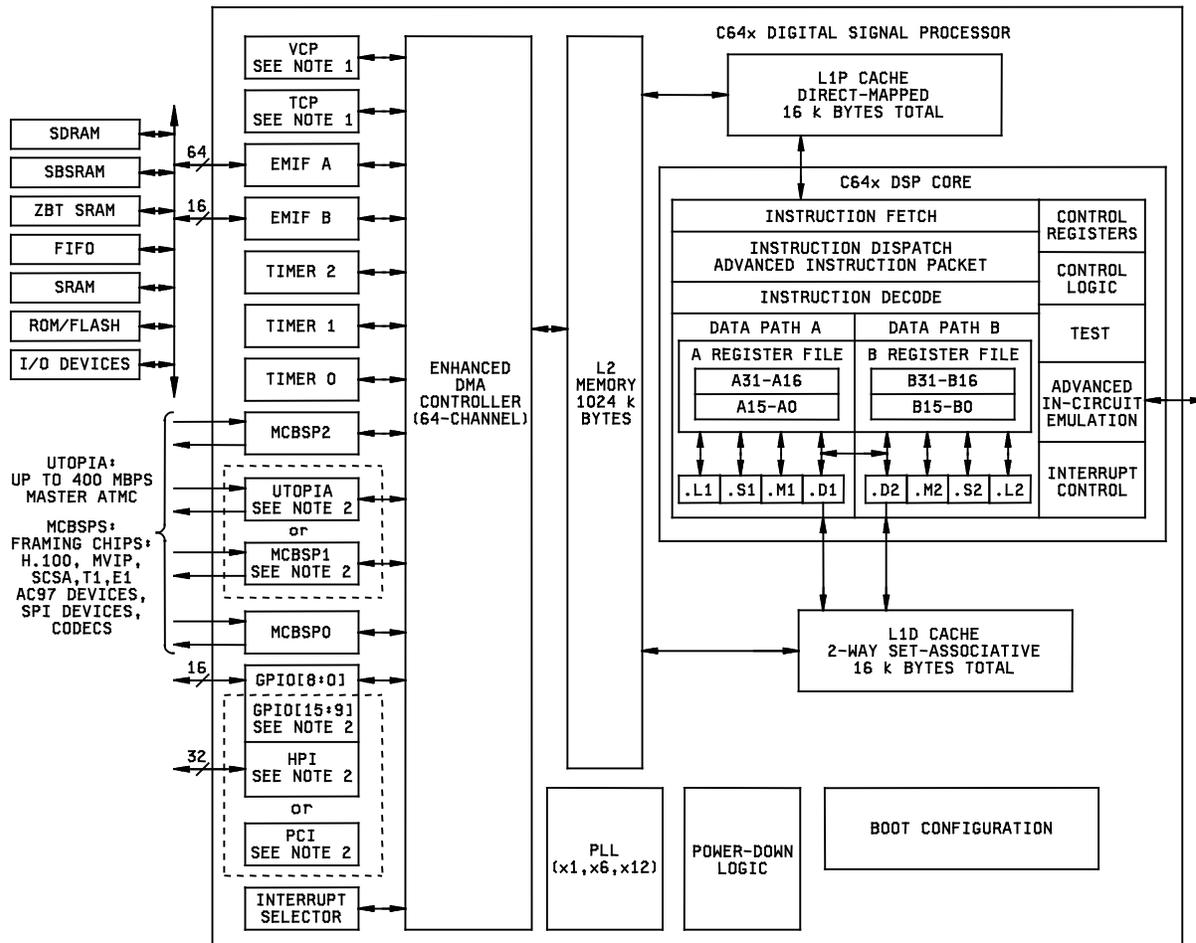
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 30

Case X and Y – Continued.

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
K1	HD25/AD25	M1	HD19/AD19	P1	HR/ \overline{W} / $\overline{PCBE2}$	T1	$\overline{HDS1/PSERR}$	V1	HD10/AD10
K2	HD27/AD27	M2	HD21/AD21	P2	V _{SS}	T2	$\overline{HDS2/PCBE1}$	V2	HD8/AD8
K3	HD30/AD30	M3	GP9/PIDSEL	P3	RSV	T3	$\overline{HAS/PPAR}$	V3	HD9/AD9
K4	HD28/AD28	M4	HD22/AD22	P4	\overline{HRDY} / \overline{PIRDY}	T4	$\overline{HCNTL0/}$ \overline{PSTOP}	V4	HD11/AD11
K5	DV _{DD}	M5	DV _{DD}	P5	HD16/AD16	T5	DV _{DD}	V5	V _{SS}
K6	RSV	M6	DV _{DD}	P6	V _{SS}	T6	V _{SS}	V6	DV _{DD}
K7	CV _{DD}	M7	V _{SS}	P7	RSV	T7	CV _{DD}	V7	V _{SS}
K20	CV _{DD}	M20	V _{SS}	P20	CV _{DD}	T20	CV _{DD}	V20	V _{SS}
K21	V _{SS}	M21	DV _{DD}	P21	V _{SS}	T21	V _{SS}	V21	DV _{DD}
K22	DV _{DD}	M22	\overline{APDT}	P22	ABUSREQ	T22	AEA22	V22	V _{SS}
K23	$\overline{ACE2}$	M23	AEA4	P23	AEA10	T23	$\overline{ABE7}$	V23	\overline{AHOLD}
K24	$\overline{ACE1}$	M24	AEA3	P24	AEA9	T24	$\overline{ABE6}$	V24	AEA21
K25	$\overline{ACE0}$	M25	$\overline{ABE3}$	P25	DV _{DD}	T25	AEA14	V25	AEA20
K26	\overline{AAWE} / \overline{ASDWE} / \overline{ASWE}	M26	$\overline{ABE2}$	P26	AEA8	T26	AEA13	V26	AEA19
L1	HD23/AD23	N1	HD17/AD17	R1	$\overline{HCNTL1/}$ $\overline{PDEVSEL}$	U1	HD14/AD14	W1	V _{SS}
L2	$\overline{GP10/PCBE3}$	N2	DV _{DD}	R2	$\overline{HCS/PPERR}$	U2	HD12/AD12	W2	HD7/AD7
L3	HD26/AD26	N3	RSV	R3	$\overline{HHWIL/}$ \overline{PTRDY}	U3	HD13/AD13	W3	$\overline{PCBE0}$
L4	HD24/AD24	N4	HD20/AD20	R4	\overline{HINT} / \overline{PFRAME}	U4	HD15/AD15	W4	HD6/AD6
L5	DV _{DD}	N5	HD18/AD18	R5	DV _{DD}	U5	DV _{DD}	W5	DV _{DD}
L6	V _{SS}	N6	V _{SS}	R6	RSV	U6	V _{SS}	W6	V _{SS}
L7	CV _{DD}	N7	CV _{DD}	R7	V _{SS}	U7	CV _{DD}	W7	CV _{DD}
L20	CV _{DD}	N20	RSV	R20	V _{SS}	U20	CV _{DD}	W20	CV _{DD}
L21	V _{SS}	N21	V _{SS}	R21	DV _{DD}	U21	V _{SS}	W21	V _{SS}
L22	AARDY	N22	\overline{AHOLDA}	R22	$\overline{ASOE3}$	U22	DV _{DD}	W22	DV _{DD}
L23	$\overline{ABE1}$	N23	AEA7	R23	AEA12	U23	AEA18	W23	AED46
L24	$\overline{ABE0}$	N24	AEA6	R24	AEA11	U24	AEA17	W24	AED47
L25	ASDCKE	N25	V _{SS}	R25	$\overline{ABE5}$	U25	AEA16	W25	RSV
L26	$\overline{ACE3}$	N26	AEA5	R26	$\overline{ABE4}$	U26	AEA15	W26	V _{SS}

FIGURE 2. Terminal connections - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 31

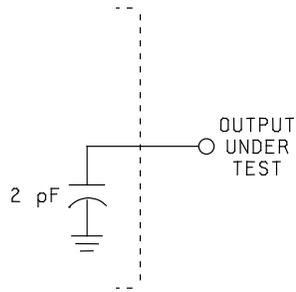


Notes:

1. VCP and TCP decoder coprocessors are applicable to the device type 3 only.
2. The UTOPIA peripheral is muxed with MCBSP1, and the PCI peripheral is MUXed with the HPI peripheral and the GPIO[15:9] port. For more details on the multiplexed pins of these peripherals, see manufacturer data sheet.

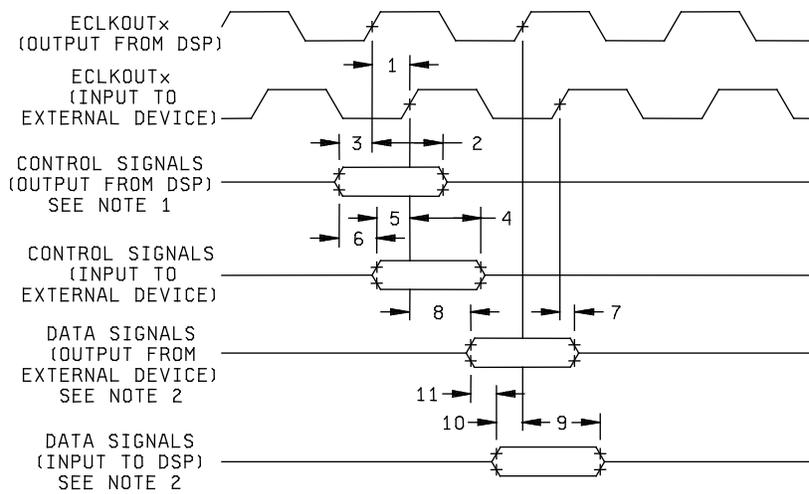
FIGURE 3. Block diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 32



AC TIMING REFERENCE CIRCUIT FOR AC TIMING MEASUREMENTS

FIGURE 4. Timing reference.



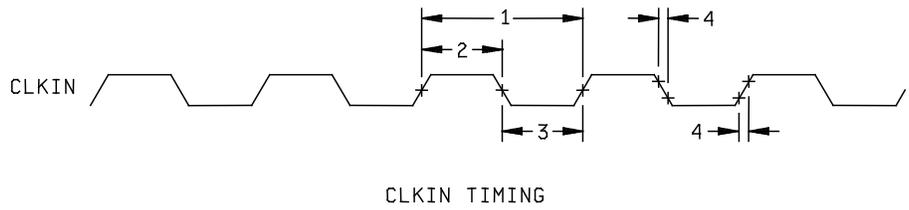
BOARD-LEVEL INPUT/OUTPUT TIMINGS

Notes:

1. Control signals include data for writes.
2. Data signals are generated during Reads from an external device.

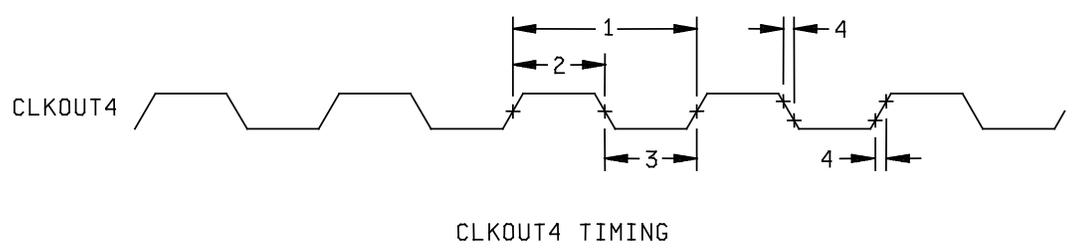
FIGURE 5. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 33</p>

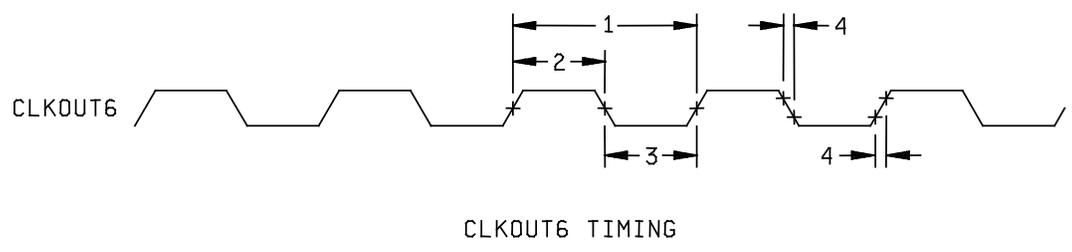


CLKIN TIMING

FIGURE 6. Timing waveforms.



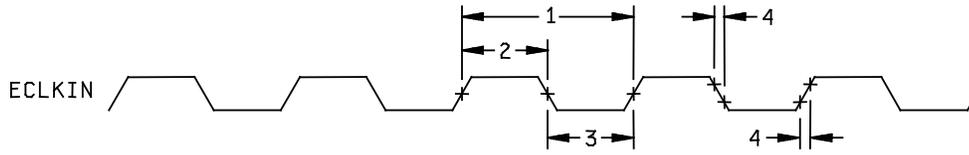
CLKOUT4 TIMING



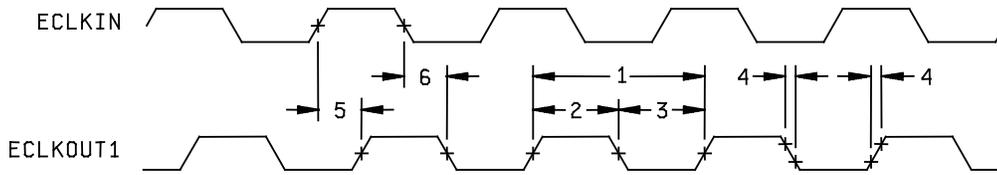
CLKOUT6 TIMING

FIGURE 7. Timing waveforms.

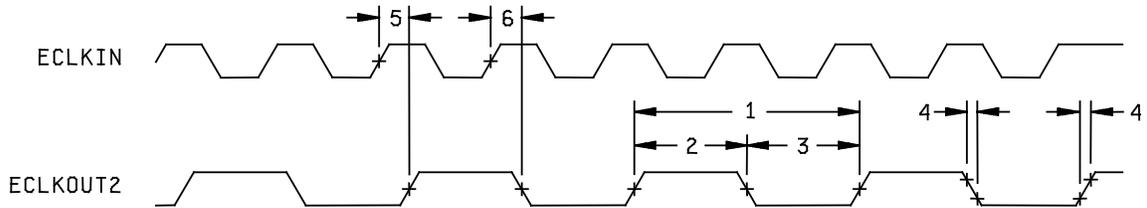
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 34</p>



ECLKIN TIMING FOR EMIFA AND EMIFB



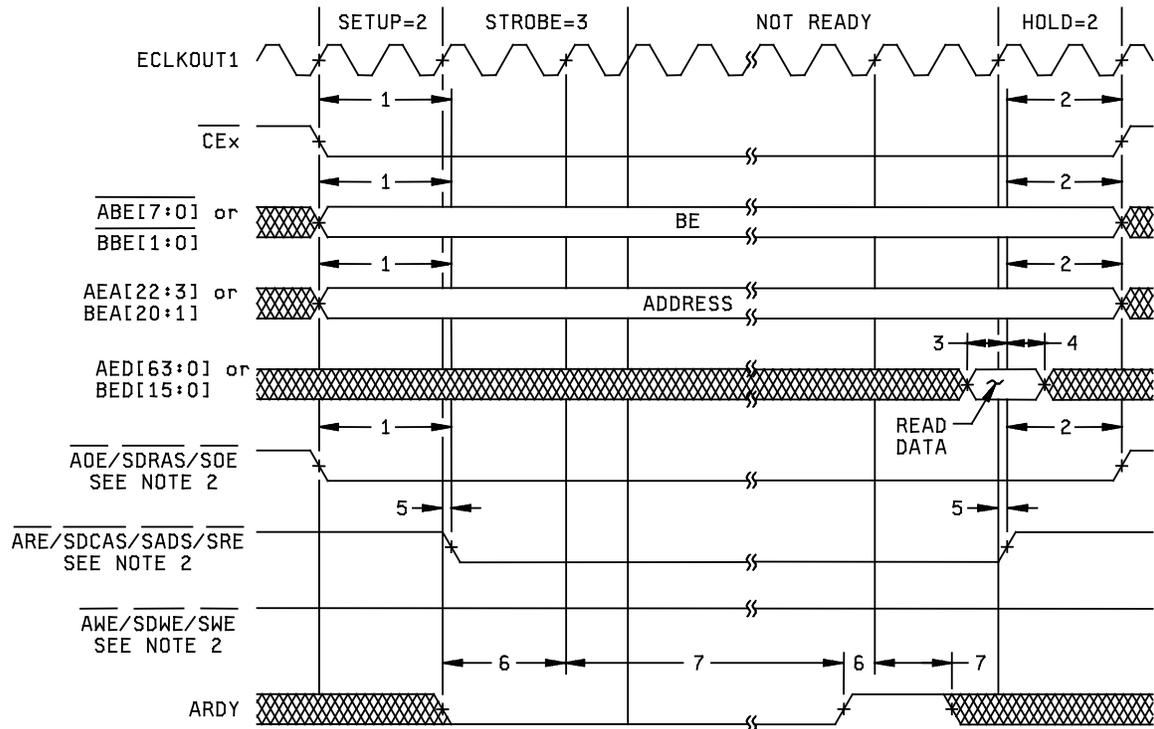
ECLKOUT1 TIMING FOR EMIFA AND EMIFB MODULES



ECLKOUT2 TIMING FOR EMIFA AND EMIFB MODULES

FIGURE 8. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 35</p>



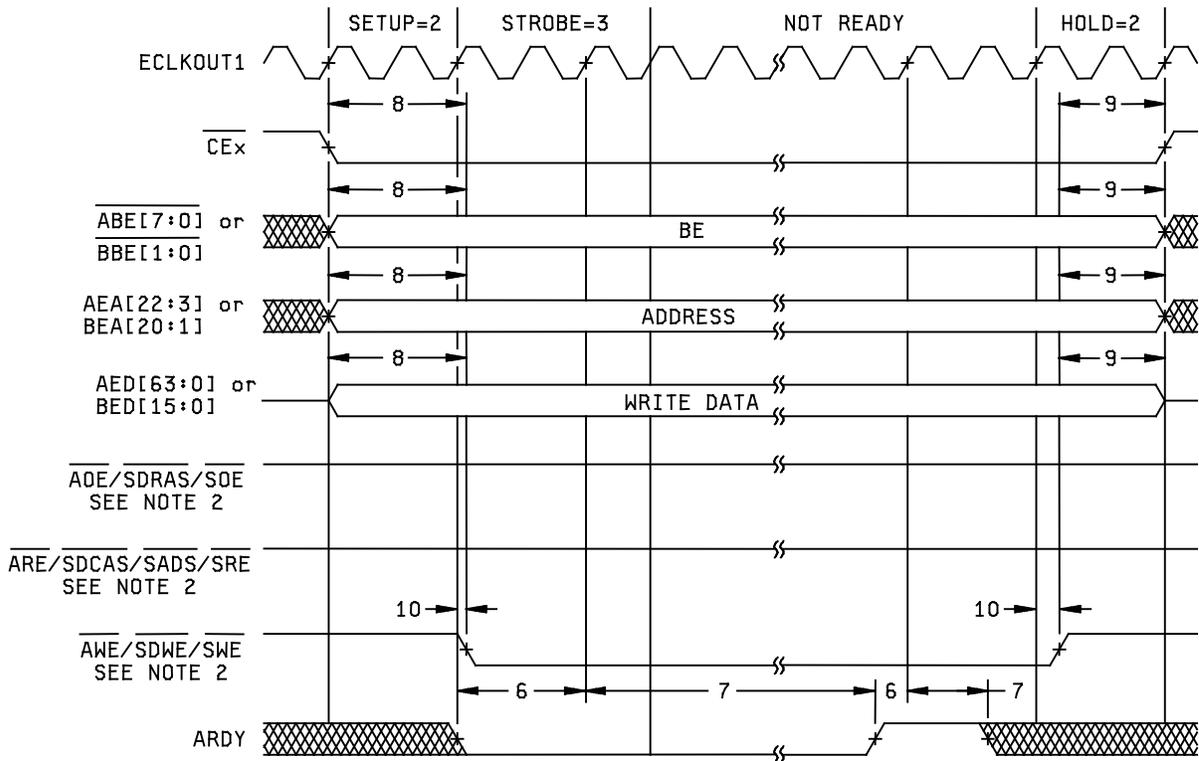
ASYNCHRONOUS MEMORY READ TIMING FOR EMIFA AND EMIFB
SEE NOTE 1

Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{AOE} / \overline{SDRAS} / \overline{SOE} , \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , and \overline{AWE} / \overline{SDWE} / \overline{SWE} operate as \overline{AOE} (identified under select signals), \overline{ARE} , and \overline{AWE} , respectively, during asynchronous memory accesses.

FIGURE 9. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 36



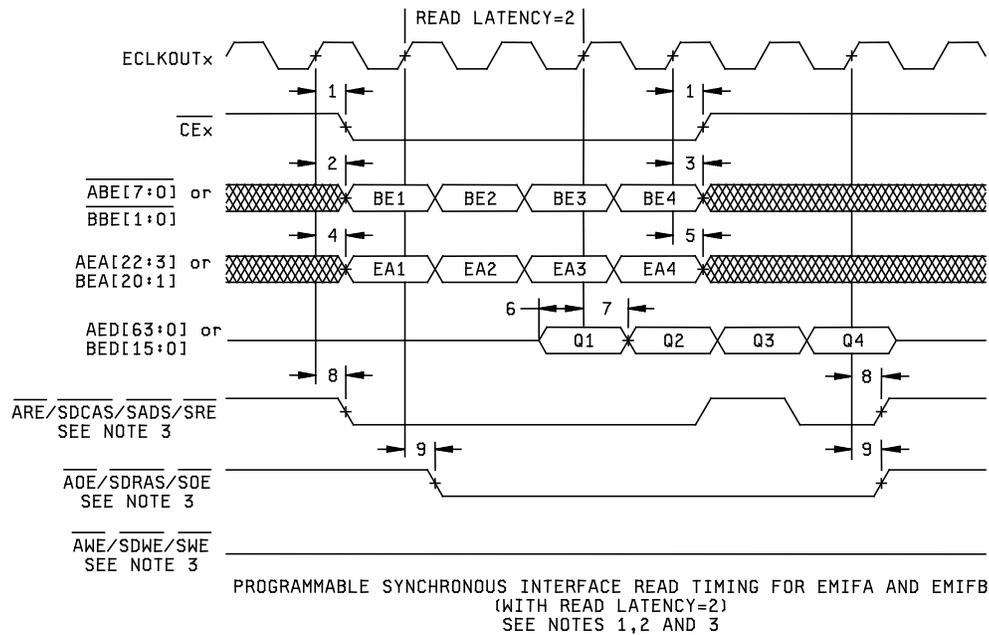
ASYNCHRONOUS MEMORY WRITE TIMING FOR EMIFA AND EMIFB
SEE NOTE 1

Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{AOE} / \overline{SDRAS} / \overline{SOE} , \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , and \overline{AWE} / \overline{SDWE} / \overline{SWE} operate as \overline{AOE} (identified under select signals), \overline{ARE} , and \overline{AWE} , respectively, during asynchronous memory accesses.

FIGURE 10. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 37

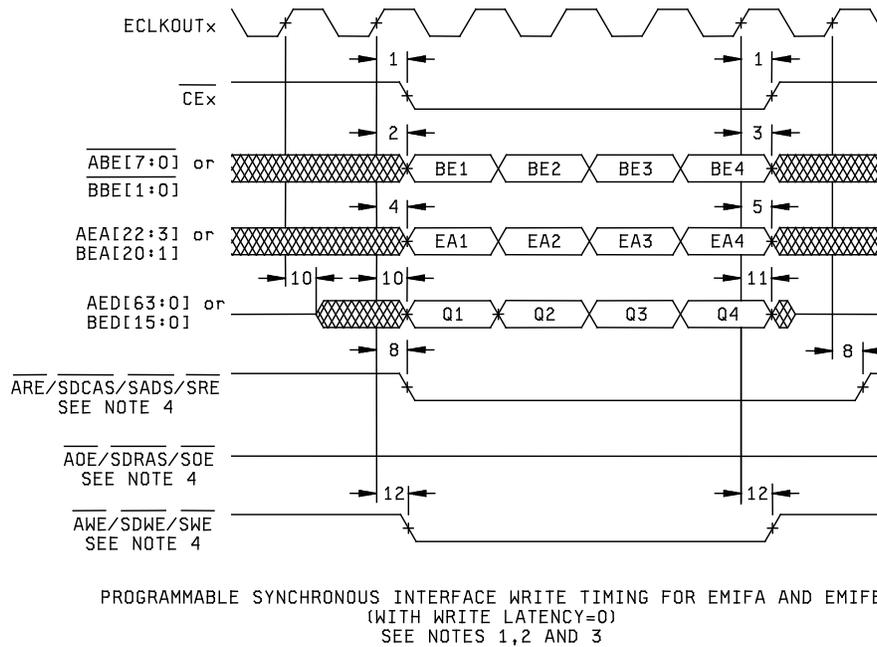


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. The read latency and the length of the \overline{CEx} assertion are programmable via the SYNCRL and CEEXT fields, respectively, in the EMIFxCE Space Secondary Control register (CEXSEC). In this figure, SYNCRL = 2 and CEEXT = 0.
3. The following parameters are programmable via the EMIF CE Space Secondary Control register (CEXSEC):
 - Read latency (SYNCRL): 0-, 1-, 2-, or 3-cycle read latency.
 - Write latency (SYNCWL): 0-, 1-, 2-, or 3-cycle write latency.
 - \overline{CEx} assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, \overline{CEx} goes inactive after the final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, \overline{CEx} is active when \overline{SOE} is active (CEEXT = 1).
 - Function of $\overline{SADS}/\overline{SRE}$ (RENEN): For standard SBSRAM or ZBT SRAM interface, $\overline{SADS}/\overline{SRE}$ acts as \overline{SADS} with deselect cycles (RENEN = 0). For FIFO interface, $\overline{SADS}/\overline{SRE}$ acts as \overline{SRE} with NO deselect cycles (RENEN = 1).
 - Synchronization clock (SNCKLK): Synchronized to ECLKOUT1 or ECLKOUT2.
4. $\overline{ARE}/\overline{SDCAS}/\overline{SADS}/\overline{SRE}$, $\overline{AOE}/\overline{SDRAS}/\overline{SOE}$, and $\overline{AWE}/\overline{SDWE}/\overline{SWE}$ operate as $\overline{SADS}/\overline{SRE}$, \overline{SOE} , and \overline{SWE} respectively, during synchronous interface accesses.

FIGURE 11. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 38

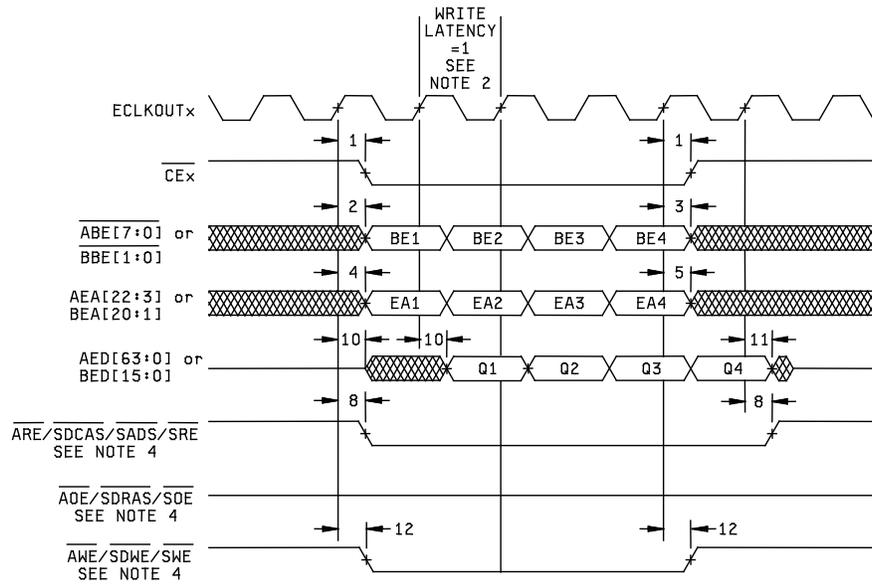


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. The write latency and the length of the \overline{CEx} assertion are programmable via the SYNCWL and CEEXT fields, respectively, in the EMIFxCE Space Secondary Control register (CEXSEC). In this figure, SYNCWL = 0 and CEEXT = 0.
3. The following parameters are programmable via the EMIF CE Space Secondary Control register (CEXSEC):
 - Read latency (SYNCRL): 0-, 1-, 2-, or 3-cycle read latency.
 - Write latency (SYNCWL): 0-, 1-, 2-, or 3-cycle write latency.
 - \overline{CEx} assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, \overline{CEx} goes inactive after the final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, \overline{CEx} is active when \overline{SOE} is active (CEEXT = 1).
 - Function of $\overline{SADS}/\overline{SRE}$ (RENEN): For standard SBSRAM or ZBT SRAM interface, $\overline{SADS}/\overline{SRE}$ acts as \overline{SADS} with deselect cycles (RENEN = 0). For FIFO interface, $\overline{SADS}/\overline{SRE}$ acts as \overline{SRE} with NO deselect cycles (RENEN = 1).
 - Synchronization clock (SNCKLK): Synchronized to ECLKOUT1 or ECLKOUT2.
4. $\overline{ARE}/\overline{SDCAS}/\overline{SADS}/\overline{SRE}$, $\overline{AOE}/\overline{SDRAS}/\overline{SOE}$, and $\overline{AWE}/\overline{SDWE}/\overline{SWE}$ operate as $\overline{SADS}/\overline{SRE}$, \overline{SOE} , and \overline{SWE} respectively, during synchronous interface accesses.

FIGURE 12. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 39



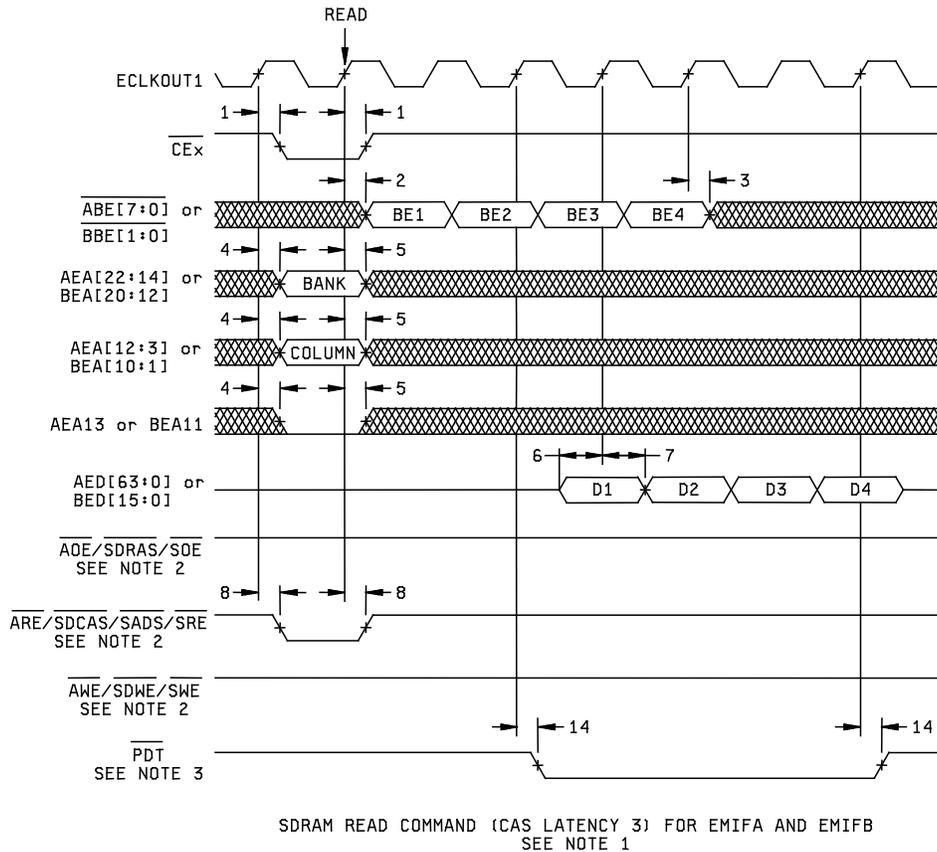
PROGRAMMABLE SYNCHRONOUS INTERFACE WRITE TIMING FOR EMIFA AND EMIFB
(WITH WRITE LATENCY=1)
SEE NOTES 1,2 AND 3

Notes:

- These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an “A” and all EMIFB signals are prefixed by a “B”. Throughout the rest of this document, in generic EMIF areas of discussion, prefix “A” or “B” may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
- The write latency and the length of the \overline{CEx} assertion are programmable via the SYNCWL and CEEXT fields, respectively, in the EMIFxCE Space Secondary Control register (CEXSEC). In this figure, SYNCWL = 1 and CEEXT = 0.
- The following parameters are programmable via the EMIF CE Space Secondary Control register (CEXSEC):
 - Read latency (SYNCR): 0-, 1-, 2-, or 3-cycle read latency.
 - Write latency (SYNCWL): 0-, 1-, 2-, or 3-cycle write latency.
 - \overline{CEx} assertion length (CEEXT): For standard SBSRAM or ZBT SRAM interface, \overline{CEx} goes inactive after the final command has been issued (CEEXT = 0). For synchronous FIFO interface with glue, \overline{CEx} is active when \overline{SOE} is active (CEEXT = 1).
 - Function of $\overline{SADS}/\overline{SRE}$ (RENEN): For standard SBSRAM or ZBT SRAM interface, $\overline{SADS}/\overline{SRE}$ acts as \overline{SADS} with deselect cycles (RENEN = 0). For FIFO interface, $\overline{SADS}/\overline{SRE}$ acts as \overline{SRE} with NO deselect cycles (RENEN = 1).
 - Synchronization clock (SNCLK): Synchronized to ECLKOUT1 or ECLKOUT2.
- $\overline{ARE}/\overline{SDCAS}/\overline{SADS}/\overline{SRE}$, $\overline{AOE}/\overline{SDRAS}/\overline{SOE}$, and $\overline{AWE}/\overline{SDWE}/\overline{SWE}$ operate as $\overline{SADS}/\overline{SRE}$, \overline{SOE} , and \overline{SWE} respectively, during synchronous interface accesses.

FIGURE 13. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 40

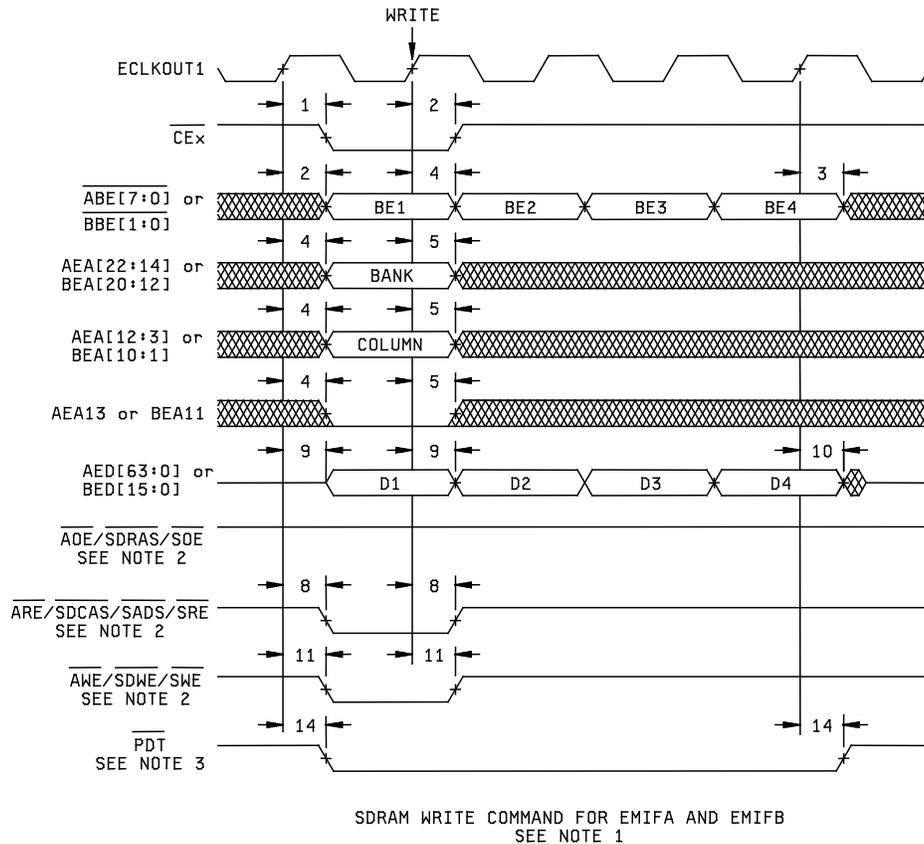


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} operate as \overline{SDCAS} / \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.
3. \overline{PDT} signal is only asserted when the EDMA is in PDT mode (set the PDTS bit to 1 in the EDMA options parameter RAM). For \overline{PDT} read. Data is not latched into EMIF. The PDTRL field in the PDT control register (PDTCTL) configures the latency of the \overline{PDT} signal with respect to the data phase of a read transaction. The latency of the \overline{PDT} signal for a read can be programmed to 0, 1, 2, or 3 by setting PDTRL to 00, 01, 10, or 11, respectively. PDTRL equals 00 (zero latency) in this figure.

FIGURE 14. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 41

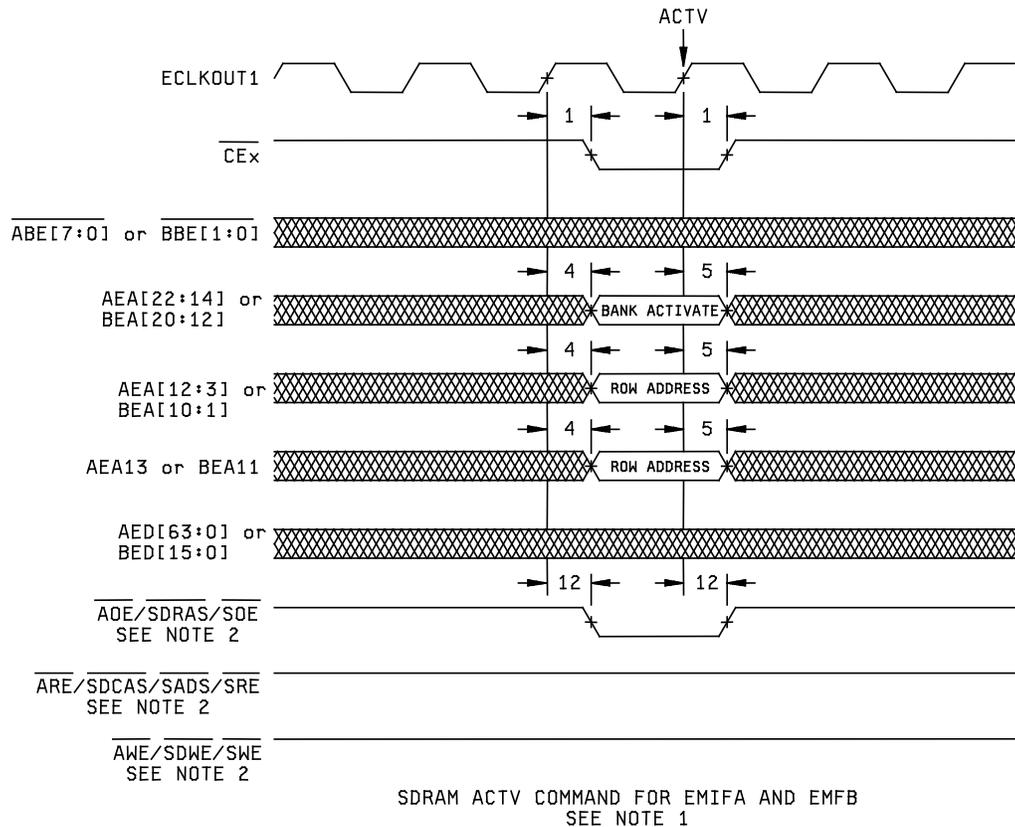


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. $\overline{ARE}/\overline{SDCAS}/\overline{SADS}/\overline{SRE}$, $\overline{AWE}/\overline{SDWE}/\overline{SWE}$, and $\overline{AOE}/\overline{SDRAS}/\overline{SOE}$ operate as $\overline{SDCAS}/\overline{SDWE}$, and \overline{SDRAS} respectively, during SDRAM accesses.
3. \overline{PDT} signal is only asserted when the EDMA is in PDT mode (set the PDTS bit to 1 in the EDMA options parameter RAM). For \overline{PDT} read. Data is not latched into EMIF. The PDTRL field in the PDT control register (PDTCTL) configures the latency of the \overline{PDT} signal with respect to the data phase of a read transaction. The latency of the \overline{PDT} signal for a read can be programmed to 0, 1, 2, or 3 by setting PDTRL to 00, 01, 10, or 11, respectively. PDTRL equals 00 (zero latency) in this figure.

FIGURE 15. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 42

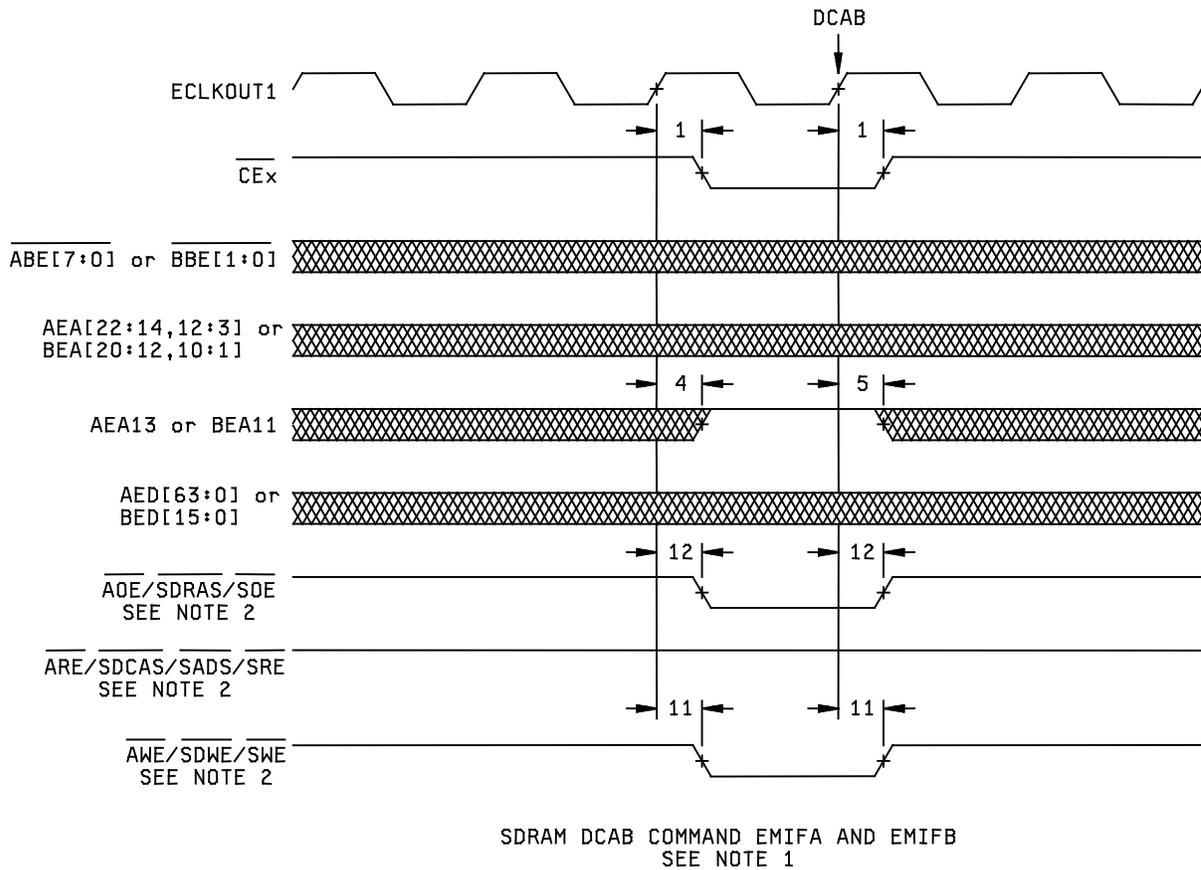


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} operate as \overline{SDCAS} / \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 16. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 43

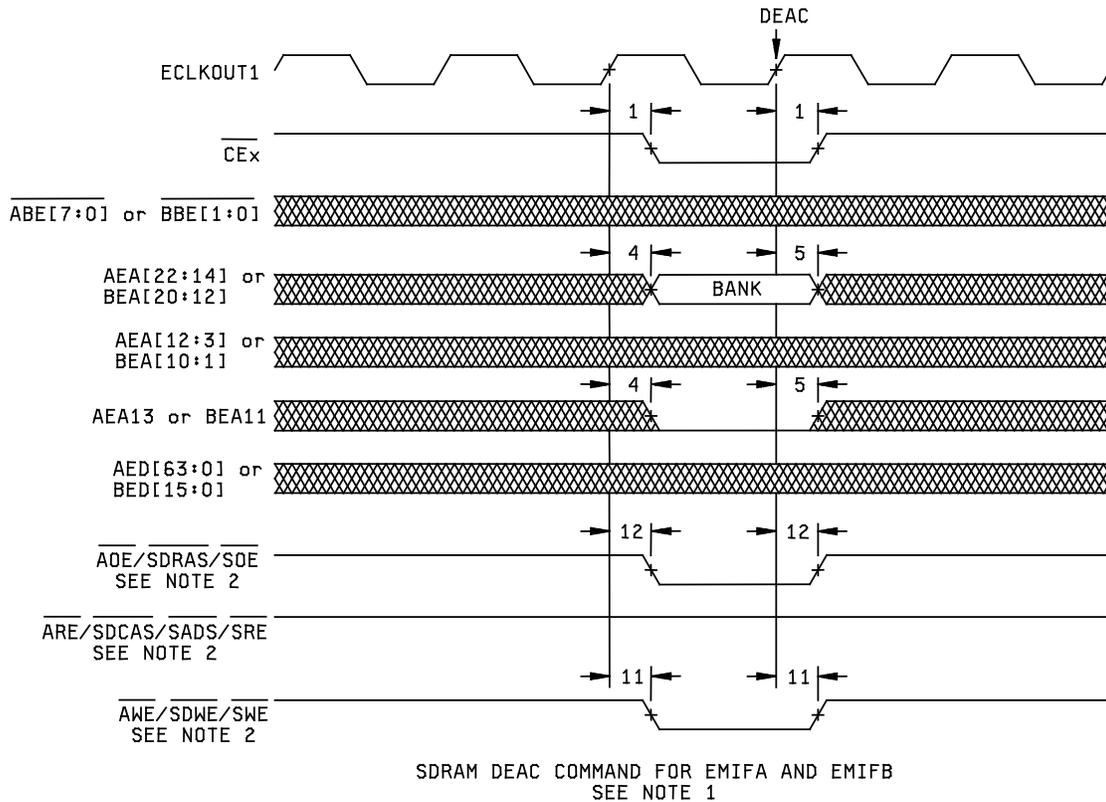


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} operate as \overline{SDCAS} / \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 17. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 44

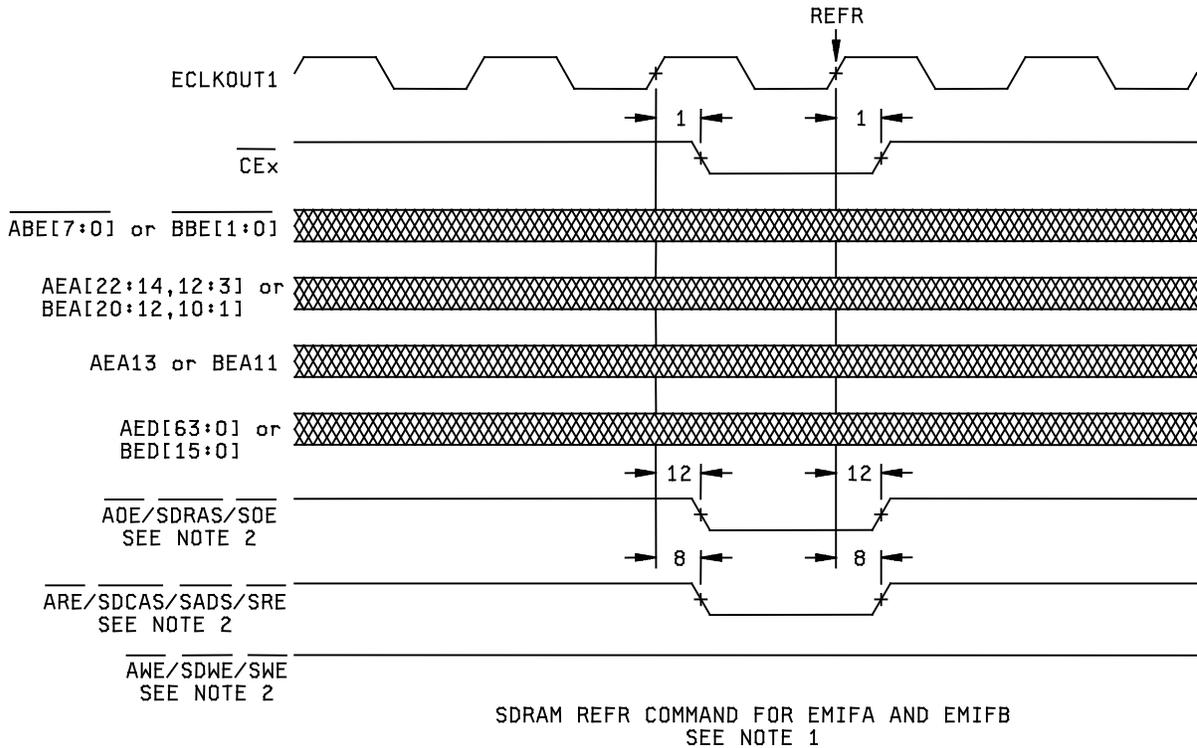


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} operate as \overline{SDCAS} / \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 18. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 45

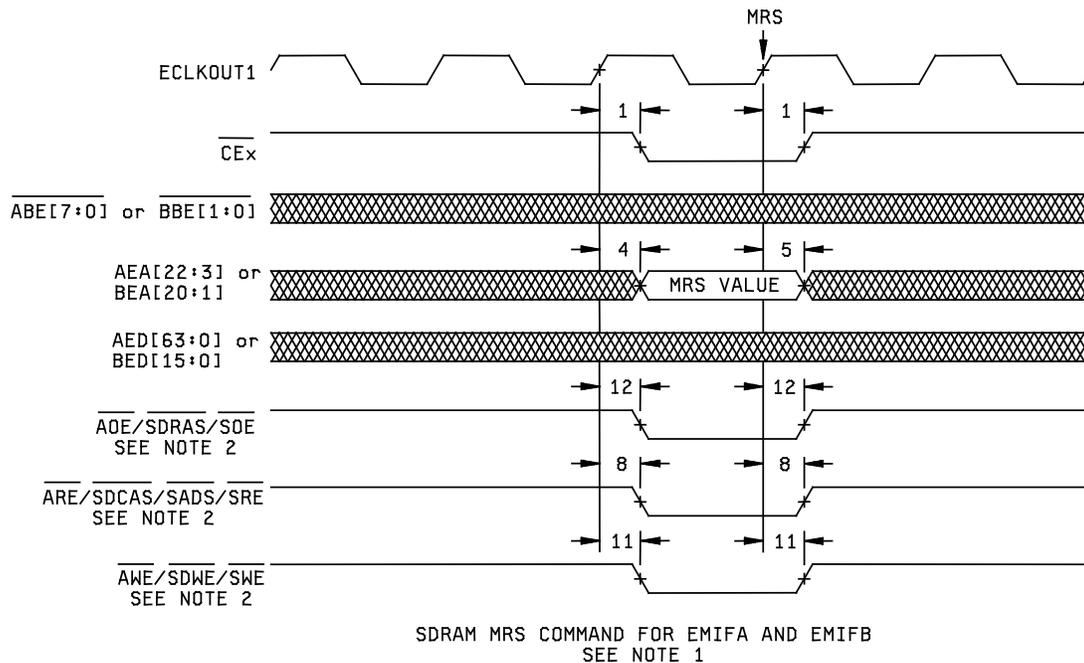


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} operate as \overline{SDCAS} / \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 19. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 46

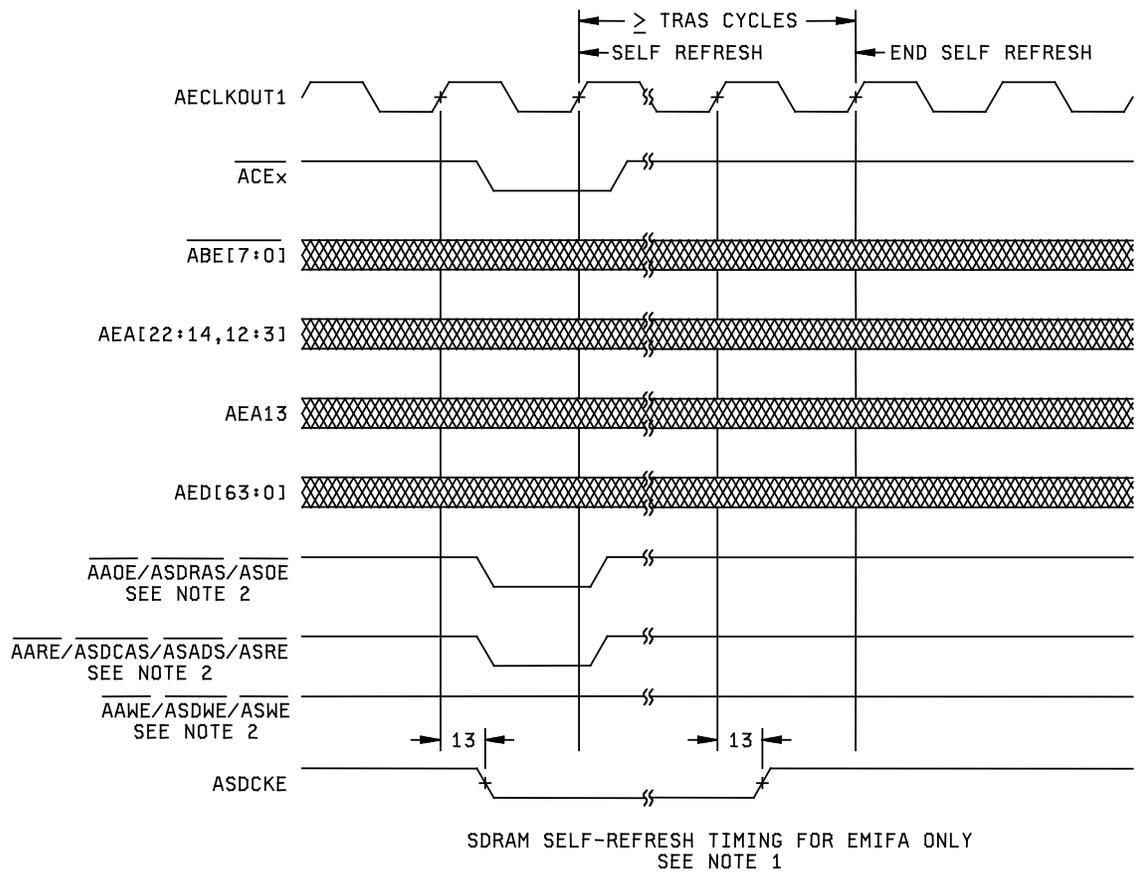


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} operate as \overline{SDCAS} / \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 20. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 47

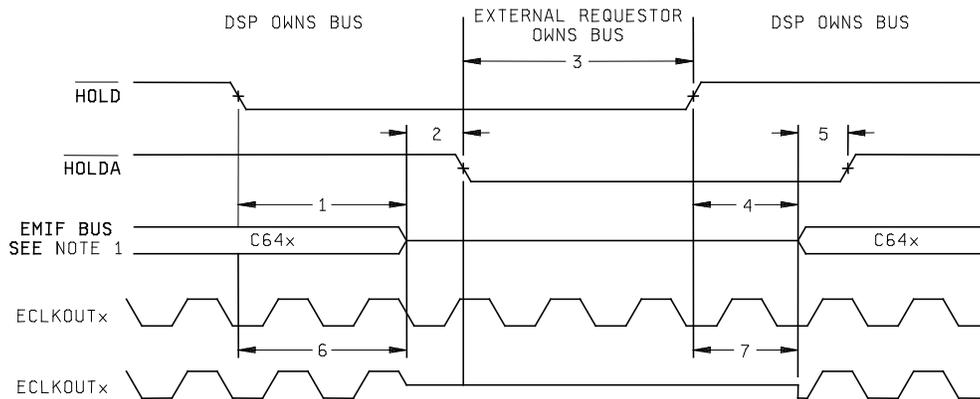


Notes:

1. These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g. the asynchronous memory access signals are shown as generic (\overline{AOE} , \overline{ARE} , and \overline{AWE}) instead of \overline{AAOE} , \overline{AARE} , and \overline{AAWE} (for EMIFA) and \overline{BAOE} , \overline{BARE} , and \overline{BAWE} (for EMIFB)].
2. \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} operate as \overline{SDCAS} / \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 21. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 48

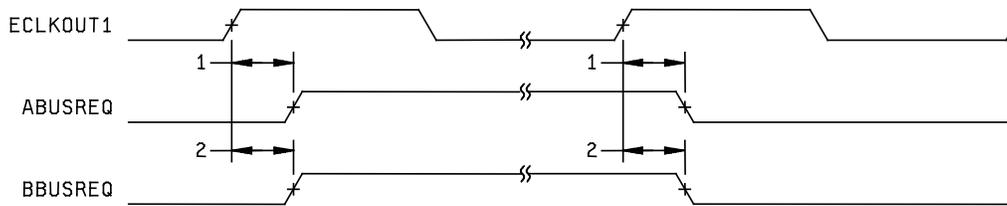


HOLD/HOLDA TIMING FOR EMIFA AND EMIFB

Notes:

- For EMIFA, EMIF bus consists of: $\overline{\text{ACE}}[3:0]$, $\overline{\text{ABE}}[7:0]$, $\overline{\text{AED}}[63:0]$, $\overline{\text{AEA}}[22:3]$, $\overline{\text{AARE}} / \overline{\text{ASDCAS}} / \overline{\text{ASADS}} / \overline{\text{ASRE}}$, $\overline{\text{AAOE}} / \overline{\text{ASDRAS}} / \overline{\text{ASOE}}$, and $\overline{\text{AAWE}} / \overline{\text{ASDWE}} / \overline{\text{ASWE}}$, $\overline{\text{ASDCKE}}$, $\overline{\text{ASOE}}$, and $\overline{\text{ADPT}}$.
 For EMIFB, EMIF bus consists of: $\overline{\text{BCE}}[3:0]$, $\overline{\text{BBE}}[1:0]$, $\overline{\text{BED}}[15:0]$, $\overline{\text{BEA}}[20:1]$, $\overline{\text{BARE}} / \overline{\text{BSDCAS}} / \overline{\text{BSADS}} / \overline{\text{BSRE}}$, $\overline{\text{BAOE}} / \overline{\text{BSDRAS}} / \overline{\text{BSOE}}$, and $\overline{\text{BAWE}} / \overline{\text{BSDWE}} / \overline{\text{BSWE}}$, $\overline{\text{BSOE}}$, and $\overline{\text{BDPT}}$.

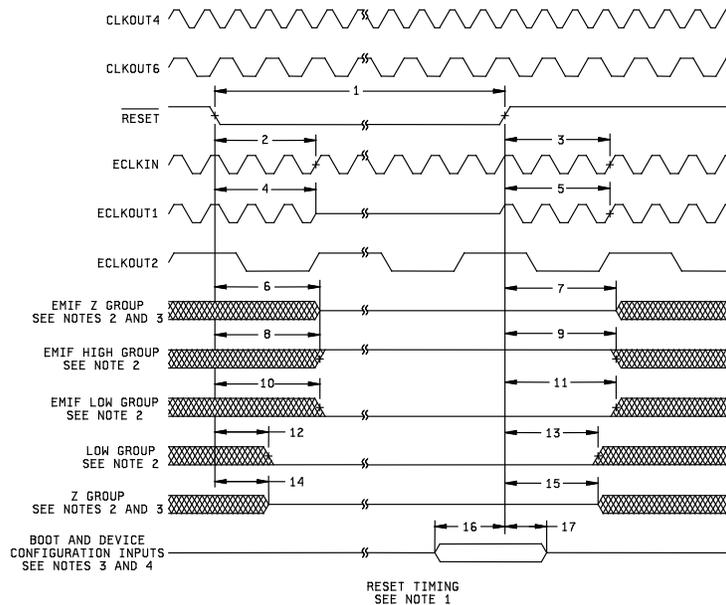
FIGURE 22. Timing waveforms.



BUSREQ TIMING FOR EMIFA AND EMIFB

FIGURE 23. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 49



Notes:

- These devices have two EMIFs (EMIFA and EMIFB). All EMIFA signals are prefixed by an "A" and all EMIFB signals are prefixed by a "B". Throughout the rest of this document, in generic EMIF areas of discussion, prefix "A" or "B" may be omitted [e.g ECLKIN, ECLKOUT1, AND ECLKOUT2].
- EMIF Z group consists of: $\overline{AEA}[22:3]$, $\overline{BEA}[20:1]$, $\overline{AED}[63:0]$, $\overline{BED}[15:0]$, $\overline{CE}[3:0]$, $\overline{ABE}[7:0]$, $\overline{BBE}[1:0]$, \overline{ARE} / \overline{SDCAS} / \overline{SADS} / \overline{SRE} , \overline{AWE} / \overline{SDWE} / \overline{SWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SOE} , $\overline{SOE3}$, \overline{ASDCKE} , and \overline{DPT} .
 EMIF high group consists of: \overline{AHOLDA} and \overline{BHOLDA} (when the corresponding \overline{HOLD} input is high)
 EMIF low group consists of: $\overline{ABUSREQ}$ and $\overline{BBUSREQ}$; \overline{AHOLDA} and \overline{BHOLDA} (when the corresponding \overline{HOLD} input is low)
 Low group consists of: $\overline{XSP_CS}$, $\overline{CLKX2/XSP_CLK}$, and $\overline{DX2/XSP_DO}$; all of which apply only when PCI EEPROM (BEA13) is enabled (with $\overline{PCI_EN} = 1$ and $\overline{MCBSP2_EN} = 0$). Otherwise, the $\overline{CLKX2/XSP_DO}$ pins are in the Z group. For more details on the PCI configuration pins, see the device configurations section from the manufacturer data sheet.
 Z group consists of: $\overline{HD}[31:0]/\overline{AD}[31:0]$, $\overline{CLKX0}$, $\overline{CLKX1/URADDR4}$, $\overline{CLKX2/XSP_CLK}$, $\overline{FSX0}$, $\overline{FSX1/UXADDR3}$, $\overline{FSX2}$, $\overline{DX0}$, $\overline{DX1/UXADDR4}$, $\overline{DX2/XSP_DO}$, $\overline{CLKR0}$, $\overline{CLKR1/URADDR2}$, $\overline{CLKR2}$, $\overline{FSR0}$, $\overline{FSR1/UXADDR2}$, $\overline{FSR2}$, $\overline{TOUT0}$, $\overline{TOUT1}$, $\overline{TOUT2}$, $\overline{GP}[8:0]$, $\overline{GP10/PCBE3}$, $\overline{HR/W/PCBE2}$, $\overline{HDS2/PCBE1}$, $\overline{PCBE0}$, $\overline{GP13/PINTA}$, $\overline{GP11/PREQ}$, $\overline{HDS1/PSERR}$, $\overline{HCS/PPERR}$, $\overline{HCNTL1/PDEVSEL}$, $\overline{HAS/PPAR}$, $\overline{HCNTL0/PSTOP}$, $\overline{HHWIL/PTRDY}$ (16 bit HPI mode only), $\overline{HRDY/PIRDY}$, $\overline{HINT/PFRAME}$, $\overline{UXDATA}[7:0]$, \overline{UXSOC} , \overline{UXCLAV} , and \overline{URCLAV} .
- If $\overline{BEA}[20:13]$, 11, 7] and $\overline{HD5/AD5}$ pins are actively driven, care must be taken to ensure no timing contention between parameters 6, 7, 14, 15, 16, and 17.
- Boot and device configurations Inputs (during reset) include: EMIFB address pins $\overline{BEA}[20:13]$, 11, 7] and $\overline{HD5/AD5}$. The $\overline{PCI_EN}$ pin must be driven valid at all times and the user must not switch values throughout device operation. The $\overline{MCBSP2_EN}$ pin must be driven valid at all times and the user can switch values throughout device operation.

FIGURE 24. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 50

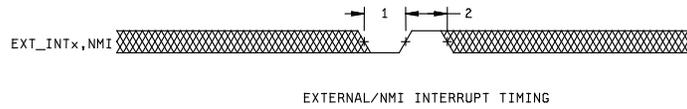
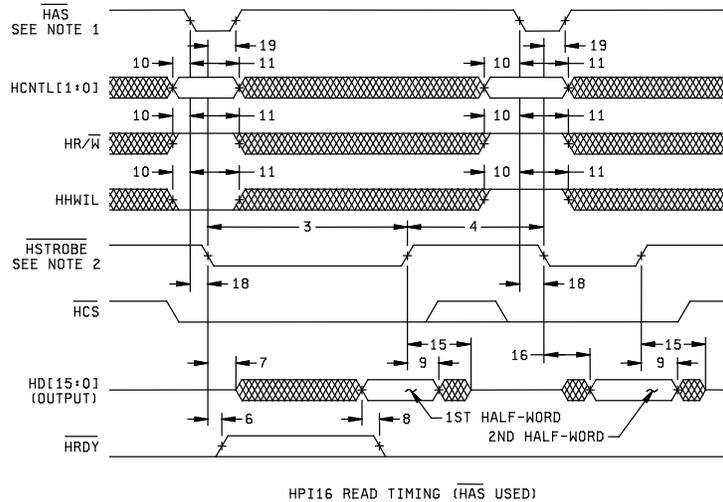
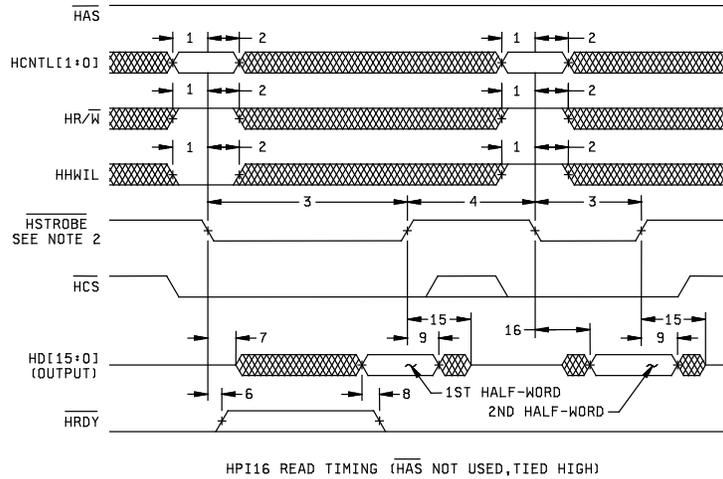


FIGURE 25. Timing waveforms.

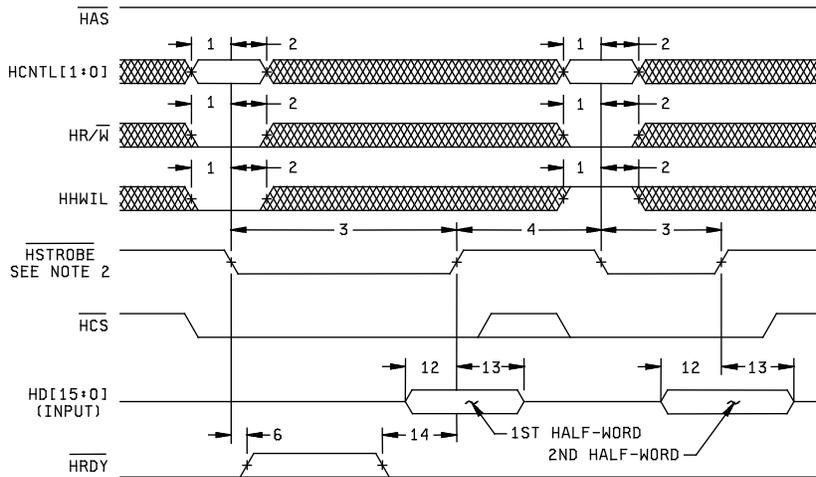


Notes:

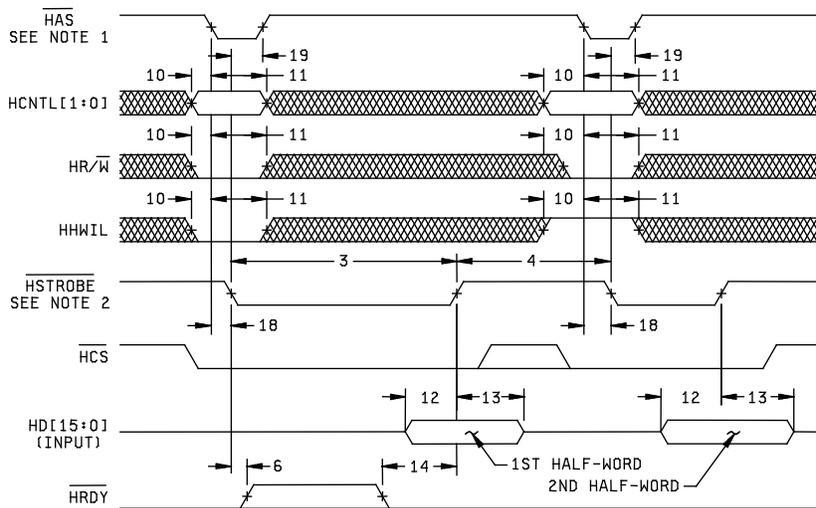
1. For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.
2. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})]$ or $\overline{\text{HCS}}$

FIGURE 26. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 51



HPI16 WRITE TIMING ($\overline{\text{HAS}}$ NOT USED, TIED HIGH)



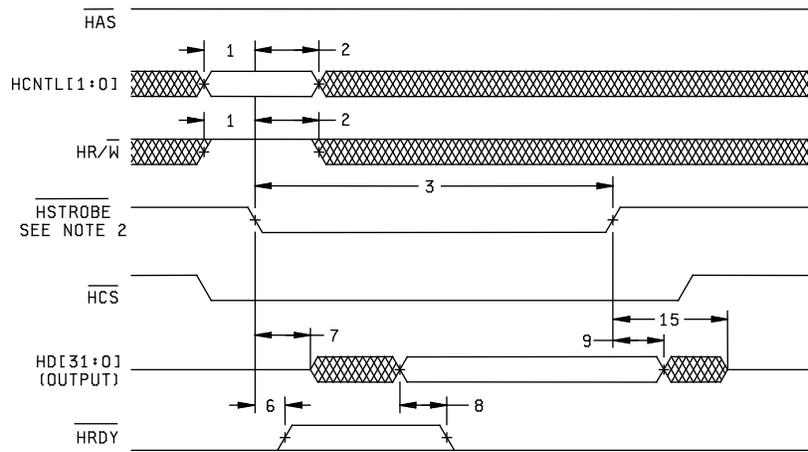
HPI16 WRITE TIMING ($\overline{\text{HAS}}$ USED)

Notes:

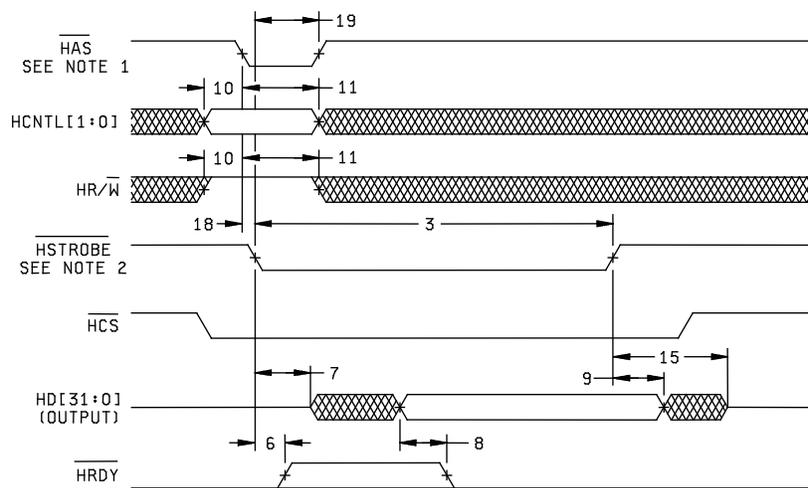
1. For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.
2. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})]$ or $\overline{\text{HCS}}$

FIGURE 27. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 52</p>



HP132 READ TIMING (HAS NOT USED, TIED HIGH)



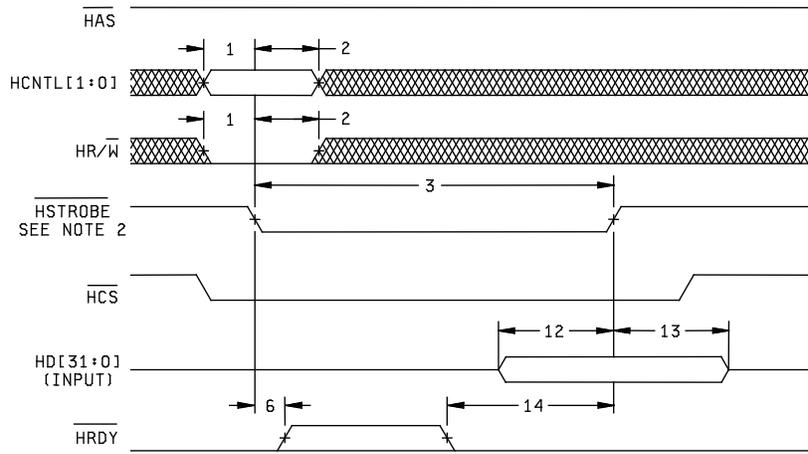
HP132 READ TIMING (HAS USED)

Notes:

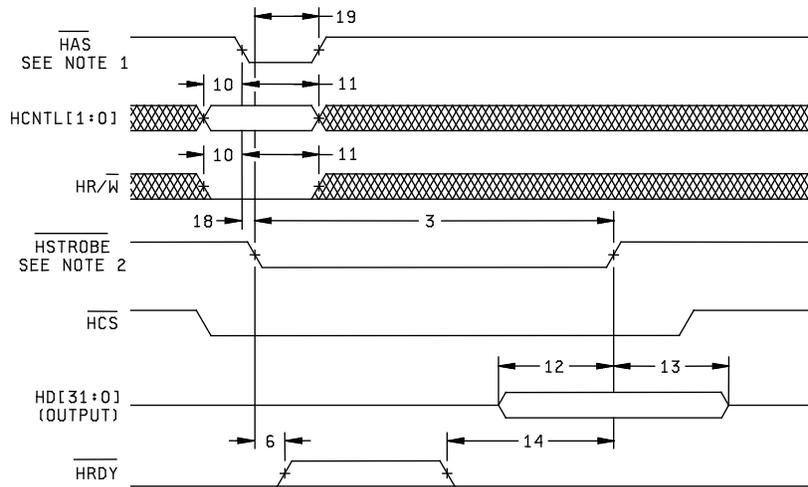
1. For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.
2. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})]$ or $\overline{\text{HCS}}$

FIGURE 28. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 53</p>



HP132 WRITE TIMING (HAS NOT USED, TIED HIGH)



HP132 WRITE TIMING (HAS USED)

Notes:

1. For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.
2. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})]$ or $\overline{\text{HCS}}$

FIGURE 29. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 54</p>

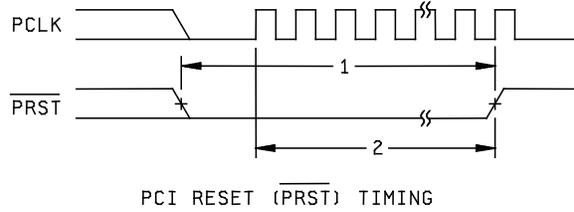
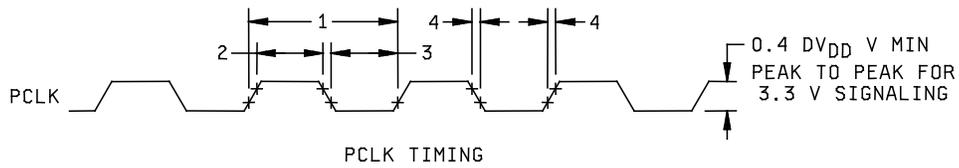


FIGURE 30. Timing waveforms.

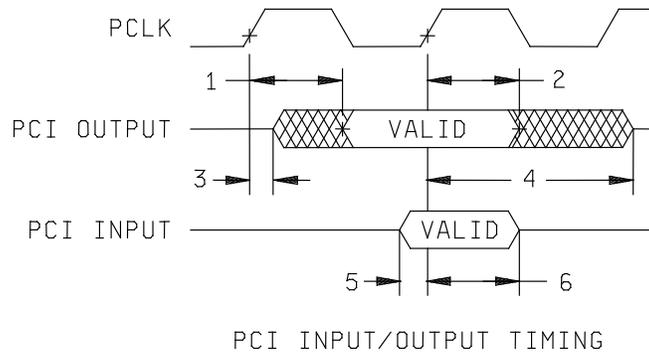


FIGURE 31. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 55

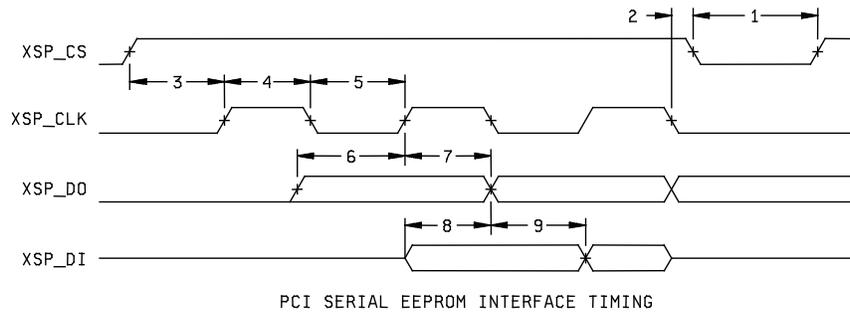


FIGURE 32. Timing waveforms.

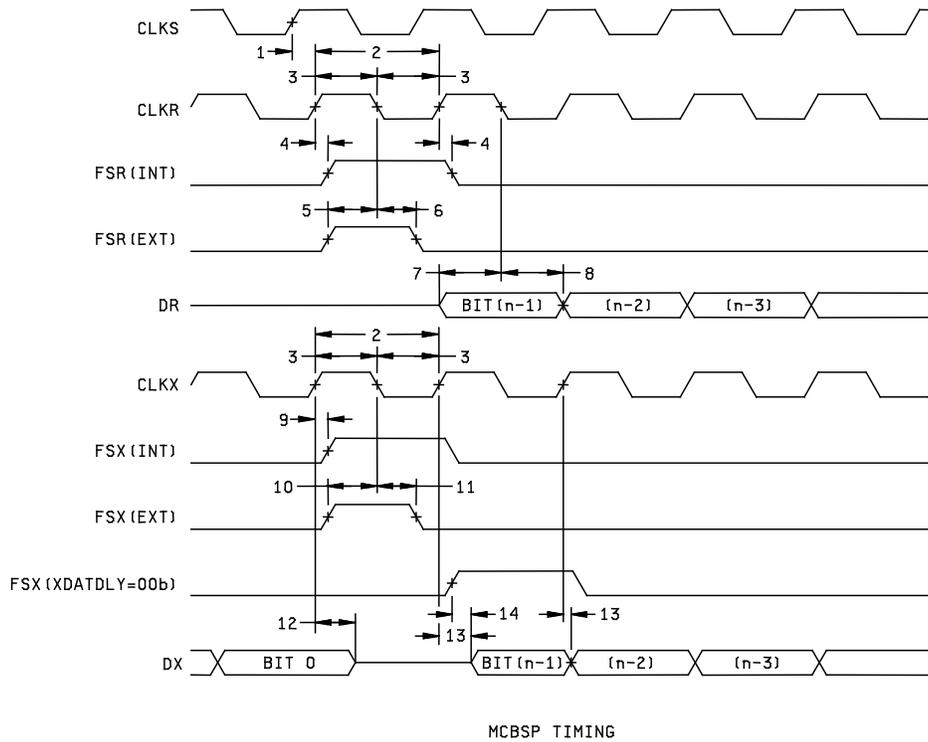


FIGURE 33. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 56</p>

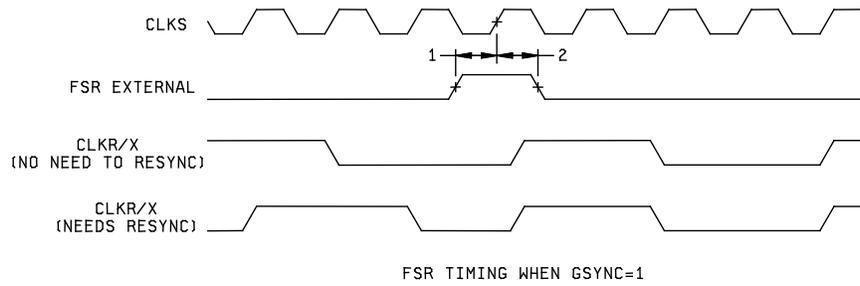


FIGURE 34. Timing waveforms.

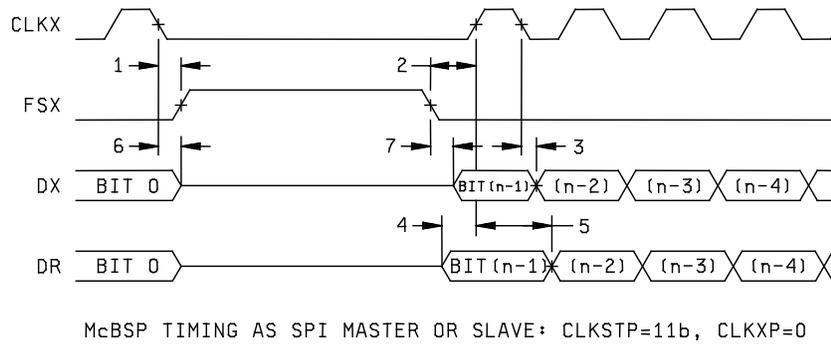
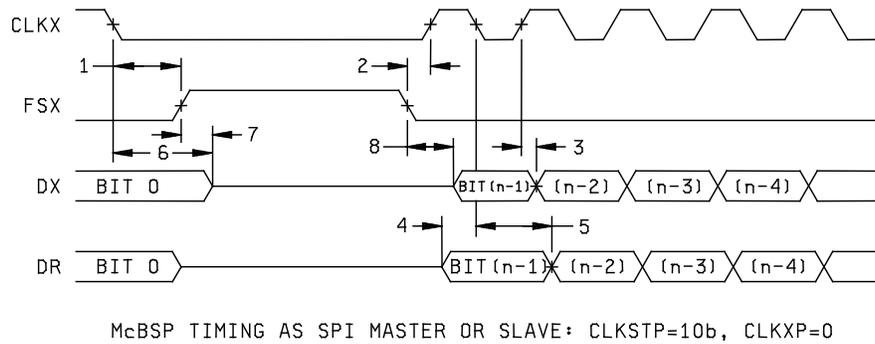
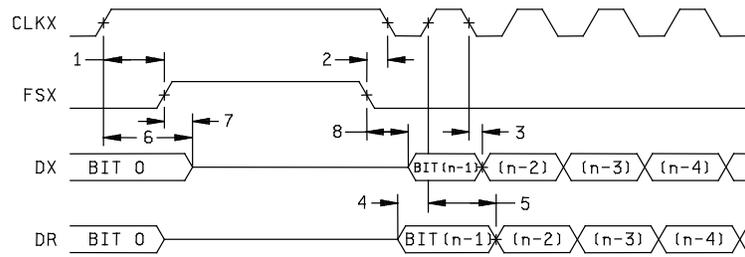
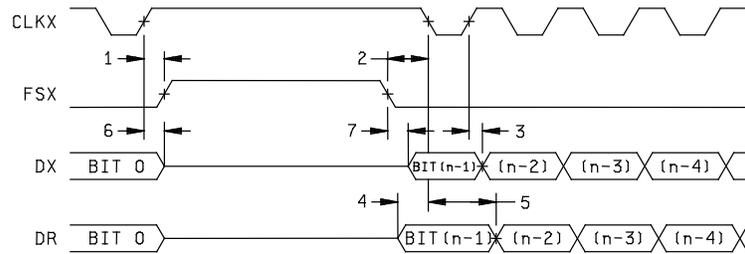


FIGURE 35. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 57

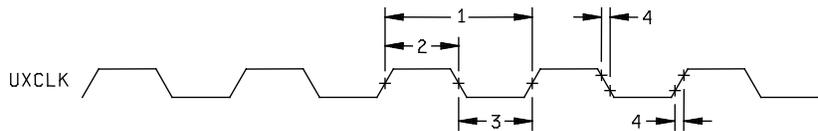


McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=10b, CLKXP=1

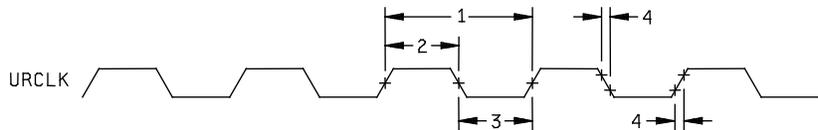


McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=11b, CLKXP=1

FIGURE 36. Timing waveforms.



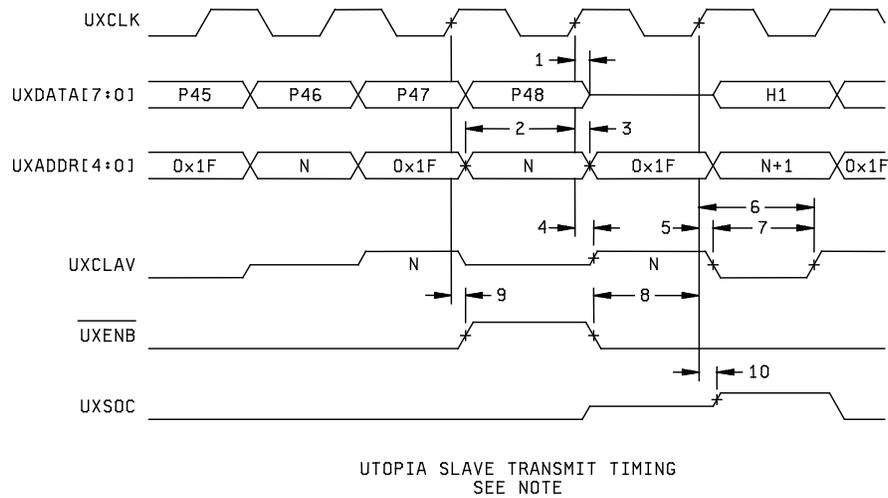
UXCLK TIMING



URCLK TIMING

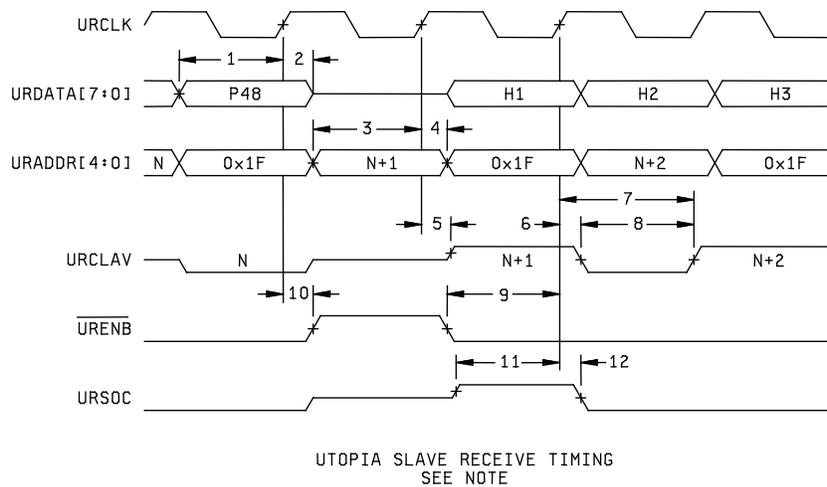
FIGURE 37. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 58</p>



Note: The UTOPIA slave module has signals that are middle level signals indicating a high impedance state (i.e., the UXCLAV and UXSOC signals).

FIGURE 38. Timing waveforms.



Note: The UTOPIA slave module has signals that are middle level signals indicating a high impedance state (i.e., the UXCLAV and UXSOC signals).

FIGURE 39. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 59

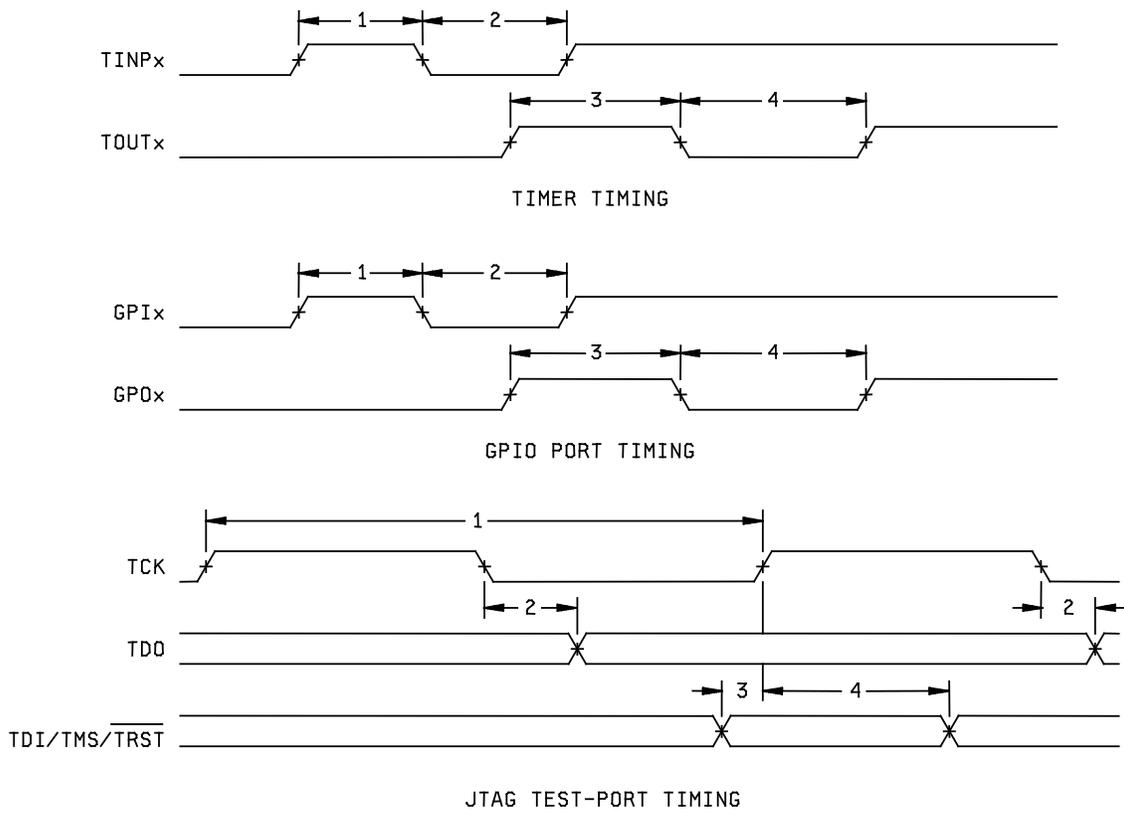


FIGURE 40. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/05607</p>
		<p>REV D</p>	<p>PAGE 60</p>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/05607-01XE	<u>2/</u>	
V62/05607-02XE	<u>2/</u>	
V62/05607-03XA	<u>2/</u>	SM32C6416TGLZA8EP
V62/05607-04XA	<u>2/</u>	SM32C6416TGLZI1EP
V62/05607-05YA	01295	SM32C6416TBGLZA8EP
V62/05607-06YA	01295	SM32C6416TBGLZI1EP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ Not available from an approved source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/05607
		REV D	PAGE 61