

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance of an IEEE 1394a-2000 OHCI PHY/link layer controller microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/05605</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TSB43AB23A-EP	IEEE 1394a-2000 OHCI PHY/Link-layer controller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	128	JEDEC MO-136	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.

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1.3 Absolute maximum ratings. 2/

Supply voltage range:

REG18	-0.2 V to +2.2 V
AV _{DD}	-0.3 V to +4.0 V
DV _{DD}	-0.3 V to +4.0 V
PLLV _{DD}	-0.3 V to +4.0 V
V _{DDP}	-0.5 V to +5.5 V
Input voltage range for PCI, V _I , PHY, and miscellaneous	-0.5 V to V _{DD} +0.5 V
Output voltage range for PCI, V _O , PHY and miscellaneous	-0.5 V to V _{DD} +0.5 V
Input clamp current, (I _{IK}) (V _I < 0 or V _I > V _{DD})	±20 mA <u>3/</u>
Output clamp current, (I _{OK}) (V _O < 0 or V _O > V _{DD})	±20 mA <u>4/</u>
Electrostatic discharge	HBM: 2 kV <u>5/</u>
Continuous total power dissipation	See dissipation rating table
Operating ambient temperature range, (T _A) : TSB43AB21AI	-40°C to +85°C
Storage temperature range, (T _{STG}).....	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from cage for 10 seconds	+260°C

Dissipation Rating Table

Case outline	T _A < 25°C Power rating	Derating Factor Above T _A = 25°C	T _A = 70°C Power Rating	T _A = 85°C Power Rating
X <u>6/</u>	1.116W	0.013 W/°C	0.513 W	0.312 W
X <u>7/</u>	0.8215 W	0.01 W/°C	0.377 W	0.229 W

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/ Applies to external input and bi-directional buffers. For 5-V tolerant use V_I > V_{DDI}. For PCI use V_I > V_{DDP}.

4/ Applies to external output and bi-directional buffers. For 5-V tolerant use V_O > V_{DDI}. For PCI use V_O > V_{DDP}.

5/HBM is human body model.

6/ Standard JEDEC high-K board.

7/ Standard JEDEC low-K board.

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1.4 Recommended operating conditions.

		Test condition	Min	Max	Unit
REG 18			1.6	2.0	V
Core voltage, AV_{DD}			3.0	3.6	V
Core voltage, DV_{DD}			3.0	3.6	V
Core voltage, $PLL_{V_{DD}}$			2.7	3.6	V
Output voltage, V_O		TTL and LVCMOS terminals	0	DV_{DD}	V
PCI I/O clamping voltage, V_{DDP}		$V_{DDP} = 3.3\text{ V}$	3.0	3.6	V
		$V_{DDP} = 5.0\text{ V}$	4.5	5.5	
High level input voltage, V_{IH} <u>8/</u>		PCI	3.3 V	$0.475V_{DDP}$	V
			5.0 V	V_{DDP}	
		PC(0-2)		$0.7 DV_{DD}$	V
		$\overline{G_RST}$		DV_{DD}	
Miscellaneous <u>9/</u>			2.0	V_{DDP}	
Low level input voltage, V_{IL} <u>8/</u>		PCI	3.3 V	0	V
			5.0 V	0	
		PC(0-2)		0	$0.2 DV_{DD}$
		$\overline{G_RST}$		0	$0.3 DV_{DD}$
Miscellaneous <u>9/</u>			0	0.8	
Input voltage, V_I		PCI	3.3 V	0	V
		Miscellaneous <u>9/</u>		0	
Output voltage, V_O <u>10/</u>		PCI	3.3 V	0	V
		Miscellaneous <u>9/</u>		0	
Input transition time (t_r and t_f), t_t			0	6	ns
Operating ambient temperature, T_A		$R\theta_{JA} = 70.82\text{ }^\circ\text{C/W}$		85	$^\circ\text{C}$
Output current, I_O		TPBIAS outputs	-5.6	1.3	mA
Differential input voltage, V_{ID}		Cable inputs, during data reception	118	260	mV
		Cable inputs, during arbitration	168	265	
Common-mode input voltage, V_{IC}		TPB cable inputs, source power node	0.4706	2.515	V
		TPB cable inputs, nonsource power node	0.4706	2.015 <u>11/</u>	
Maximum junction temperature, T_J		128-PDT high-K JEDEC board, $R\theta_{JA} = 74.6\text{ }^\circ\text{C/W}$, $P_D = 0.312\text{ W}$	$T_A = 85^\circ\text{C}$	105	$^\circ\text{C}$
		128-PDT low-K JEDEC board, $R\theta_{JA} = 101.3\text{ }^\circ\text{C/W}$, $P_D = 0.229\text{ W}$	$T_A = 85^\circ\text{C}$	105	$^\circ\text{C}$

8/ Applies to external inputs and bi-directional buffers without hysteresis.

9/ Miscellaneous terminals are: GPIO2(90), GPIO3 (89), SDA (92), SCL (91).

10/ Applies to external output buffers.

11/ For a node that does not source power; see section 4.2.2.2 in IEEE Std 1394a-2000.

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1.4 Recommended operating conditions - Continued.

		Test condition	Min	Max	Unit
Power setup reset time, t_{pu}	$\overline{G_RST}$ input		2		ms
Receiver input jitter	TPA, TPB cable inputs, S100 operation			± 1.08	ns
	TPA, TPB cable inputs, S200 operation			± 0.5	
	TPA, TPB cable inputs, S400 operation			± 0.315	
Receiver input skew	Between TPA and TPB cable inputs, S100 operation			± 0.8	ns
	Between TPA and TPB cable inputs, S200 operation			± 0.55	
	Between TPA and TPB cable inputs, S400 operation			± 0.5	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1394a-2000 - IEEE Standard for High Performance Serial Bus.

(Copies of these documents are available online at <http://www.ieee.org> or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Test load diagram. The test load diagram shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions Recommended operating conditions unless otherwise specified		Limits		Unit
				Min	Max	
High level output voltage	V _{OH}	PCI	I _{OH} = -0.5 mA	0.9 DV _{DD}		V
			I _{OH} = -2 mA	2.4		
		Miscellaneous 2/	I _{OH} = -4 mA	DV _{DD} - 0.6		
Low level output voltage	V _{OL}	PCI	I _{OL} = 1.5 mA		0.1 DV _{DD}	V
			I _{OL} = 6 mA		0.55	
		Miscellaneous 2/	I _{OL} = 4 mA		0.5	
Three-state output high impedance	I _{OZ}	Output pins	V _{DD} = 3.6 V, V _O = DV _{DD} or GND		±20	μA
Low level input current	I _{IL}	Input pins	V _{DD} = 3.6 V, V _I = GND		±20	μA
		I/O pins 3/	V _{DD} = 3.6 V, V _I = GND	±20		
High level input current	I _{IH}	PCI 3/	V _{DD} = 3.6 V, V _I = DV _{DD}		±20	μA
		Others 3/	V _{DD} = 3.6 V, V _I = DV _{DD}	±20		
Device						
Supply current (internal voltage regulator enabled, REG_EN = L)	I _{DD}	4/		158 Typ		mA
		5/		128 Typ		
		6/		69.8 Typ		
Supply current – ultra low power mode (internal voltage regulator enabled, REG_EN = L)	I _{DD(ULP)}	Ports disabled, V _{DD} = 1.8 V (internal), T _A = 25°C		3 Typ		mA
Supply current – ultra low power mode (internal voltage regulator disabled, REG_EN = H, REG18 = 1.8 V)	I _{DD(ULP)}	Ports disabled, V _{DD} = 1.8 V (external), T _A = 25°C		50 Typ		μA
Power status threshold, CPS inputs 7/	V _{TH}	400 kΩ resistor 7/		4.7	7.5	V
TPBIAS output voltage	V _O	At rated I _O current		1.665	2.015	V
Input current (PC0-PC2 inputs)	I _I	V _{DD} = 3.6 V			5	μA
Pullup current ($\overline{G_RST}$ input)	I _{IRST}	V _I = 1.5 V		-90	-20	μA
		V _I = 0 V		-90	-20	
Driver						
Differential output voltage	V _{OD}	56 Ω, see figure 4		172	265	mV
Driver difference current, TPA+, TPA-, TPB+, TPB-	I _{DIFF}	Drivers enabled, speed signaling off		-1.05 8/	1.05 8/	mA
Common-mode speed signaling current, TPB+, TPB-	I _{SP200}	S200 speed signaling enabled		-4.84 9/	-2.53 9/	mA
Common-mode speed signaling current, TPB+, TPB-	I _{SP400}	S400 speed signaling enabled		-12.4 9/	-8.1 9/	mA
Off state differential voltage	V _{OFF}	Drivers disabled, see figure 4			20	mV

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions Recommended operating conditions unless otherwise specified	Limits		Unit
			Min	Max	
Receiver					
Differential impedance	Z _{ID}	Drivers disabled	4		kΩ
				4	pF
Common mode impedance	Z _{IC}	Drivers disabled	20		kΩ
				24	pF
Receiver input threshold voltage	V _{TH-R}	Drivers disabled	-30	30	mV
Cable bias detect threshold, TPBx cable inputs	V _{TH-CB}	Drivers disabled	0.6	1	V
Positive arbitration comparator threshold voltage	V _{TH+}	Drivers disabled	89	168	MV
Negative arbitration comparator threshold voltage	V _{TH-}	Drivers disabled	-168	-89	mV
Speed signal threshold	V _{TH-SP200}	TPBIAS-TPA common mode voltage, drivers disabled	49	131	mV
Speed signal threshold	V _{TH-SP400}	TPBIAS-TPA common mode voltage, drivers disabled	314	396	mV
Thermal characteristics					
R _{θJA} , high K board	128-PDT	Board mounted, no air flow, JEDEC test board		74.6	°C/W
R _{θJA} , low K-board	128-PDT			101.3	°C/W
R _{θJC}	128-PDT			18.7	°C/W
Switching characteristics for PHY port interface					
Jitter, transmit		Between TPA and TPB		±0.15	ns
Skew, transmit		Between TPA and TPB		±0.1	ns
TP differential rise time, transmit	t _r	10% to 90%, at 1394 connector	0.5	1.2	ns
TP differential fall time, transmit	t _f	90% to 10%, at 1394 connector	0.5	1.2	ns
Operating, timing, and switching characteristics of XI					
	V _{DD}		3.0	3.6	V(PLL _{VDD})
High level input voltage	V _{IH}		0.63 V _{DD} Typ		V
Low level input voltage	V _{IL}			0.33 V _{DD}	V
Input clock frequency			24.576 Typ		MHz
Input clock frequency tolerance				<100	PPM
Input slew rate			0.2	4	V/ns
Input clock duty cycle			40%	60%	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

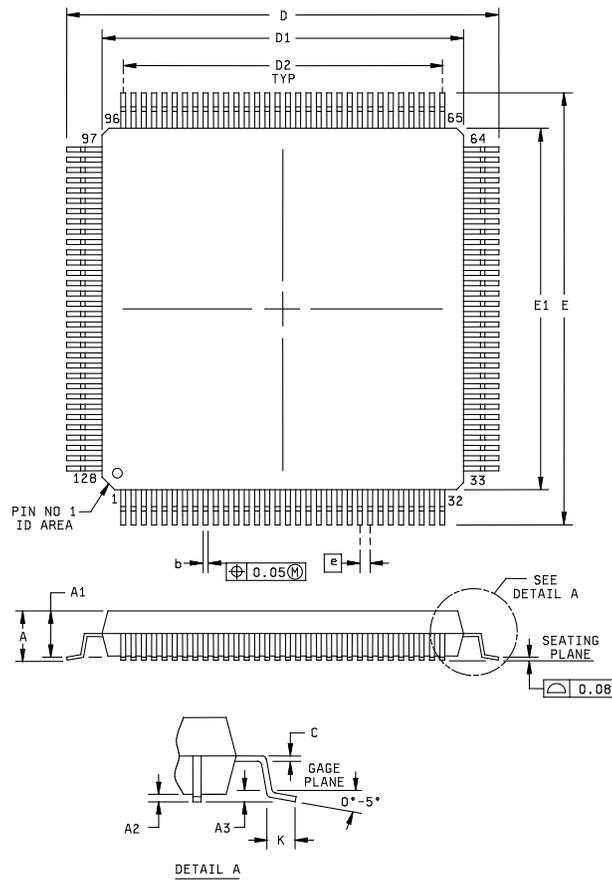
Test	Symbol	Test conditions Recommended operating conditions unless otherwise specified	Limits		Unit
			Min	Max	
Switching characteristics for PCI interface 10/					
Setup time for PCLK	t_{su}	-50% to 50%	7		ns
Hold time for PCLK	t_h	-50% to 50%	0		ns
Delay time, PCLK to data valid	t_{val}	-50% to 50%	2	11	ns

Notes:

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific testing, product performance is assured by characterization and/or design.
- 2/ Miscellaneous terminals are: GPIO2(90), GPIO3 (89), SDA (92), SCL (91).
- 3/ For I/o terminals, input leakage (I_{IL} and I_{IH}) includes I_{OZ} of the disabled output.
- 4/ Transmit data (transmit on all ports full isochronous payload of 84 μ s, S400, data value of CCCC CCCCh).
- 5/ Repeat data (receive on one port, transmit on other two ports, full isochronous payload of 84 μ s, S400, data value of CCCC CCCCh).
- 6/ Idle (receive or transmit cycle start on the port), $V_{DD} = 3.3$ V, $T_A = 25^\circ$ C.
- 7/ Measured at cable power side of resistor.
- 8/ Limits defined as algebraic sum of TPA+ and TPA- driver currents. Limits also apply to TPB+ and TPB- algebraic sum of driver currents.
- 9/ Limits defined as absolute limit of each of TPB+ and TPB- driver currents.
- 10/ These parameters are ensured by design.

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Case X



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		1.20		.047	D/E	15.90	16.10	.626	.634
A1	0.95	1.05	.037	.041	D1/E1	13.95	14.05	.549	.553
A2	0.05		.002		D2	12.40 Typ		.488 Typ	
A3	0.25 Typ		.010		e	0.40 Typ		.016 Typ	
b	0.13	0.23	.005	.009	L	0.45	0.75	.018	.030
C	0.13 NOM		.005 NOM						

Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-136

FIGURE 1. Case outline.

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Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	DGND	33	PCI_AD13	65	DV _{DD}	97	AGND
2	PCI_C/ $\overline{\text{BE3}}$	34	PCI_AD12	66	DGND	98	AV _{DD}
3	V _{DDP}	35	PCI_AD11	67	CAN	99	R1
4	PCI_IDSEL	36	DGND	68	PHY_TEST_MA	10	R0
5	PCI_AD23	37	PCI_AD10	69	CPS	101	FILTER0
6	PCI_AD22	38	PCI_AD9	70	AV _{DD}	102	FILTER1
7	DV _{DD}	39	PCI_AD8	71	AGND	103	PLL _{VDD}
8	PCI_AD21	40	DV _{DD}	72	AV _{DD}	104	PLL _{GND}
9	PCI_AD20	41	PCI_C/ $\overline{\text{BE0}}$	73	AGND	105	X1
10	PCI_AD19	42	PCI_AD7	74	TPB0-	106	X0
11	PCI_AD18	43	DGND	75	TPB0+	107	$\overline{\text{REG_EN}}$
12	DGND	44	PCI_AD6	76	AGND	108	$\overline{\text{PCI_CLKRUN}}$
13	PCI_AD17	45	PCI_AD5	77	TPA0-	109	$\overline{\text{PCI_INTA}}$
14	PCI_AD16	46	V _{DDP}	78	TPA0+	110	$\overline{\text{G_RST}}$
15	PCI_C/ $\overline{\text{BE2}}$	47	PCI_AD4	79	TPBIAS0	111	DV _{DD}
16	V _{DDP}	48	PCI_AD3	80	AGND	112	PCI_PCLK
17	$\overline{\text{PCI_FRAME}}$	49	PCI_AD2	81	AV _{DD}	113	DGND
18	$\overline{\text{PCI_IRDY}}$	50	PCI_AD1	82	TB1-	114	$\overline{\text{PCI_GNT}}$
19	DV _{DD}	51	DGND	83	TB1+	115	$\overline{\text{PCI_REQ}}$
20	$\overline{\text{PCI_TRDY}}$	52	PCI_AD0	84	AGND	116	V _{DDP}
21	$\overline{\text{PCI_DEVSEL}}$	53	$\overline{\text{PCI_RST}}$	85	AV _{DD}	117	$\overline{\text{PCI_PME}}$
22	$\overline{\text{PCI_STOP}}$	54	CYCLEOUT	86	TPA1-	118	PCI_AD31
23	DGND	55	CYCLEIN	87	TPA1+	119	DGND
24	$\overline{\text{PCI_PERR}}$	56	DV _{DD}	88	TPBIAS1	120	PCI_AD30
25	$\overline{\text{PCI_SERR}}$	57	GPIO3/TEST1	89	AGND	121	PCI_AD29
26	PCI_PAR	58	GPIO2/TEST0	90	AV _{DD}	122	PCI_AD28
27	DV _{DD}	59	SCL	91	TPB2-	123	DV _{DD}
28	PCI_C/ $\overline{\text{BE1}}$	60	SDA	92	TPB2+	124	PCI_AD27
29	PCI_AD15	61	REG18	93	AV _{DD}	125	PCI_AD26
30	DV _{DDP}	62	PC2	94	TPA2-	126	REG18
31	PCI_AD14	63	PC1	95	TPA2+	127	PCI_AD25
32	DGND	64	PC0	96	TPBIAS2	128	PCI_AD24

FIGURE 2. Terminal connections.

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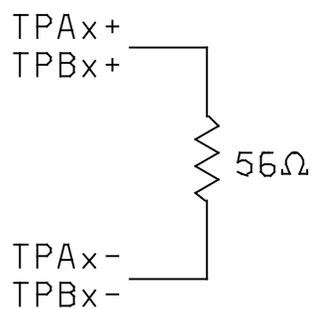


FIGURE 4. Test load diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/05605-01XE	01295	TSB43AB23IPDTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243
Point of contact: U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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