REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under paragraph 6.3, delete CAGE 01295 as a source of supply for the 02XA device. - ro	05-06-17	R. MONNIN
B	Correct lead finishes on last page. Update boilerplate. - CFS	05-12-02	Thomas M. Hess
C	Add device type 04. Make a change to the symbol “c” min dimension from 0.007 inch (0.17 mm) to 0.005 inch (0.13 mm). - ro	10-01-19	C. SAFFLE
D	Update document paragraphs to current requirements. - ro	16-04-07	C. SAFFLE
E	Delete second sentence from note 4 as specified under figure 1. Update document paragraphs to current requirements. - ro	22-01-19	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	E	E	E	E	E	E	E	E														
PAGE	18	19	20	21	22	23	24	25														
REV STATUS OF PAGES	**REV**			E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E		
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/landandmaritime**
Original date of drawing YY-MM-DD 05-02-10	**CHECKED BY** TOM HESS **APPROVED BY** RAYMOND MONNIN	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 3.3 V RS-485 TRANSCEIVER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/05604**
	REV **E**	**PAGE** 1 **OF** 25

AMSC N/A

5962-V001-22

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3 V RS-485 transceiver microcircuit, with device types 01 and 02 having a operating temperature range of -40°C to +125°C, device type 03 having a operating temperature range of -40°C to +85°C, and device type 04 having a operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05604	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function	Signaling rate
01	SN65HVD10-EP	3.3 V RS-485 transceiver	25 Mbps
02	SN65HVD11-EP	3.3 V RS-485 transceiver	10 Mbps
03	SN65HVD12-EP	3.3 V RS-485 transceiver	1 Mbps
04	SN65HVD10-EP	3.3 V RS-485 transceiver	25 Mbps

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012 AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.3 V to 6 V
Voltage range at A or B ..... -9 V to 14 V
Input voltage range at D, DE, R, or $\overline{RE}$ ..... -0.5 V to V_{CC} +0.5 V
Voltage input range, transient pulse, A and B through 100 Ω (see figure 15) ..... -50 V to 50 V
Electrostatic discharge (ESD):
  Human body model: 3/
    A, B, and GND ..... 16 kV
    All pins ..... 4 kV
  Charged device model: 4/
    All pins charge ..... 1 kV
Continuous total power dissipation ..... See dissipation rating table
Junction temperature (T_J) ..... 170°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Thermal resistance, junction-to-ambient (θ_{JA}) 5/

1.4 Recommended operating conditions. 6/

Supply voltage range (V_{CC}) ..... 3 V minimum to 3.6 V maximum
Voltage at any bus terminal (separately or common mode) V_I or V_{IC} ..... -7 V minimum to 12 V maximum 7/
High level input voltage (V_{IH}) at D, DE, $\overline{RE}$ pins ..... 2 V minimum to V_{CC} maximum
Low level input voltage (V_{IL}) at D, DE, $\overline{RE}$ pins ..... 0 V minimum to 0.8 V maximum
Differential input voltage (V_{ID}) (see figure 11) ..... -12 V minimum to 12 V maximum
High level output current (I_{OH}):
  Driver ..... -60 mA minimum
  Receiver ..... -8 mA minimum
Low level output current (I_{OL}):
  Driver ..... 60 mA maximum
  Receiver ..... 8 mA maximum
Differential load resistance (R_L) ..... 54 Ω minimum
Differential load capacitance (C_L) ..... 50 pF nominal
Signaling rate
  Device types 01 and 04 ..... 25 Mbps maximum
  Device type 02 ..... 10 Mbps maximum
  Device type 03 ..... 1 Mbps maximum
Junction temperature (T_J) ..... 145°C maximum 5/

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
3/ Tested in accordance with JEDEC standard 22, test method A114-A.
4/ Tested in accordance with JEDEC standard 22, test method C101.
5/ See thermal characteristics section in 1.5.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
7/ The algebraic convention, in which the least positive (most negative) limit is designated as minimum in this data sheet.

1.5 Thermal characteristics.

Junction-to-ambient thermal resistance (θ_{JA}) (high K board, no airflow) ..... 121°C/W typical 8/ 9/
Junction-to-board thermal resistance (θ_{JB}) (high K board) ..... 67°C/W typical
Junction-to-case thermal resistance (θ_{JC}) ..... 41°C/W typical
Device power dissipation (P_D):
(R_L = 60 Ω, C_L = 50 pF, DE at V_{CC} $\overline{RE}$ at 0 V, input to D a 50% duty cycle square wave at indicated signaling rate)
Device types 01 and 04 (25 Mbps) ..... 233 mW maximum
Device type 02 (10 Mbps) ..... 176 mW maximum
Device type 03 (500 kbps) ..... 161 mW maximum
Ambient air temperature (T_A) (high K board, no airflow) ..... -40°C to +116°C
Thermal shutdown junction temperature (T_{JSD}) ..... 165°C typical

Package dissipation ratings table.

Package	$T_A \leq 25°C$ power rating	Derating factor 1/ above T_A = 25°C	T_A = 70°C power rating	T_A = 85°C power rating	T_A = 125°C power rating
X 2/	597 mW	4.97 mW/°C	373 mV	298 mW	100 mW
X 3/	990 mW	8.26 mW/°C	620 mW	496 mW	165 mW

1/ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
2/ Tested in accordance with the low-K thermal metric definitions of EIA/JESD51-3.
3/ Tested in accordance with the high-K thermal metric definitions of EIA/JESD51-7.

8/ The intent of θ_{JA} specification is solely for thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application specific environment.
9/ JESD51-7, high effective thermal conductivity test board for leaded surface mount packages.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-3	–	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JEDEC 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD22-A114	–	Electrostatic Discharge Sensitivity Testing Human Body Model
JESD22-C101	–	Field Induced Charged Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth tables. The truth tables shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 5 through 15.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics section.							
Input clamp voltage	V_{IK}	I_I = -18 mA	-40°C to +125°C	01,02	-1.5		V
			-40°C to +85°C	03	-1.5		
			-55°C to +125°C	04	-1.5		
Differential output voltage 2/	$\|V_{OD}\|$	I_O = 0	-40°C to +125°C	01,02	2	V_{CC}	V
			-40°C to +85°C	03	2	V_{CC}	
			-55°C to +125°C	04	2	V_{CC}	
		R_L = 54 Ω, see figure 5	-40°C to +125°C	01,02	1.5		
			-40°C to +85°C	03	1.5		
			-55°C to +125°C	04	1.5		
		V_{test} = -7 V to 12 V, see figure 6	-40°C to +125°C	01,02	1.5		
			-40°C to +85°C	03	1.5		
			-55°C to +125°C	04	1.5		
Change in magnitude of differential output voltage	$\Delta\|V_{OD}\|$	See figures 5 and 6	-40°C to +125°C	01,02	-0.2	0.2	V
			-40°C to +85°C	03	-0.2	0.2	
			-55°C to +125°C	04	-0.2	0.2	
Peak-to-peak common mode output voltage	$V_{OC(PP)}$	See figure 7 3/	+25°C	01,02, 03,04	400 typical		mV
Steady state common mode output voltage	$V_{OC(SS)}$	See figure 7	-40°C to +125°C	01,02	1.4	2.5	V
			-40°C to +85°C	03	1.4	2.5	
			-55°C to +125°C	04	1.4	2.5	
Change in steady state common mode output voltage	$\Delta V_{OC(SS)}$	See figure 7	-40°C to +125°C	01,02	-0.05	0.05	V
			-40°C to +85°C	03	-0.05	0.05	
			-55°C to +125°C	04	-0.05	0.05	

See footnotes at end of Driver electrical characteristics section.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics section - continued.							
High impedance output current	I_{OZ}	See receiver input currents	-40°C to +125°C	01,02			
			-40°C to +85°C	03			
			-55°C to +125°C	04			
Input current	I_I	D pin	-40°C to +125°C	01,02	-100	0	µA
			-40°C to +85°C	03	-100	0	
			-55°C to +125°C	04	-100	0	
		DE pin	-40°C to +125°C	01,02	0	100	
			-40°C to +85°C	03	0	100	
			-55°C to +125°C	04	0	100	
Short circuit output current	I_{OS}	-7 V ≤ V_O ≤ 12 V	-40°C to +125°C	01,02	-250	250	mA
			-40°C to +85°C	03	-250	250	
			-55°C to +125°C	04	-250	250	
Differential output capacitance 3/	$C_{(OD)}$	V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V	+25°C	01,02, 03,04	16 typical		pF
Supply current	I_{CC}	$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, no load, receiver disabled and driver enabled	-40°C to +125°C	01,02		15.5	mA
			-40°C to +85°C	03		15.5	
			-55°C to +125°C	04		15.5	
		$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, no load, receiver disabled and driver disabled (standby)	-40°C to +125°C	01,02		5	µA
			-40°C to +85°C	03		5	
			-55°C to +125°C	04		5	
		$\overline{RE}$ at 0 V, D and DE at V_{CC}, no load, receiver enabled and driver enabled	-40°C to +125°C	01,02		15.5	mA
			-40°C to +85°C	03		15.5	
			-55°C to +125°C	04		15.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ For T_A > 85°C, V_{CC} is ±5 %.

3/ All typical values are at 25°C and with a 3.3 V supply.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics section.							
Propagation delay time, low to high level output	t_{PLH}	R_L = 54 Ω, C_L = 50 pF, see figure 8	-40°C to +125°C	01	5	16	ns
			-40°C to +125°C	02	18	40	
			-40°C to +85°C	03	135	330	
			-55°C to +125°C	04	5	16	
Propagation delay time, high to low level output	t_{PHL}	R_L = 54 Ω, C_L = 50 pF, see figure 8	-40°C to +125°C	01	5	16	ns
			-40°C to +125°C	02	18	40	
			-40°C to +85°C	03	135	330	
			-55°C to +125°C	04	5	16	
Differential output signal rise time	t_r	R_L = 54 Ω, C_L = 50 pF, see figure 8	-40°C to +125°C	01	3	11.5	ns
			-40°C to +125°C	02	10	30	
			-40°C to +85°C	03	100	330	
			-55°C to +125°C	04	3	11.5	
Differential output signal fall time	t_r	R_L = 54 Ω, C_L = 50 pF, see figure 8	-40°C to +125°C	01	3	11.5	ns
			-40°C to +125°C	02	10	30	
			-40°C to +85°C	03	100	330	
			-55°C to +125°C	04	3	11.5	

See footnotes at end of Driver switching characteristics section.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics section – continued.							
Pulse skew ($t_{PHL} – t_{PLH}$)	$t_{sk(p)}$	R_L = 54 Ω, C_L = 50 pF, see figure 8	-40°C to +125°C	01		1.5	ns
			-40°C to +125°C	02		2.5	
			-40°C to +85°C	03		9	
			-55°C to +125°C	04		1.5	
Part to part skew 2/	$t_{sk(pp)}$		-40°C to +125°C	01		6	ns
			-40°C to +125°C	02		11	
			-40°C to +85°C	03		100	
			-55°C to +125°C	04		6	
Propagation delay time, high impedance to high level output	t_{PZH}	R_L = 110 Ω, $\overline{RE}$ at 0 V, see figure 9	-40°C to +125°C	01		33	ns
			-40°C to +125°C	02		55	
			-40°C to +85°C	03		320	
			-55°C to +125°C	04		33	
Propagation delay time, high level to high impedance output	t_{PHZ}	R_L = 110 Ω, $\overline{RE}$ at 0 V, see figure 9	-40°C to +125°C	01		26	ns
			-40°C to +125°C	02		55	
			-40°C to +85°C	03		320	
			-55°C to +125°C	04		26	
Propagation delay time, high impedance to low level output	t_{PZL}	R_L = 110 Ω, $\overline{RE}$ at 0 V, see figure 10	-40°C to +125°C	01		26	ns
			-40°C to +125°C	02		55	
			-40°C to +85°C	03		320	
			-55°C to +125°C	04		26	

See footnotes at end of Driver switching characteristics section.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics section - continued.							
Propagation delay time, low level to high impedance output	t_{PLZ}	R_L = 110 Ω, $\overline{RE}$ at 0 V, see figure 10	-40°C to +125°C	01		26	ns
			-40°C to +125°C	02		75	
			-40°C to +85°C	03		420	
			-55°C to +125°C	04		26	
Propagation delay time, standby to high level output	t_{PZH}	R_L = 110 Ω, $\overline{RE}$ at 3 V, see figure 9	-40°C to +125°C	01,02		6	µs
			-40°C to +85°C	03		6	
			-55°C to +125°C	04		14	
Propagation delay time, standby to low level output	t_{PZL}	R_L = 110 Ω, $\overline{RE}$ at 3 V, see figure 10	-40°C to +125°C	01,02		6	µs
			-40°C to +85°C	03		6	
			-55°C to +125°C	04		14	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ tsk(pp) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics section.							
Positive going input threshold voltage	V_{IT+}	I_O = -8 mA	-40°C to +125°C	01,02		-0.01	V
			-40°C to +85°C	03		-0.01	
			-55°C to +125°C	04		-0.01	
Negative going input threshold voltage	V_{IT-}	I_O = 8 mA	-40°C to +125°C	01,02	-0.2		V
			-40°C to +85°C	03	-0.2		
			-55°C to +125°C	04	-0.2		
Hysteresis voltage 2/ (V_{IT+} - V_{IT-})	V_{hys}		+25°C	01,02, 03,04	35 typical		mV
Enable input clamp voltage	V_{IK}	I_I = -18 mA	-40°C to +125°C	01,02	-1.5		V
			-40°C to +85°C	03	-1.5		
			-55°C to +125°C	04	-1.5		
High level output voltage	V_{OH}	V_{ID} = 200 mV, I_{OH} = -8 mA, see figure 11	-40°C to +125°C	01,02	2.4		V
			-40°C to +85°C	03	2.4		
			-55°C to +125°C	04	2.4		
Low level output voltage	V_{OL}	V_{ID} = -200 mV, I_{OH} = 8 mA, see figure 11	-40°C to +125°C	01,02		0.4	V
			-40°C to +85°C	03		0.4	
			-55°C to +125°C	04		0.4	
High impedance state output current	I_{OZ}	V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}	-40°C to +125°C	01,02	-1	1	µA
			-40°C to +85°C	03	-1	1	
			-55°C to +125°C	04	-1	1	

See footnotes at end of Receiver electrical characteristics section.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics section – continued.							
Bus input current	I_I	V_A or V_B = 12 V, other input at 0 V	-40°C to +125°C	01		0.5	mA
		V_A or V_B = 12 V, V_{CC} = 0 V, other input at 0 V				0.5	
		V_A or V_B = -7 V, other input at 0 V			-0.4		
		V_A or V_B = -7 V, V_{CC} = 0 V, other input at 0 V			-0.4		
		V_A or V_B = 12 V, other input at 0 V	-40°C to +125°C	02		0.11	
			-40°C to +85°C	03		0.11	
		V_A or V_B = 12 V, V_{CC} = 0 V, other input at 0 V	-40°C to +125°C	02		0.13	
			-40°C to +85°C	03		0.13	
		V_A or V_B = -7 V, other input at 0 V	-40°C to +125°C	02	-0.1		
			-40°C to +85°C	03	-0.1		
		V_A or V_B = -7 V, V_{CC} = 0 V, other input at 0 V	-40°C to +125°C	02	-0.05		
			-40°C to +85°C	03	-0.05		
		V_A or V_B = 12 V, other input at 0 V	-55°C to +125°C	04		0.5	
		V_A or V_B = 12 V, V_{CC} = 0 V, other input at 0 V				0.5	
		V_A or V_B = -7 V, other input at 0 V			-0.4		
		V_A or V_B = -7 V, V_{CC} = 0 V, other input at 0 V			-0.4		

See footnotes at end of Receiver electrical characteristics section.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics section - continued.							
High level input current, $\overline{RE}$	I_{IH}	V_{IH} = 2 V	-40°C to +125°C	01,02	-30	0	µA
			-40°C to +85°C	03	-30	0	
			-55°C to +125°C	04	-30	0	
Low level input current, $\overline{RE}$	I_{IL}	V_{IL} = 0.8 V	-40°C to +125°C	01,02	-30	0	µA
			-40°C to +85°C	03	-30	0	
			-55°C to +125°C	04	-30	0	
Differential input capacitance	$C_{(ID)}$	V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V	+25°C	01,02, 03,04	15 typical 2/		pF
Supply current	I_{CC}	$\overline{RE}$ at 0 V, D and DE at 0 V, no load, receiver enabled and driver disabled	-40°C to +125°C	01,02		8	mA
			-40°C to +85°C	03		8	
			-55°C to +125°C	04		8	
		$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, no load, receiver disabled and driver disabled (standby)	-40°C to +125°C	01,02		5	µA
			-40°C to +85°C	03		5	
			-55°C to +125°C	04		5	
		$\overline{RE}$ at 0 V, D and DE at V_{CC}, no load, receiver enabled and driver enabled	-40°C to +125°C	01,02		15.5	mA
			-40°C to +85°C	03		15.5	
			-55°C to +125°C	04		15.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All typical values are at 25°C and with a 3.3 V supply.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver switching characteristics section.							
Propagation delay time, low to high level output	t_{PLH}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 12	-40°C to +125°C	01	12.5	25	ns
			-55°C to +125°C	04	12.5	25	
Propagation delay time, high to low level output	t_{PHL}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 12	-40°C to +125°C	01	12.5	25	ns
			-55°C to +125°C	04	12.5	25	
Propagation delay time, low to high level output	t_{PLH}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 12	-40°C to +125°C	02	30	70	ns
			-40°C to +85°C	03	30	70	
Propagation delay time, high to low level output	t_{PHL}	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 12	-40°C to +125°C	02	30	70	ns
			-40°C to +85°C	03	30	70	
Pulse skew ($t_{PHL} – t_{PLH}$)	$t_{sk(p)}$	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, see figure 12	-40°C to +125°C	01		1.5	ns
			-40°C to +125°C	02		4	
			-40°C to +85°C	03		4	
			-55°C to +125°C	04		1.5	
Part to part skew 2/	$t_{sk(pp)}$		-40°C to +125°C	01		8	ns
			-40°C to +125°C	02		15	
			-40°C to +85°C	03		15	
			-55°C to +125°C	04		8	
Output signal rise time	t_r	C_L = 15 pF, see figure 12	-40°C to +125°C	01,02	1	6	ns
			-40°C to +85°C	03	1	6	
			-55°C to +125°C	04	1	6	
Output signal fall time	t_f	C_L = 15 pF, see figure 12	-40°C to +125°C	01,02	1	6	ns
			-40°C to +85°C	03	1	6	
			-55°C to +125°C	04	1	6	

See footnotes at end of Receiver switching characteristics section.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver switching characteristics section - continued.							
Output enable time to high level	t_{PZH}	C_L = 15 pF, DE at 3 V, see figure 13	-40°C to +125°C	01,02		16	ns
			-40°C to +85°C	03		16	
			-55°C to +125°C	04		16	
Output enable time to low level	t_{PZL}	C_L = 15 pF, DE at 3 V, see figure 13	-40°C to +125°C	01,02		16	ns
			-40°C to +85°C	03		16	
			-55°C to +125°C	04		16	
Output disable time from high level	t_{PHZ}	C_L = 15 pF, DE at 3 V, see figure 13	-40°C to +125°C	01,02		21	ns
			-40°C to +85°C	03		21	
			-55°C to +125°C	04		21	
Output disable time from low level	t_{PLZ}	C_L = 15 pF, DE at 3 V, see figure 13	-40°C to +125°C	01,02		16	ns
			-40°C to +85°C	03		16	
			-55°C to +125°C	04		16	
Propagation delay time, standby to high level output	t_{PZH}	C_L = 15 pF, DE at 0 V, see figure 14	-40°C to +125°C	01,02		6	µs
			-40°C to +85°C	03		6	
			-55°C to +125°C	04		14	
Propagation delay time, standby to low level output	t_{PZL}	C_L = 15 pF, DE at 0 V, see figure 14	-40°C to +125°C	01,02		6	µs
			-40°C to +85°C	03		6	
			-55°C to +125°C	04		14	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Case X

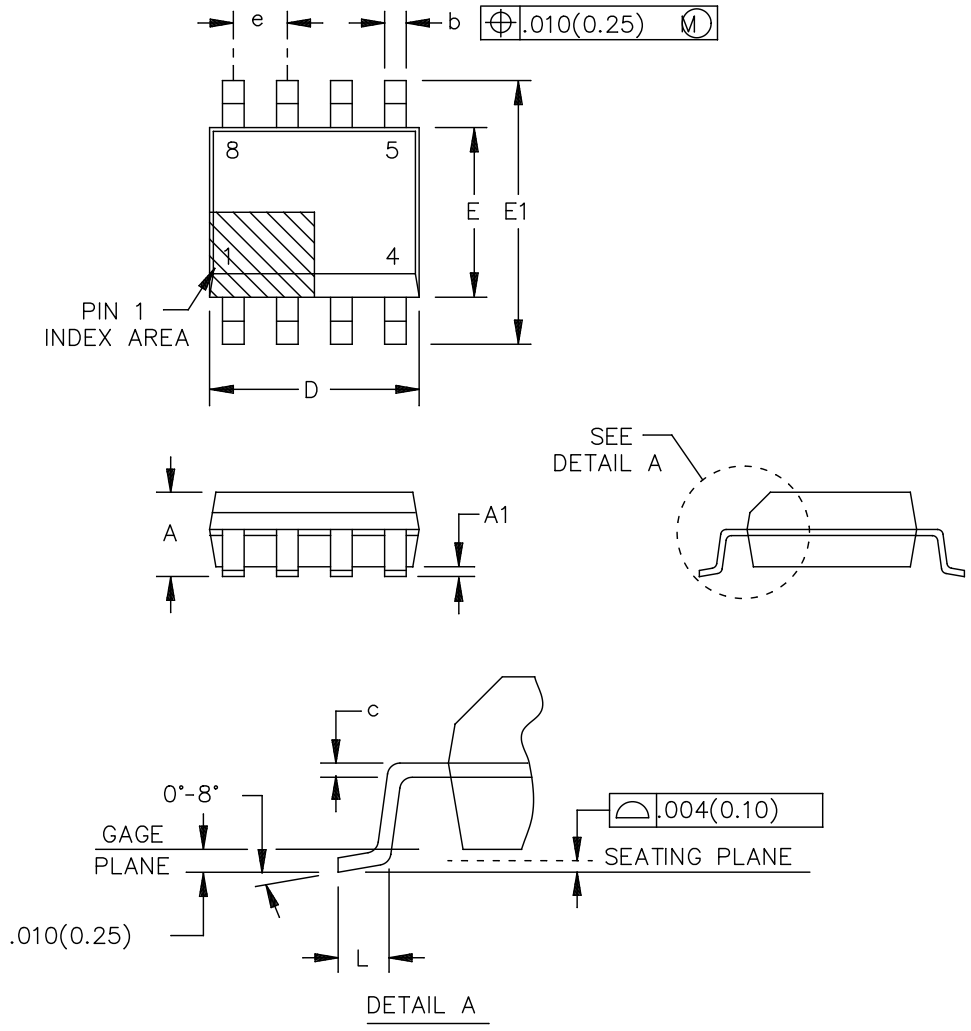


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
n	8 leads		8 leads	

NOTE:
1. All linear dimensions are in inches. Millimeter dimensions are given for information only.
2. This drawing is subject to change without notice.
3. Dimension D body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed .006 inch (0.15 mm) per end.
4. Dimension E body width does not include interlead flash.
5. Falls within JEDEC MS-012 variation AA.

FIGURE 1. Case outline. – continued.

Device types	01,02,03,04	
Case outline	X	
Terminal number	Terminal symbol	Description
1	R	Receiver output.
2	$\overline{RE}$	Receiver enable.
3	DE	Driver enable.
4	D	Driver input.
5	GND	Ground.
6	A	Driver output A.
7	B	Driver output B.
8	V_{CC}	Supply voltage.

FIGURE 2. Terminal connections.

DRIVER

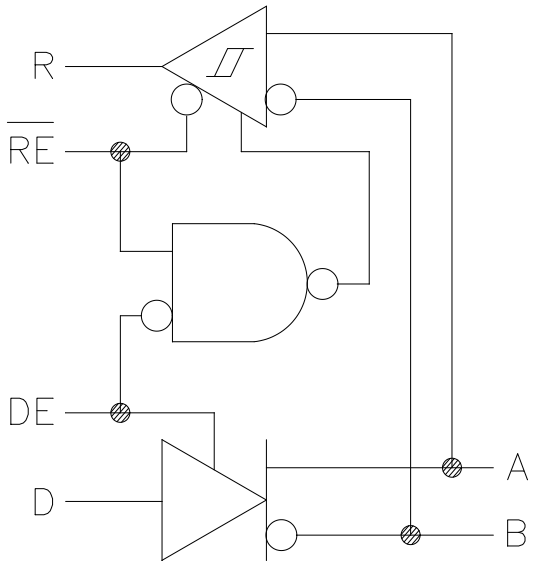
INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \leq -0.2$ V	L	L
$-0.2 \text{ V} < V_{ID} < -0.01$ V	L	?
$-0.01 \text{ V} \leq V_{ID}$	L	H
X	H	Z
Open circuit	L	H
Short circuit	L	H

H = high level
L = low level
Z = high impedance
X = irrelevant
? = indeterminate

FIGURE 3. Truth tables.



LOGIC DIAGRAM
(POSITIVE LOGIC)

FIGURE 4. Logic diagram.

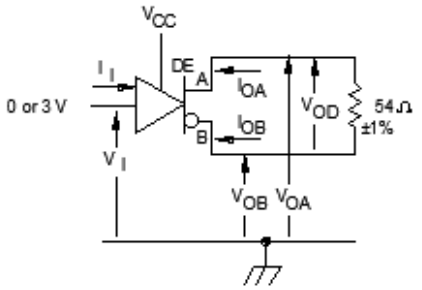


FIGURE 5. DRIVER V_{OD} TEST CIRCUIT AND VOLTAGE AND CURRENT DEFINITIONS

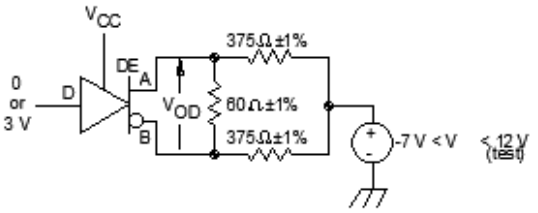
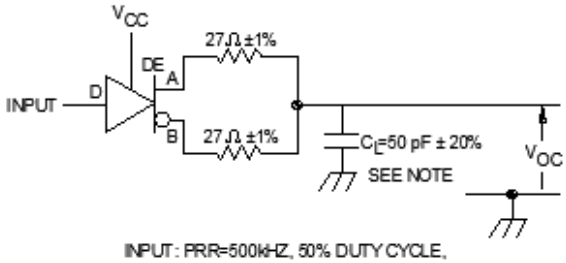
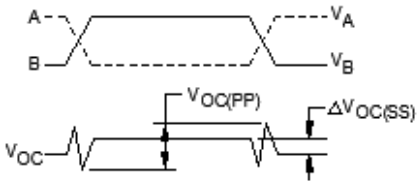


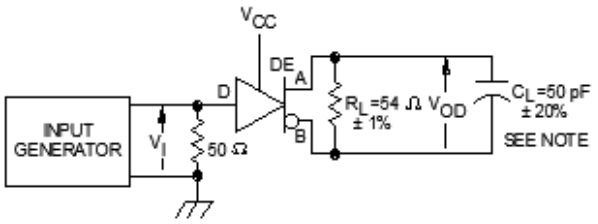
FIGURE 6. DRIVER V_{OD} WITH COMMON-MODE LOADING TEST CIRCUIT

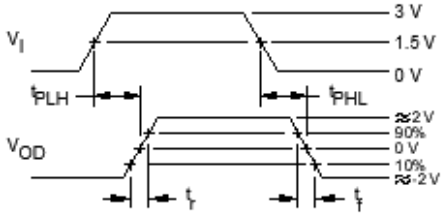




INPUT: PRR=500kHZ, 50% DUTY CYCLE,
t_r < 6 ns, t_f < 6 ns, Z_o = 50Ω

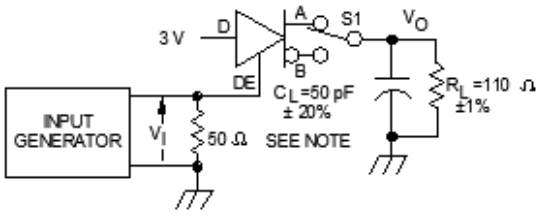
FIGURE 7. TEST CIRCUIT AND DEFINITIONS FOR THE DRIVER COMMON-MODE OUTPUT VOLTAGE

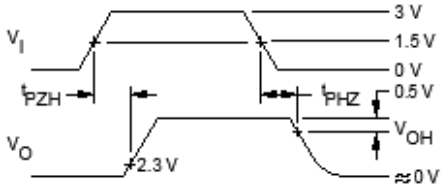




GENERATOR: PRR=500kHZ, 50% DUTY CYCLE,
t_r < 6 ns, t_f < 6 ns, Z_o = 50Ω

FIGURE 8. DRIVER SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS



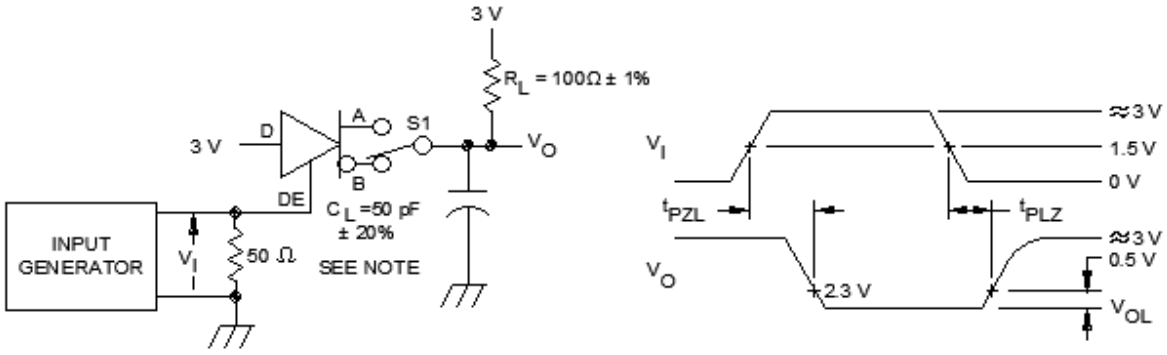


GENERATOR: PRR=500kHZ, 50% DUTY CYCLE,
t_r < 6 ns, t_f < 6 ns, Z_o = 50Ω

FIGURE 9. DRIVER HIGH-LEVEL ENABLE AND DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

NOTE: C_L includes fixture and instrumentation capacitance.

FIGURES 5 through 9. Timing waveforms and test circuit.



GENERATOR: PRR=500kHZ, 50% DUTY CYCLE,
t_r < 6 ns, t_f < 6 ns, Z_O = 50Ω

FIGURE 10. DRIVER LOW-LEVEL OUTPUT ENABLE AND DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

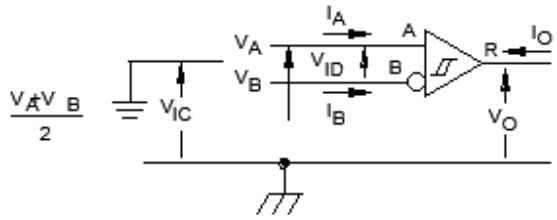
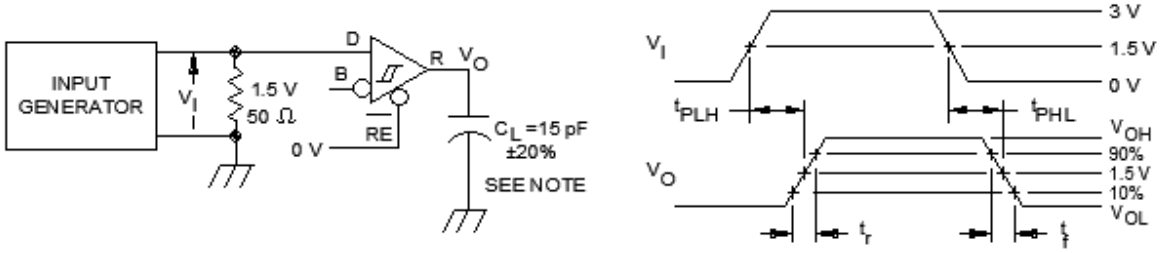


FIGURE 11. RECEIVER VOLTAGE AND CURRENT DEFINITIONS

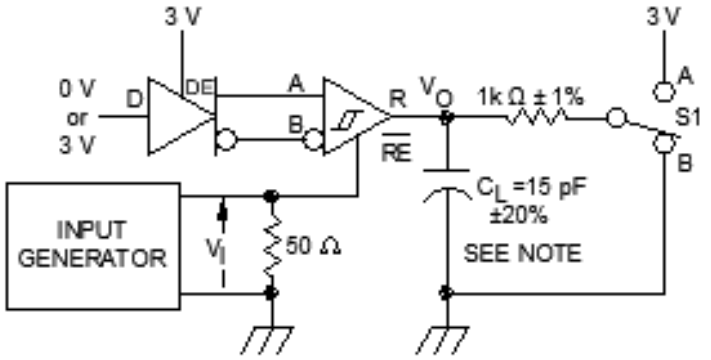


GENERATOR: PRR=500kHZ, 50% DUTY CYCLE,
t_r < 6 ns, t_f < 6 ns, Z_O = 50Ω

FIGURE 12. RECEIVER SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

NOTE: C_L includes fixture and instrumentation capacitance.

FIGURES 10 through 12. Timing waveforms and test circuit – Continued.



GENERATOR: PRR=500kHZ, 50% DUTY CYCLE, t_r < 6 ns, t_f < 6 ns, Z_O = 50Ω

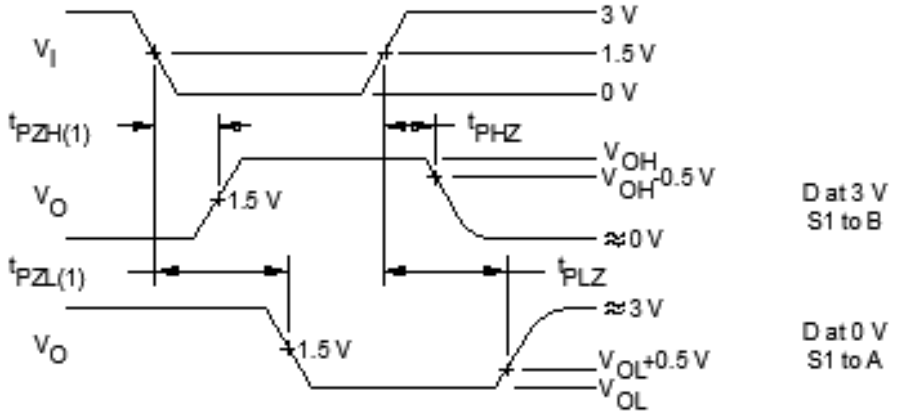
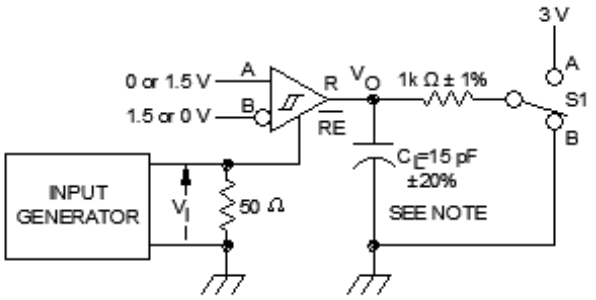


FIGURE 13. RECEIVER ENABLE AND DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS WITH DRIVER ENABLED

NOTE: C_L includes fixture and instrumentation capacitance.

FIGURE 13. Timing waveforms and test circuit – Continued.



GENERATOR: PRR=500kHZ, 50% DUTY CYCLE, t_r < 6 ns, t_f < 6 ns, Z_O = 50Ω

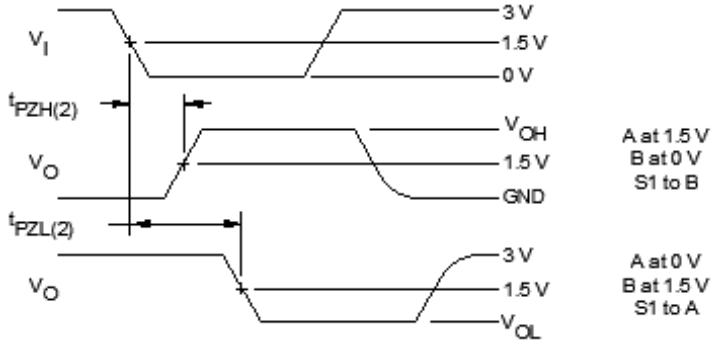


FIGURE 14. RECEIVER ENABLE TIME FROM STANDBY (DRIVER DISABLE)

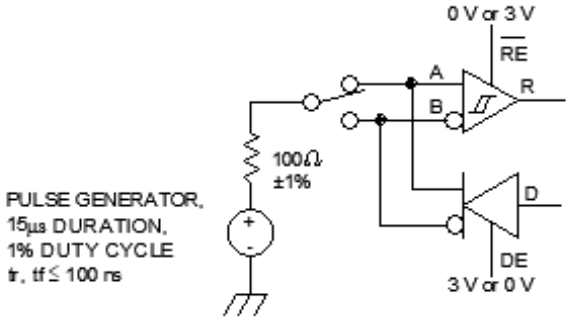


FIGURE 15. TEST CIRCUIT, TRANSIENT OVER VOLTAGE TEST

The transient over voltage test is conducted to test survivability only. Data stability at the R output is not specified.

NOTE: C_L includes fixture and instrumentation capacitance.

FIGURES 14 through 15. Timing waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Signaling rate	Unit loads	Vendor part number 2/	SOIC marking
V62/05604-01XE	01295	25 Mbps	1/2	SN65HVD10QDREP	V10QEP
V62/05604-02XA	3/	10 Mbps	1/8	SN65HVD11QDREP	V11QEP
V62/05604-03XE	01295	1 Mbps	1/8	SN65HVD12IDREP	V12IEP
V62/05604-04XE	01295	25 Mbps	1/2	SN65HVD10MDREP	V10MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ The D package is taped and reeled as indicated by the R suffix to the part number (for example SN65HVD10QDREP).
3/ No source currently available.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243