REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add case outline “Z”. - CFS	05-08-26	Thomas M. Hess
B	Update boilerplate paragraphs to current MIL-PRF-3853 requirements. - PHN	13-12-11	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-01-19	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C				
PAGE	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
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REV STATUS OF PAGES	**REV**	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 05-03-23	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL SIGNAL PROCESSORS, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/05601
	REV C	**PAGE** 1 **OF** 58

AMSC N/A

5962-V022-21

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance floating-point digital signal processor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/05601	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device type	Generic	Circuit function
01	SM320F2810-EP	Digital Signal Processors
02	SM320F2811-EP	Digital Signal Processors
03	SM320F2812-EP	Digital Signal Processors
04	SM320C2810-EP	Digital Signal Processors
05	SM320C2811-EP	Digital Signal Processors
06	SM320C2812-EP	Digital Signal Processors

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	179		Plastic ball grid array
Z	176	JEDEC MS-026	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

1.3 Absolute maximum ratings. 2/

Supply voltage ranges, (V_{DDIO}, V_{DDA1}, V_{DDA2}, V_{DDAIO}, $AV_{DDREFBG}$)	-0.3 V to +4.6 V
Supply voltage ranges, (V_{SSA1}/V_{SSA2} to V_{DDA1}/ V_{DDA2}/ $AV_{DDREFBG}$)	-0.3 V to +4.6 V
V_{SS1} to V_{DD1}	-0.3 V to +2.5 V
Supply voltage ranges, (V_{DD}, V_{DD1})	-0.5 V to +2.5 V
V_{DD3VFL} range	-0.3 V to +4.6 V
Input voltage range, (V_{IN})	-0.3 V to +4.6 V
Output voltage range, (V_O)	-0.3 V to +4.6 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})	±20 mA 3/
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})	±20 mA
Analog input (ADCIN) clamp current, total (max)	±20 mA 4/
Operating ambient temperature ranges, (T_A : M version (GHH))	-55°C to +125°C
Storage temperature range, (T_{STG})	-65°C to +150°C 5/

1.4 Recommended operating conditions.

Device supply voltage, I/O, (V_{DDIO})	+3.14 V to +3.47 V
Device supply voltage, CPU (V_{DD}, V_{DD1}):	
1.8 V (135 MHz)	+1.71 V to 1.89 V
1.9 V (150 MHz)	+1.81 to +2.0 V
Supply ground, (V_{SS})	0 V
ADC supply voltage ($V_{DDA!}$, V_{DDA2}, $AV_{DDREFBG}$, V_{DDAIO})	+3.14 V to +3.47 V
Flash programming supply voltage, (V_{DD3VFL})	+3.14 V to +3.47 V
Device clock frequency (system clock), ($f_{SYSCLKOUT}$) :	
V_{DD} = 1.9 V ± 5%	2 MHz to 150 MHz
V_{DD} = 1.8 V ± 5%	2 MHz to 135 MHz
High level input voltage, (V_{IH}) :	
All inputs except XCLKIN	+2.0 V to V_{DDIO}
XCLKIN (@ 50 μA max)	+0.7V_{DD} to V_{DD}
Maximum low level input voltage, (V_{IL}) :	
All inputs except XCLKIN	+0.8 V
XCLKIN (@ 50 μA max)	+0.3V_{DD}
Maximum high level output source current, V_{OH} = 2.4 V (I_{OH}) :	
All I/Os except group 2	-4 mA
Group 2 6/	-8 mA
Maximum low level output sink current, V_{OL} = V_{OL} max (I_{OL}) :	
All I/Os except group 2	4 mA
Group 2 6/	8 mA
Ambient temperature, (M version,) (See figure 4 and figure 5)	-55°C to +125°C

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/ Continuous clamp current per pin is ±2 mA.

4/ The analog inputs have an internal clamping circuit that clamps the voltage to a diode drop above V_{DDA} or below V_{SS}. The continuous clamp current per pin is ±2 mA.

5/ Long term high temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life.

6/ Group 2 pins are as follows: XINTF pins, $\overline{\text{PDPINTA}}$, TDO, XCLOUT, XF, ENU0, and EMU1.

1.5 Recommended operating conditions - Continued.

Thermal resistance characteristics:

Parameter	Case X	Uniit
P_{sJT}	0.658	°C/W
θ_{JA}	42.57	°C/W
θ_{JC}	16.08	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https:/www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 FIT rate versus operating junction temperature. The FIT rate versus operating junction temperature shall be as specified in figure 4.

3.5.5 Package life time versus operating junction temperature. The package life time versus operating junction temperature shall be as specified in figure 5.

3.5.6 Current consumption graphs. The current consumption graphs shall be as specified in figure 6.

3.5.7 Test load circuits. The test load circuits shall be as specified in figure 7.

3.5.8 Timing waveforms. The timing waveforms shall be as shown in figure 8- 42.

TABLE I. Electrical performance characteristics. 1/

No	Test		Symbol	Test condition 2/		Limits		Unit
						Min	Max	
	High level output voltage		V_{OH}	$I_{OH} = I_{OH\ max}$		2.4		V
				I_{OH} = 50 µA		V_{DDIO} – 0.2		
	Low level output voltage		V_{OL}	$I_{OL} = I_{OL\ max}$			0.4	V
	Low level input current	With pull up	I_{IL}	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os 3/ (including $\overline{XRS}$) except EVB	-80	-190	µA
					GPIOB/EVB	-13	-35	
		With pull down		V_{DDIO} = 3.3 V, V_{IN} = 0 V			±2	
	High level input current	With pull up	I_{IH}	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$			±2	µA
		With pull down				28	80	
	Off state output current, high impedance state (off state)		I_{OZ}	$V_O = V_{DDIO}$ or 0 V			±2	µA
	Input capacitance		C_i			2 Typ		pF
	Output capacitance		C_O			3 Typ		pF
Input clock frequency								
	Input clock frequency		f_x	Resonator		20	35	MHz
				Crystal		20	35	
				XCLKIN		4	150	
	Limp mode clock frequency		f_l			2 Typ		MHz
XCLKIN timing requirements – PLL bypassed or Enabled								
C8	Cycle time, XCLKIN		$t_{c(CI)}$	See figure 8		6.67	250	ns
C9	Fall time, XCLKIN		$t_{f(CI)}$		Up to 30 MHz		6	
					30 MHz to 150 MHz		2	
C10	Rise time, XCLKIN		$t_{r(CI)}$		Up to 30 MHz		6	
					30 MHz to 150 MHz		2	
C11	Pulse duration, X1/XCLKIN low as a percentage of $t_{c(CI)}$		$t_{w(CIL)}$			40	60	%
C12	Pulse duration, X1/XCLKIN high as a percentage of $t_{c(CI)}$		$t_{w(CIH)}$			40	60	
XCLKIN timing requirements – PLL disabled								
C8	Cycle time, XCLKIN		$t_{c(CI)}$	See figure 8		6.67	250	ns
C9	Fall time, XCLKIN		$t_{f(CI)}$		Up to 30 MHz		6	
					30 MHz to 150 MHz		2	
C10	Rise time, XCLKIN		$t_{r(CI)}$		Up to 30 MHz		6	
					30 MHz to 150 MHz		2	
C11	Pulse duration, X1/XCLKIN low as a percentage of $t_{c(CI)}$		$t_{w(CIL)}$		XCLKIN ≤ 120 MHz	40	60	%
					120 < XCLKIN ≤ 150 MHz	45	55	
C12	Pulse duration, X1/XCLKIN high as a percentage of $t_{c(CI)}$		$t_{w(CIH)}$		XCLKIN ≤ 120 MHz	40	60	
					120 < XCLKIN ≤ 150 MHz	45	55	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits		Unit
				Min	Max	
	OUTPUT CLOCK CHARACTERISTICS					
	XCLKOUT switching characteristics (PLL bypassed or enabled) 3/ 4/					
C1	Cycle time, XCLKOUT	$t_{c(XCO)}$	See figure 8	6.67 5/		ns
C3	Fall time, XCLKOUT	$t_{f(XCO)}$		2 Typ		
C4	Rise time, XCLKOUT	$t_{r(XCO)}$		2 Typ		
C5	Pulse duration, XCLKOUT low	$t_{w(XCOL)}$		H-2	H+2	
C6	Pulse duration, XCLKOUT high	$t_{w(XCOH)}$		H-2	H+2	
C7	PLL lock time 6/	t_p			$131072t_{c(CI)}$	
	RESET TIMING					
	Reset ($\overline{XRS}$) timing requirements 7/					
	Pulse duration, stable XCLKIN to $\overline{XRS}$ high	$t_{w(RSL1)}$	See figure 9-12	$8t_{c(CI)}$		cycles
	Pulse duration, $\overline{XRS}$ low — Warm reset	$t_{w(RSL2)}$		$8t_{c(CI)}$		
	Pulse duration, $\overline{XRS}$ low — WD-initiated reset	$t_{w(RSL2)}$		$512t_{c(CI)}$ Typ		
	Pulse duration, reset pulse generated by watchdog	$t_{w(WDRS)}$		$512t_{c(CI)}$ Typ		
	Delay time, address/data valid after $\overline{XRS}$ high	$t_{d(EX)}$		$32t_{c(CI)}$ Typ		
	Oscillator start-up time	t_{OSCT} 8/		1		ms
	Setup time for $\overline{XPLLDIS}$ pin	$t_{su(XPLLDIS)}$		$16t_{c(CI)}$		cycles
	Hold time for $\overline{XPLLDIS}$ pin	$t_{h(XPLLDIS)}$		$16t_{c(CI)}$		
	Hold time for XMP/$\overline{MC}$ pin	$t_{h(XMP/MC)}$		$16t_{c(CI)}$		
	Hold time for boot mode pins	$t_{h(boot\text{-}mode)}$		$2520t_{c(CI)}$ 9/		
	LOW POWER MODE WAKEUP TIMING					
	IDLE mode switching characteristics (See figure 13)					
	Pulse duration, external wake up signal	$t_{w(WAKE\text{-}INT)}$	Without input qualifier	$2*t_{c(SCO)}$		cycles
			With input qualifier	$1*t_{c(SCO)}$+IQT 10/		
	Delay time, external wake signal to program execution resume 11/	$t_{d(WAKE\text{-}INT)}$				
	- Wake up from Flash - Flash module in active state		Without input qualifier	$8*t_{c(SCO)}$		
	- Wake up from Flash - Flash module in active state		With input qualifier	$8*t_{c(SCO)}$+IQT 10/		
	- Wake up from Flash - Flash module in sleep state		Without input qualifier	$1050*t_{c(SCO)}$		
	- Wake up from Flash - Flash module in sleep state		With input qualifier	$1050*t_{c(SCO)}$+IQT 10/		
	- Wake up from SARAM		Without input qualifier	$8*t_{c(SCO)}$		
	- Wake up from SARAM		With input qualifier	$8*t_{c(SCO)}$+IQT 10/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
LOW POWER MODE WAKEUP TIMING					
Standby mode switching characteristics (See figure 14)					
Delay time, IDLE instruction executed to XCLKOUT high	$t_{d(IDLE-XCOH)}$		$32*t_{c(SCO)}$		cycles
Pulse duration, external wake up signal	$t_{w(WAKE-INT)}$	Without input qualifier	$12*t_{c(CI)}$		
		With input qualifier	$(2+QUALSTDBY)*t_{c(CI)}$ 12/		
Delay time, external wake signal to program execution resume 11/	$t_{d(WAKE-STBY)}$				
- Wake up from Flash - Flash module in active state		Without input qualifier	$12*t_{c(CI)}$		
- Wake up from Flash - Flash module in active state		With input qualifier	$12*t_{c(CI)} + t_{w(WAKE-INT)}$		
- Wake up from Flash - Flash module in sleep state		Without input qualifier	$1125*t_{c(SCO)}$		
- Wake up from Flash - Flash module in sleep state		With input qualifier	$1125*t_{c(SCO)}+t_{w(WAKE-INT)}$		
- Wake up from SARAM		Without input qualifier	$12*t_{c(CI)}$		
- Wake up from SARAM		With input qualifier	$12*t_{c(CI)} + t_{w(WAKE-INT)}$		
HALT mode switching characteristics					
Delay time, IDLE instruction executed to XCLKOUT high	$t_{d(IDLE-XCOH)}$	See figure 15	$32*t_{c(SCO)}$		cycles
Pulse duration, XNMI wakeup signal	$t_{w(WAKE-XNMI)}$		$2*t_{c(CI)}$		
Pulse duration, $\overline{XRS}$ wake up signal	$t_{w(WAKE-XRS)}$		$8*t_{c(CI)}$		
PLL lock up time	t_p			$131072*t_{c(CI)}$	
Delay time, PLL lock to program execution resume	$t_{d(WAKE)}$				
- Wake up from flash - Flash module in sleep state			$1125*t_{c(SCO)}$		
- Wake-up from SARAM			$35*t_{c(SCO)}$		
PWM timing					
PWM switching characteristics 13/ 14/ (See figure 16)					
Pulse duration, PWMx output high/low	$t_{w(PWM)}$ 15/		25		ns
Delay time, XCLKOUT high to PWMx output switching	$t_{d(PWM)XCO}$	XCLKOUT = SYSCLKOUT/4		10	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
PWM timing – Continued					
Time and Capture unit timing requirements 16/ 17/ (See figure 17)					
Pulse duration, TDIRx low/high	$t_{w(TDIR)}$	Without input qualified	$2*t_{c(SCO)}$		cycles
		With input qualified	$1*t_{c(SCO)}$+ IQT 18/		
Pulse duration, CAPx input low/high	$t_{w(CAP)}$	Without input qualified	$2*t_{c(SCO)}$		
		With input qualified	$1*t_{c(SCO)}$+ IQT 18/		
Pulse duration, TCLKINx low as a percentage of TCLKINx cycle time	$t_{w(TCLKINL)}$		40	60	%
Pulse duration, TCLKINx high as a percentage of TCLKINx cycle time	$t_{w(TCLKINH)}$		40	60	
Cycle time, TCLKINx	$t_{c(TCLKIN)}$		$4*t_{c(HCO)}$		ns
External ADC start of conversion – EVA – Switching characteristics 19/ (See figure 18)					
Delay time, XCLKOUT high to $\overline{\text{EVASOC}}$ low	$t_{d(XCOH-EVASOCL)}$			$1*t_{c(SCO)}$	cycle
Pulse duration, $\overline{\text{EVASOC}}$ low	$t_{w(EVASOCL)}$		$32*t_{c(HCO)}$		ns
External ADC start of conversion – EVB – Switching characteristics 19/ (See figure 19)					
Delay time, XCLKOUT high to $\overline{\text{EVBSOC}}$ low	$t_{d(XCOH-EVBSOCL)}$			$1*t_{c(SCO)}$	cycle
Pulse duration, $\overline{\text{EVBSOC}}$ low	$t_{w(EVBSOCL)}$		$32*t_{c(HCO)}$		ns
INTERRUPT TIMING					
Interrupt switching characteristics					
Delay time, $\overline{\text{PDPINTx}}$ low to PWM high impedance state	$t_{d(PDP-PWM)HZ}$	Without input qualified		12	ns
		With input qualified		$1*t_{c(SCO)}$+IQT+ 12 18/	
Delay time, $\overline{\text{CxTRIP}}$ / $\overline{\text{TxCTRIP}}$ signal low to PWM high impedance state	$t_{d(TRIP-PWM)HZ}$	Without input qualified		$3*t_{c(SCO)}$	
		With input qualified		$[2*t_{c(SCO)}]$+IQT 18/	
Delay time, INT low/high to interrupt vector fetch	$t_{d(INT)}$		t_{qual}+12 $t_{c(XCO)}$		
Interrupt timing requirements (see figure 20)					
Pulse duration, INT input low/high	$t_{w(INT)}$	With no qualifier	$2*t_{c(SCO)}$		cycles
		With qualifier	$1*t_{c(SCO)}$+IQT 18/		
Plus duration, $\overline{\text{PDPINTx}}$ input low	$t_{w(PDP)}$	With no qualifier	$2*t_{c(SCO)}$		
		With qualifier	$1*t_{c(SCO)}$+IQT 18/		
Plus duration, $\overline{\text{CxTRIP}}$ input low	$t_{w(CxTRIP)}$	With no qualifier	$2*t_{c(SCO)}$		
		With qualifier	$1*t_{c(SCO)}$+IQT 18/		
Plus duration, $\overline{\text{TxCTRIP}}$ input low	$t_{w(TxCTRIP)}$	With no qualifier	$2*t_{c(SCO)}$		
		With qualifier	$1*t_{c(SCO)}$+IQT 18/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/		Limits		Unit
				Min	Max	
GENERAL PURPOSE INPUT/OUTPUT (GPIO) – OUTPUT TIMING						
General purpose output switching characteristics (See figure 21)						
Delay time, XCLKOUT high to GPIO low/high	$t_{d(XCOH-GPO)}$	All GPIOs			$1*t_{c(SCO)}$	cycle
Rise time, GPIO switching low to high	$t_{r(GPO)}$	All GPIOs			10	ns
Fall time, GPIO switching high to low	$t_{f(GPO)}$	All GPIOs			10	
Toggling frequency, GPO pins	f_{GPO}				20	MHz
General purpose input timing requirements (See figure 22)						
Pulse duration, GPIO low/high	$t_{w(GPI)}$	All GPIOs	With no qualifier	$2*t_{c(SCO)}$		cycles
			With qualifier	$1*t_{c(SCO)}$+IQT 18/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				Min	Max	Min	Max	
SPI MASTER MODE TIMING								
SPI master mode external timing (clock phase = 0) 20/ 21/				SPI when (SPIBRR+1) is even or SPIBRR = 0 or 2		SPI when (SPIBRR+1) is odd and SPIBRR > 3		
1	Cycle time, SPICLK	$t_{c(SPC)M}$	See figure 23	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2 22/	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$		23/	24/	26/	27/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$		23/	24/	26/	27/	
3 22/	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$		23/	24/	28/	29/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$		23/	24/	28/	29/	
4 22/	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)	$t_{d(SPCH-SIMO)M}$		-10	-10	-10	-10	
	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)	$t_{d(SPCL-SIMO)M}$		-10	-10	-10	-10	
5 22/	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)M}$		23/		28/		
	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)M}$		23/		28/		
8 22/	Setup time, SPIOMI before SPICLK low (clock polarity = 0)	$t_{su(SOMI-SPCL)M}$		0		0		
	Setup time, SPIOMI before SPICLK high (clock polarity = 1)	$t_{su(SOMI-SPCH)M}$		0		0		
9 22/	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SOMI)M}$		25/		26/		
	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCH-SOMI)M}$		25/		26/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				Min	Max	Min	Max	
SPI MASTER MODE TIMING - Continued								
SPI master mode external timing (clock phase = 1) 20/ 21/				SPI when (SPIBRR+1) is even or SPIBRR = 0 or 2		SPI when (SPIBRR+1) is odd and SPIBRR > 3		
1	Cycle time, SPICLK	$t_{c(SPC)M}$	See figure 24	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2 22/	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$		23/	24/	26/	27/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$		23/	24/	26/	27/	
3 22/	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$		23/	24/	28/	29/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$		23/	24/	28/	29/	
6 22/	Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$t_{su(SIMO-SPCH)M}$		23/		23/		
	Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$t_{su(SIMO-SPCL)M}$		23/		23/		
7 22/	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SIMO)M}$		23/		23/		
	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCL-SIMO)M}$		23/		23/		
10 22/	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{su(SOMI-SPCH)M}$		0		0		
	Setup time, SPIOMI before SPICLK low (clock polarity = 1)	$t_{su(SOMI-SPCL)M}$		0		0		
11 22/	Valid time, SPISOMI data valid after SPICLK high(clock polarity = 0)	$t_{v(SPCH-SOMI)M}$		25/		23/		
	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SOMI)M}$		25/		23/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/		Limits		Unit
					Min	Max	
SPI SLAVE MODE TIMING							
SPI slave mode external timing (clock phase = 0) 20/ 21/							
12	Cycle time, SPICLK	$t_{c(SPC)S}$	See figure 25		$5t_{c(LCO)}$ 21/		ns
13 22/	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$			30/	31/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$			30/	31/	
14 22/	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$			30/	31/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$			30/	31/	
15 22/	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)	$t_{d(SPCH-SOMI)S}$			32/		
	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)	$t_{d(SPCL-SOMI)S}$			32/		
16 22/	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCH-SOMI)S}$			33/		
	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCL-SOMI)S}$			33/		
19 22/	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{su(SIMO-SPCL)S}$			0		
	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{su(SIMO-SPCH)S}$			0		
20 22/	Valid time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)S}$			31/		
	Valid time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)S}$			31/		
SPI slave mode external timing (clock phase = 1) 20/ 21/							
12	Cycle time, SPICLK	$t_{c(SPC)S}$	See figure 26		$8t_{c(LCO)}$		ns
13 22/	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$			30/	31/	
	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$			30/	31/	
14 22/	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$			30/	31/	
	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$			30/	31/	
17 22/	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{su(SOMI-SPCH)S}$			34/		
	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$t_{su(SOMI-SPCL)S}$			34/		
18 22/	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SOMI)S}$			33/		
	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SOMI)S}$			33/		
21 22/	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	$t_{su(SIMO-SPCH)S}$			0		
	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	$t_{su(SIMO-SPCL)S}$			0		
22 22/	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SIMO)S}$			31/		
	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SIMO)S}$			31/		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
EXTERNAL INTERFACE READ TIMING					
External memory interface Read switching characteristics					
Delay time, XCLOUT high to zone chip select active low	$t_{d(XCOH-XZCSL)}$	See figure 27		1	ns
Delay time, XCLOUT high/low to zone chip select inactive high	$t_{d(XCOHL-XZCSH)}$		-2	3	
Delay time, XCLOUT high to address valid	$t_{d(XCOH-XA)}$			2	
Delay time, XCLOUT high/low to $\overline{XRD}$ active low	$t_{d(XCOHL-XRDL)}$			1	
Delay time, XCLOUT high/low to $\overline{XRD}$ inactive high	$t_{d(XCOHL-XRDH)}$		-2	1	
Hold time, address valid after zone chip select inactive high	$t_{h(XA)XZCSH}$		35/		
Hold time, address valid after $\overline{XRD}$ inactive high	$t_{h(XA)XRD}$		35/		
External memory interface Read timing requirements					
Access time, read data from address valid	$t_{a(A)}$	See figure 27		(LR+AR)-14 36/	ns
Access time, read data valid from $\overline{XRD}$ active low	$t_{a(XRD)}$			AR-12 36/	
Setup time, read data valid before $\overline{XRD}$ strobe inactive high	$t_{su(XD)XRD}$		12		
Hold time, read data valid after $\overline{XRD}$ inactive high	$t_{h(XD)XRD}$		0		
External memory interface Write switching characteristics					
Delay time, XCLOUT high to zone chip select active low	$t_{d(XCOH-XZCSL)}$	See figure 28		1	ns
Delay time, XCLOUT high or low to zone chip select inactive high	$t_{d(XCOHL-XZCSH)}$		-2	3	
Delay time, XCLOUT high to address valid	$t_{d(XCOH-XA)}$			2	
Delay time, XCLOUT high/low to $\overline{XWE}$ low	$t_{d(XCOHL-XWEL)}$			2	
Delay time, XCLOUT high/low to $\overline{XWE}$ high	$t_{d(XCOHL-XWEH)}$			2	
Delay time, XCLOUT high/low to XR/$\overline{W}$ low	$t_{d(XCOH-XRNWL)}$			1	
Delay time, XCLOUT high/low to XR/$\overline{W}$ high	$t_{d(XCOH—XRNWH)}$		-2	1	
Enable time, data bus driven from $\overline{XWE}$ low	$t_{en(XD)XWEL}$		0		
Delay time, data valid after $\overline{XWE}$ active low	$t_{d(XWEL-XD)}$			4	
Hold time, address valid after zone chip select inactive high	$t_{h(XA)XZCSH}$		35/		
Hold time, write data valid after $\overline{XWE}$ inactive high	$t_{h(XD)XWE}$		TW-2 37/		
Data bus disabled after XR/$\overline{W}$ inactive high	$t_{dis(XD)XRNW}$		4		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
EXTERNAL INTERFACE READY ON READ TIMING WITH ONE EXTERNAL WAIT STATE					
External memory interface Read switching characteristics(Ready-on-Read, 1 Wait state)					
Delay time, XCLOUT high to zone chip select active low	$t_{d(XCOH-XZCSL)}$	See figure 29		1	ns
Delay time, XCLOUT high/low to zone chip select inactive high	$t_{d(XCOHL-XZCSH)}$		-2	3	
Delay time, XCLOUT high to address valid	$t_{d(XCOH-XA)}$			2	
Delay time, XCLOUT high/low to $\overline{XRD}$ active low	$t_{d(XCOHL-XRDL)}$			1	
Delay time, XCLOUT high/low to $\overline{XRD}$ inactive high	$t_{d(XCOHL-XRDH)}$		-2	1	
Hold time, address valid after zone chip select inactive high	$t_{h(XA)XZCSH}$		35/		
Hold time, address valid after $\overline{XRD}$ inactive high	$t_{h(XA)XRD}$		35/		
External memory interface Read timing requirements (Ready-on-Read, 1 Wait state)					
Access time, read data from address valid	$t_{a(A)}$	See figure 29		(LR+AR)-14 36/	ns
Access time, read data valid from $\overline{XRD}$ active low	$t_{a(XRD)}$			AR-12 36/	
Setup time, read data valid before $\overline{XRD}$ strobe inactive high	$t_{su(XD)XRD}$		12		
Hold time, read data valid after $\overline{XRD}$ inactive high	$t_{h(XD)XRD}$		0		
Synchronous XREADY timing requirements (Ready-on-Read, 1 Wait state) 38/					
Setup time, XREADY (Synch) low before XCLKOUT high/low	$t_{su(XRDYsynchL)XCOHL}$	See figure 29	15		ns
Hold time, XREADY (Synch) low	$t_{h(XRDYsynchL}$		12		
Earliest time XREADY (Synch) can go high before the sampling XCLKOUT edge	$t_{e(XRDYsynchH)}$			3	
Setup time, XREADY (Synch) high before XCLKOUT high/low	$t_{su(XRDYsynchH)XCOHL}$		15		
Hold time, XREADY (Synch) held high after zone chip select high	$\mathbf{t_{h(XRDYsynchH)XZCSH}}$		0		
Asynchronous XREADY timing requirements (Ready-on-Read, 1 Wait state) 39/					
Setup time, XREADY (Asynch) low before XCLKOUT high/low	$t_{su(XRDYAsynchL)XCOHL}$	See figure 30	11		ns
Hold time, XREADY (Asynch) low	$t_{h(XRDYAsynchL}$		8		
Earliest time XREADY (Asynch) can go high before the sampling XCLKOUT edge	$t_{e(XRDYAsynchH)}$			3	
Setup time, XREADY (Asynch) high before XCLKOUT high/low	$t_{su(XRDYAsynchH)XCOHL}$		11		
Hold time, XREADY (Asynch) held high after zone chip select high	$\mathbf{t_{h(XRDYAsynchH)XZCSH}}$		0		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
EXTERNAL INTERFACE READY ON WRITE TIMING WITH ONE EXTERNAL WAIT STATE					
External memory interface Write switching characteristics(Ready-on-Write, 1 Wait state)					
Delay time, XCLOUT high to zone chip select active low	$t_{d(XCOH-XZCSL)}$	See figure 31		1	ns
Delay time, XCLOUT high or low to zone chip select inactive high	$t_{d(XCOHL-XZCSH)}$		-2	3	
Delay time, XCLOUT high to address valid	$t_{d(XCOH-XA)}$			2	
Delay time, XCLOUT high/low to $\overline{XWE}$ low	$t_{d(XCOHL-XWEL)}$			2	
Delay time, XCLOUT high/low to $\overline{XWE}$ high	$t_{d(XCOHL-XWEH)}$			2	
Delay time, XCLOUT high/low to XR/$\overline{W}$ low	$t_{d(XCOH-XRNWL)}$			1	
Delay time, XCLOUT high/low to XR/$\overline{W}$ high	$t_{d(XCOH—XRNWH)}$		-2	1	
Enable time, data bus driven from $\overline{XWE}$ low	$t_{en(XD)XWEL}$		0		
Delay time, data valid after $\overline{XWE}$ active low	$t_{d(XWEL-XD)}$			4	
Hold time, address valid after zone chip select inactive high	$t_{h(XA)XZCSH}$		35/		
Hold time, write data valid after $\overline{XWE}$ inactive high	$t_{h(XD)XWE}$		TW-2 37/		
Data bus disabled after XR/$\overline{W}$ inactive high	$t_{dis(XD)XRNW}$		4		
Synchronous XREADY timing requirements (Ready-on-Write, 1 Wait state) 38/					
Setup time, XREADY (Synch) low before XCLKOUT high/low	$t_{su(XRDYsynchL)XCOHL}$	See figure 31	15		ns
Hold time, XREADY (Synch) low	$t_{h(XRDYsynchL}$		12		
Earliest time XREADY (Synch) can go high before the sampling XCLKOUT edge	$t_{e(XRDYsynchH)}$			3	
Setup time, XREADY (Synch) high before XCLKOUT high/low	$t_{su(XRDYsynchH)XCOHL}$		15		
Hold time, XREADY (Synch) held high after zone chip select high	$\mathbf{t_{h(XRDYsynchH)XZCSH}}$		0		
Asynchronous XREADY timing requirements (Ready-on-Write, 1 Wait state) 39/					
Setup time, XREADY (Asynch) low before XCLKOUT high/low	$t_{su(XRDYAsynchL)XCOHL}$	See figure 32	11		ns
Hold time, XREADY (Asynch) low	$t_{h(XRDYAsynchL}$		8		
Earliest time XREADY (Asynch) can go high before the sampling XCLKOUT edge	$t_{e(XRDYAsynchH)}$			3	
Setup time, XREADY (Asynch) high before XCLKOUT high/low	$t_{su(XRDYAsynchH)XCOHL}$		11		
Hold time, XREADY (Asynch) held high after zone chip select high	$\mathbf{t_{h(XRDYAsynchH)XZCSH}}$		0		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
$\overline{\text{XHOLD}}$ / $\overline{\text{XHOLDA}}$ **TIMING**					
$\overline{\text{XHOLD}}$ / $\overline{\text{XHOLDA}}$ **timing requirements (XCLKOUT = XTIMCLK)** 40/ 41/					
Delay time, $\overline{\text{XHOLD}}$ low to Hi-Z on all address, data, and control	$t_{d(HL-HiZ)}$	See figure 33		$4t_{c(XTIM)}$	ns
Delay time, $\overline{\text{XHOLD}}$ low to $\overline{\text{XHOLDA}}$ low	$t_{d(HL-HAL)}$			$5t_{c(XTIM)}$	
Delay time, $\overline{\text{XHOLD}}$ high to $\overline{\text{XHOLDA}}$ high	$t_{d(HH-HAH)}$			$3t_{c(XTIM)}$	
Delay time, $\overline{\text{XHOLD}}$ high to bus valid	$t_{d(HH-BV)}$			$4t_{c(XTIM)}$	
$\overline{\text{XHOLD}}$ / $\overline{\text{XHOLDA}}$ **timing requirements (XCLKOUT = 1/2 XTIMCL)** 40/ 41/ 42/					
Delay time, $\overline{\text{XHOLD}}$ low to Hi-Z on all address, data, and control	$t_{d(HL-HiZ)}$	See figure 34		$4t_{c(XTIM)}+t_{c(XCO)}$	ns
Delay time, $\overline{\text{XHOLD}}$ low to $\overline{\text{XHOLDA}}$ low	$t_{d(HL-HAL)}$			$4t_{c(XTIM)}+2t_{c(XCO)}$	
Delay time, $\overline{\text{XHOLD}}$ high to $\overline{\text{XHOLDA}}$ high	$t_{d(HH-HAH)}$			$4t_{c(XTIM)}$	
Delay time, $\overline{\text{XHOLD}}$ high to bus valid	$t_{d(HH-BV)}$			$6t_{c(XTIM)}$	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/	Limits		Unit
			Min	Max	
ON CHIP ANALOG TO DIGITAL CONVERTER					
ADC electrical characteristics – DC specifications					
Resolution			12		Bits
ADC clock 44/			1		kHz
				25	MHz
Accuracy					
INL (integral nonlinearity) 45/		1- 18.75 MHz ADC clock		±1.5	LSB
DNL (Differential nonlinearity) 45/		1- 18.75 MHz ADC clock		±1	
Offset error 46/			-80	80	
Overall gain error with internal reference 47/			-200	200	
Overall gain error with external reference 47/		If ADCREFP-ADCREFM = 1 V ±0.1%	-50	50	
Channel to channel offset variation			±8 Typ		
Channel to channel Gain variation			±8 Typ		
Analog input					
Analog input voltage (ADCINx to ADCLO) 49/			0	3	V
Adclo			-5	5	mV
Input capacitance			10 Typ		pF
Input leakage current				±5	µA
Internal Voltage reference 47/					
Accuracy, $ADCV_{REFP}$			1.9	2.1	V
Accuracy, $ADCV_{REFM}$			0.95	1.05	
Voltage difference, ADCREFP-ADCREFM			1 Typ		
Temperature coefficient			50 Typ		PPM/°C
Reference noise			100 Typ		µV
External Voltage reference 48/					
Accuracy, $ADCV_{REFP}$			1.9	2.1	V
Accuracy, $ADCV_{REFM}$			0.95	1.05	
Input voltage difference, ADCREFP-ADCREFM			0.99	1.01	
AC specifications					
Signal to noise ratio + distortion	SINAD		62 Typ		dB
Signal to noise ratio	SNR		62 Typ		
Total harmonic distortion	THD(100 kHz)		-68 Typ		
Effective number of bits	ENOB(SNR)		10.1 Typ		Bits
Spurious free dynamic range	SFDR		69 Typ		dB

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/		Limits		Unit
				Min	Max	
ON CHIP ANALOG TO DIGITAL CONVERTER - Continued						
ADC power up Delays 50/						
Delay time for band gap reference to be stable. Bits 6 and 5 of the ADCTRL3 register (PWDNBG and PWDNREF) are to be set to 1 before the PWDNADC bit is enabled	$t_{d(BGR)}$	See figure 35		7	10	ms
Delay time for power down control to be stable. Bit 7 of the ADCTRL3 register (PWDNADC) is to be set to 1 before any ADC conversions are initiated	$t_{d(PWD)}$			0.02	1	
Sequential sampling mode timing 51/ See figure 36						
		Sample n	Sample n + 1	51/		
Delay time from even trigger to sampling	$t_{d(SH)}$	$2.5t_{c(ADCCLK)}$				ns
Sample/Hold width/Acquisition width 52/	t_{SH}	(1+Acqps)* $t_{c(ADCCLK)}$		40 ns with Acqps = 0 Typ		
Delay time for first result to appear in the Result register	$t_{d(schx_n)}$	$4t_{c(ADCCLK)}$		160 Typ		
Delay time for successive results to appear in the Result register	$t_{d(schx_n+1)}$		(2+Acqps)* $t_{c(ADCCLK)}$	80 Typ		
Simultaneous sampling mode timing 51/ See figure 37						
		Sample n	Sample n + 1	51/		
Delay time from even trigger to sampling	$t_{d(SH)}$	$2.5t_{c(ADCCLK)}$				ns
Sample/Hold width/Acquisition width 52/	t_{SH}	(1+Acqps)* $t_{c(ADCCLK)}$		40 ns with Acqps = 0 Typ		
Delay time for first result to appear in the Result register	$t_{d(schA0_n)}$	$4t_{c(ADCCLK)}$		160 Typ		
Delay time for first result to appear in the Result register	$t_{d(schB0_n)}$	$5t_{c(ADCCLK)}$		200 Typ		
Delay time for successive result to appear in the Result register	$t_{d(schA0_n+1)}$		(3+Acqps)* $t_{c(ADCCLK)}$	120 Typ		
Delay time for successive results to appear in the Result register	$t_{d(schB0_n+1)}$		(3+Acqps)* $t_{c(ADCCLK)}$	120 Typ		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/		Limits		Unit
					Min	Max	
MULTICHANNELBUFFERED SERIAL PORT (McBSP) TIMING							
McBSP timing requirements							
	McBSP module clock (CLKG, CLKX, CLKR) range		See figure 38		0.001	20 55/	MHz
	McBSP module cycle time (CLKG, CLKX, CLKR) range				50	1000	ns
M11	Cycle time, CLKR/X	$t_{c(CKRX)}$		CLKR/X ext	2P		
M12	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext	P-7		
M13	Rise time, CLKR/X	$t_{r(CKRX)}$		CLKR/X ext		7	
M14	Fall time, CLKR/X	$t_{f(CKRX)}$		CLKR/X ext		7	
M15	Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int	18		
				CLKR ext	2		
M16	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int	0		
				CLKR ext	6		
M17	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int	18		
				CLKR ext	2		
M18	Hold time, DR valid after CLKR low	$t_{h(CKRl-DRV)}$		CLKR int	0		
				CLKR ext	6		
M19	Setup time, external FSR high before CLKX low	$t_{su(FXH-CKXL)}$		CLKR int	18		
				CLKR ext	2		
M20	Hold time, external FSR high after CLKX low	$t_{h(CKXL-FXH)}$		CLKR int	0		
				CLKR ext	6		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test		Symbol	Test condition 2/		Limits		Unit
						Min	Max	
	MULTICHANNELBUFFERED SERIAL PORT (McBSP) TIMING							
	McBSP switching characteristics 53/ 54/							
M1	Cycle time, CLKR/X		$t_{c(CKRX)}$		CLKR/X int	2P		ns
M2	Pulse duration, CLKR/X high 56/		$t_{w(CKRXH)}$		CLKR/X int	D-5	D+5	
M3	Pulse duration, CLKR/X low 56/		$t_{w(CKRXL)}$		CLKR/X int	C-5	C+5	
M4	Delay time, CLKR high to internal FSR valid		$t_{d(CKRH-FRV)}$		CLKR int	0	4	
					CLKR ext	3	27	
M5	Delay time, CLKX high to internal FSX valid		$t_{d(CKXH-FXV)}$		CLKX int	0	4	
					CLKX ext	3	27	
M6	Disable time, CLKX high to DX high impedance following last data bit transmitted		$t_{dis(CKXH-DXHZ)}$		CLKX int		8	
					CLKX ext		14	
M7	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		$t_{d(CKXH-DXV)}$		CLKX int		9	
					CLKX ext		28	
	Delay time, CLKX high to DX valid	DXENA = 0			CLKX int		8	
					CLKX ext		14	
	Only applies to first bit transmitted when in data delay 1 or 2 (XDATDLY = 01b or 10b) modes	DXENA = 1			CLKX int		P+8	
					CLKX ext		P+14	
M8	Enable time, CLKX high to DX driven	DXENA = 0	$t_{en(CKXH-DX)}$		CLKX int	0		
					CLKX ext	6		
	Only applies to first bit transmitted when in data delay 1 or 2 (XDATDLY = 01b or 10b) modes	DXENA = 1			CLKX int	P		
					CLKX ext	P+6		
M9	Delay time, FSX high to DX valid	DXENA = 0	$t_{d(FXH-DXV)}$		FSX int		8	
					FSX ext		14	
	Only applies to first bit transmitted when in data delay 0 (XDATDLY = 00b) modes	DXENA = 1			FSX int		P+8	
					FSX ext		P+14	
M10	Enable time, FSX high to DX driven	DXENA = 0	$t_{en(FXH-DX)}$		FSX int	0		
					FSX ext	6		
	Only applies to first bit transmitted when in data delay 0 (XDATDLY = 00b) modes	DXENA = 1			FSX int	P		
					FSX ext	P+6		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	
MULTICHANNELBUFFERED SERIAL PORT (McBSP) TIMING – Continued								
McBSP as SPI Master or Slave timing requirements (CLKSTP = 10b, CLKXP = 0)								
M30	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 39	P-10		8P-10		ns
M31	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		P-10		8P-10		
M32	Setup time, FSX low before CLKX high	$t_{su(BFXL-CKXH)}$				8P+10		
M33	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 10b, CLKXP = 0) 57/								
M24	Hold time, FSX low after CLKX low	$t_{h(CKXL-FXL)}$	See figure 39	2P				ns
M25	Delay time, FSX low to CLKX high	$t_{d(FXL-CKXH)}$		P				
M28	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$		6		6P+6		
M29	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		6		4P+6		
McBSP as SPI Master or Slave timing requirements (CLKSTP = 11b, CLKXP = 0) 57/								
M39	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 40	P-10		8P-10		ns
M40	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		P-10		8P-10		
M41	Setup time, FSX low before CLKX high	$t_{su(FXL-CKXH)}$				16P+10		
M42	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 11b, CLKXP = 0) 57/								
M34	Hold time, FSX low after CLKX low	$t_{h(CKXL-FXL)}$	See figure 40	P				ns
M35	Delay time, FSX low to CLKX high	$t_{d(FXL-CKXH)}$		2P				
M37	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(FXH-DXHZ)}$		P+6		7P+6		
M38	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		6		4P+6		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	
MULTICHANNELBUFFERED SERIAL PORT (McBSP) TIMING – Continued								
McBSP as SPI Master or Slave timing requirements (CLKSTP = 10b, CLKXP = 1)								
M49	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 41	P-10		8P-10		ns
M50	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		P-10		8P-10		
M51	Setup time, FSX low before CLKX low	$t_{su(FXL-CKXL)}$				8P+10		
M52	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 10b, CLKXP = 1) 57/								
M43	Hold time, FSX low after CLKX high	$t_{h(CKXH-FXL)}$	See figure 41	2P				ns
M44	Delay time, FSX low to CLKX low	$t_{d(FXL-CKXL)}$		P				
M47	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$		6		6P+6		
M48	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		6		4P+6		
McBSP as SPI Master or Slave timing requirements (CLKSTP = 11b, CLKXP = 1) 57/								
M58	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 42	P-10		8P-10		ns
M59	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		P-10		8P-10		
M60	Setup time, FSX low before CLKX low	$t_{su(FXL-CKXL)}$				16P+10		
M61	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 11b, CLKXP =1) 57/								
M53	Hold time, FSX low after CLKX high	$t_{h(CKXH-FXL)}$	See figure 42	P				ns
M54	Delay time, FSX low to CLKX low	$t_{d(FXL-CKXL)}$		2P				
M56	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		P+6		7P+6		
M57	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		6		4P+6		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test			Symbol	Test condition 2/	Limits		Unit
					Min	Max	
FLASH TIMING (F281X ONLY)							
Recommended operation conditions							
Flash endurance for the array (Write/erase cycles)			N_f	0°C to 85°C	100		cycles
OTP endurance for the array (Write cycles)			N_{OTP}	0°C to 85°C		1	write
Flash parameters at 150 MHz SYSCLKOUT 58/							
Program time	16 Bit Word				35 Typ		µs
	8K Sector				170 Typ		ms
	16K Sector				320 Typ		ms
Erase time	8K Sector				10 Typ		S
	16K Sector				11 Typ		S
VDD3VFL current consumption during the Erase/Program cycle		Erase	$I_{DD3VFLP}$		75 Typ		mA
		Program			35 Typ		
V_{DD} current consumption during the Erase/Program cycle			I_{DDP}		140 Typ		
I_{DDIOP} current consumption during the Erase/Program cycle			I_{DDIOP}		20 Typ		
Flash/OTP access timing 59/							
Paged Flash access time			$t_{a(fp)}$		36		ns
Random access time			$t_{a(fr)}$		36		
OTP access time			$t_{a(OTP)}$		60		

Minimum required Wait States at different frequencies

SYSCLKOUT (MHz)	**SYSCLKOUT** (ns)	**Page Wait state** 60/	**Random Wait state** 60/ 61/
150	6.67	5	5
120	8.33	4	4
100	10.00	3	3
75	13.33	2	2
50	20.00	1	1
30	33.33	1	1
25	40.00	0	1
15	66.67	0	1
4	250.00	0	1

See notes at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Test conditions are over recommended ranges of supply voltage and operating case temperature unless otherwise specified. Device type: All.
3/ A load of 40 pF is assumed for these parameters.
4/ $H = 0.5t_{c(XCO)}$
5/ The PLL must be used for maximum frequency operation.
6/ This parameter has changed from 4096 XCLKIN cycles in the earlier revisions of the silicon.
7/ If external oscillator/clock source are used, reset time has to be low at least for 1 ms after V_{DD} reaches 1.5 V.
8/ Dependent on crystal/resonator and board design.
9/ The boot ROM reads the password locations. Therefore, this timing requirement include the wakeup time for flash. See manufacturer for more details.
10/ Input Qualification Time (IQT) = [5 x QUALPRD x 2] * $t_{c(SCO)}$.
11/ This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up) signal involves additional latency.
12/ AUALSTDBY is a 6 bit field in the LPMCR0 register.
13/ See the GPIO output timing for fall/rise times for PWM pins.
14/ PWM pin toggling frequency is limited by the GPIO output buffer switching frequency (20 MHz).
15/ PWM outputs may be 100%, 0%, or increments of $t_{c(HCO)}$ with respect to the PWM period.
16/ The QUALPRD bit field value can range from 0 (no qualification) through 0xFF (510 SYSCLKOUT cycles). The qualification sampling period is 2n SYSCLKOUT cycles, where “n” is the value stored in the QUALPRD bit field. As an example, when QUALPRD = 1, the qualification sampling period is 1 x 2 = 2 SYSCLKOUT cycles (i.e., the input is sampled every 2 SYSCLKOUT cycles). Six such samples will be taken over five sampling windows, each window being 2n SYSCLKOUT cycles. For QUALPRD = 1, the minimum width that is needed is 5 x 2 = 10 SYSCLKOUT cycles. However, since the external signal is driven asynchronously, a 11 SYSCLKOUT wide pulse ensures reliable recognition.
17/ Maximum input frequency to the QEP = min[HSPCLK/2, 20 MHz].
18/ Input Qualification Time (IQT) = [5 x QUALPRD x 2]*$t_{c(SCO)}$.
19/ XCLKOUT = SYSCLKOUT.
20/ The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
21/ $t_{c(SPC)}$ = SPI clock cycle time = $\frac{\text{LSPCLK}}{4}$ or $\frac{\text{LSPCLK}}{(\text{SPIBRR}+1)}$
$t_{c(LCO)}$ = LSPCLK cycle time.
22/ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).
Note: Internal clock prescalers must be adjusted such that the SPI clock speed is not greater than the I/O buffer speed signal limit (20 MHz).
23/ $0.5t_{c(SPC)M} – 10$
24/ $0.5t_{c(SPC)M}$
25/ $0.25t_{c(SPC)M} – 10$
26/ $0.5t_{c(SPC)M} – 0.5t_{c(LCO)} – 10$
27/ $0.5t_{c(SPC)M} – 0.5t_{c(LCO)}$
28/ $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} – 10$
29/ $0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$
30/ $0.5t_{c(SPC)S} – 10$
31/ $0.5t_{c(SPC)S}$
32/ $0.375t_{c(SPC)S} – 10$
33/ $0.75t_{c(SPC)S}$
34/ $0.125t_{c(SPC)S}$
35/ During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.
36/ LR = Lead period, read access. AR = Active period, read access.

37/ TW = Trail period, write access.

38/ The first XREADY (Synch) sample occurs with respect to E in figure 29:
E = (XRDLEAD + XRDACTIVE) $t_{c(XTIM)}$
When first sampled, if XREADY (Synch) is found to be high, then the access will complete. If XREADY (Synch) is found to be low, it will sampled again each $t_{c(XTIM)}$ until it is found to be high.
For each sample (n) the setup time (D) with respect to the beginning of the access can be calculated as:
D = (XRDLEAD + XRDACTIVE + n – 1)$t_{c(XTIM)}$ – $t_{su(XRDYsynchL)XCOHL}$ where n is the sample number: n = 1,2,3, and so forth.

39/ The first XREADY (Asynch) sample occurs with respect to E in figure 30:
E = (XRDLEAD + XRDACTIVE - 2) $t_{c(XTIM)}$
When first sampled, if XREADY (Asynch) is found to be high, then the access will complete. If XREADY (Asynch) is found to be low, it will sampled again each $t_{c(XTIM)}$ until it is found to be high.
For each sample (n) the setup time (D) with respect to the beginning of the access can be calculated as:
D = (XRDLEAD + XRDACTIVE + n – 3)$t_{c(XTIM)}$ – $t_{su(XRDYasynchL)XCOHL}$ where n is the sample number: n = 1,2,3, and so forth.

40/ When a low signal detected on $\overline{\text{XHOLD}}$, all pending XINTF accesses will be completed before the bus is placed in a high impedance state.

41/ The state of $\overline{\text{XHOLD}}$ is latched on the rising edge of XTIMCLK.

42/ After $\overline{\text{XHOLD}}$ is detected low or high, all bus transactions and $\overline{\text{XHOLDA}}$ transactions will occur with respect to the rising edge of XCLKOUT. Thus, for this mode where XCLKOUT = 1/2 XTIMCLK, the transitions can occur up to 1 XTIMCLK cycle earlier than the maximum value specified.

43/ Tested at 12.5 MHz ADDCLK.

44/ If SYSCLKOUT ≤ 25 MHz, ADC clock ≤ SYSCLKOUT/2.

45/ The INL degrades for frequencies beyond 18.75 MHz – 25 MHz. Applications that require these sampling rates should use a 20K resistor as bias resistor on the ADCRESEXT pin. This improve overall linearity and typical current drawn by the ADC will be a few mA more than 24.9 kΩ bias.

46/ 1 LSB has the weighted value of 1.0/4096 = 0.732 V.

47/ A single internal band gap reference (±5% accuracy) sources both ADCREFP and ADCREFM signals, and hence, these voltages track together. The ADC converter uses the difference between these two as its reference. The total gain error will be the combination of the gain error shown here and the voltage reference accuracy (ADCREFP – ADCREFM). A software based calibration procedure is recommended for better accuracy.

48/ In this mode, the accuracy of external reference is critical for overall gain. The voltage difference (ADCREFP – ADCREFM) will determine the overall accuracy.

49/ Voltages above V_{DDA} + 0.3 V or below V_{SS} – 0.3 V applied to an analog input pin may temporarily affect the conversion of another pin. To avoid this, the analog inputs should be kept within these limits.

50/ These delay are necessary and recommended to make the ADC analog reference circuit stable before conversions are initiated. If conversions are stated without these delays, the ADC results will show a higher gain. For power down, all three bits can be cleared at the same time.

51/ At 25 MHz ADC clock, $t_{c(ADCCLK)}$ = 40 ns.

52/ Acqcps value = 0 – 15 ADCTRL1[18:1]

53/ Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

54/ 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. CLKG = $\frac{\text{CLKSRG}}{(1+\text{CLKGDV})}$ where CLKSRG can be LSPCLK, CLKX, CLKR as source. CLKSRG ≤ (SYSCLKOUT/2). McBSP performance is limited by I/O buffer switching speed.

55/ Internal clock prescalers must be adjusted such that the McBSP clock (CLKG, CLKX, CLKR) speeds are not greater than the I/O buffer speed limit (20 MHz).

56/ C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

TABLE I. Electrical performance characteristics - Continued.

57/ 2P = 1/CLKG. For all SPI slave modes, CLKX has to be minimum 8 CLKG cycles. Also CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With maximum LSPCLK speed of 75 MHz, CLKX maximum frequency will be LSPCLK/16, that is 4.5 MHz and P = 13.3 ns.

58/ Typical parameters as seen at room temperature using flash API V1 including function call overhead.

59/ For 150 MHz, PAGE WS = 5 and RANDOM WS = 5
For 135 MHz, PAGE WS = 4 and RANDOM WS = 4

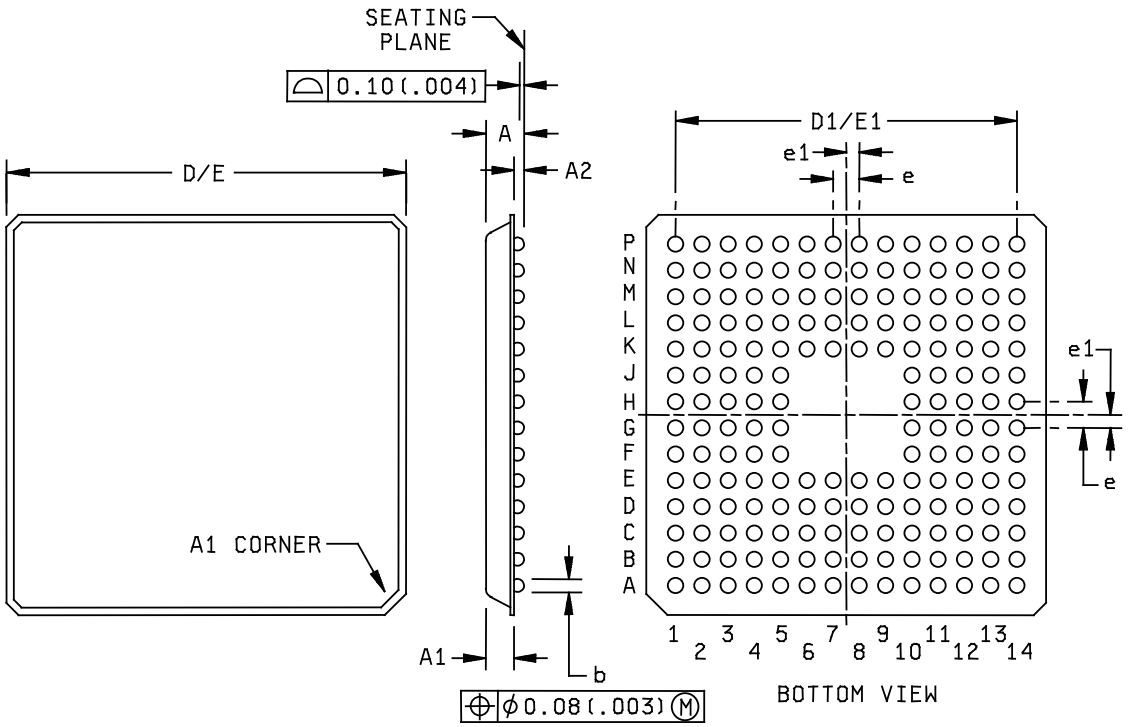
60/ Formulas to compute page wait state and random wait state:

Page Wait State = $\left[\left(\frac{t_{a(fp)}}{t_{c(SCO)}}\right) - 1\right]$ (round up to the highest integer), or 0 whichever is larger

Random Wait State = $\left(\left[\frac{t_{a(fr)}}{t_{c(SCO)}}\right] - 1\right)$ round up to the highest integer), or 1 whichever is larger

61/ Random wait state must be greater than or equal to 1.

Case X

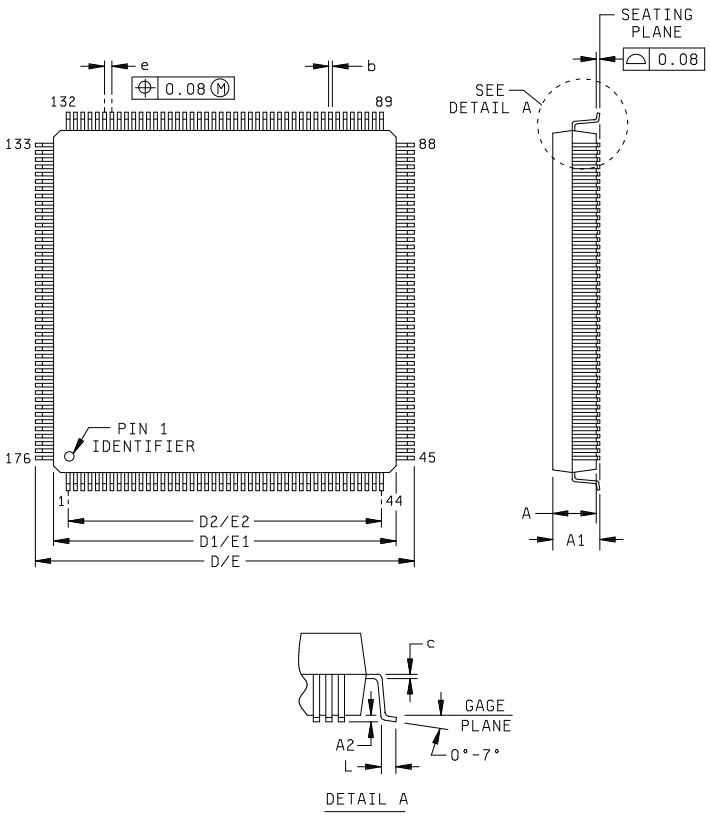


Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		1.40		.055	D/E	11.90	12.10	.469	.476
A1	0.85	0.95	.033	.037	D1/E1	10.40 Typ		.409 Typ	
A2	0.35	0.45	.014	.018	e	0.40 Typ		.016 Typ	
b	0.45	0.55	.018	.022	e1	0.80 Typ		.031 Typ	

Notes:
1. This drawing is subject to change without notice.
2. MicroStar BGA configuration.
3. This package is not lead free and needs a minimum reflow temperature of 220°C but not exceeding 235°C.

FIGURE 1. Case outlines.

Case Z



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.35	1.45	.053	.057	D/E	25.80	26.20	1.016	1.031
A1		1.60		.063	D1/E1	23.80	24.20	.937	.953
A2	0.05		.002		D2/E2	21.50 TYP		.846 TYP	
b	0.17	0.27	.007	.011	e	0.50 TYP		.020 TYP	
c	0.13 NOM		.005 NOM		L	0.45	0.75	.018	.030

Notes:
1. This drawing is subject to change without notice.
2. Fall within JEDEC MS-026.
3. This package is lead free and needs a minimum reflow temperature of 220°C but not exceeding 235°C.

FIGURE 1. Case outlines - Continued.

Case X

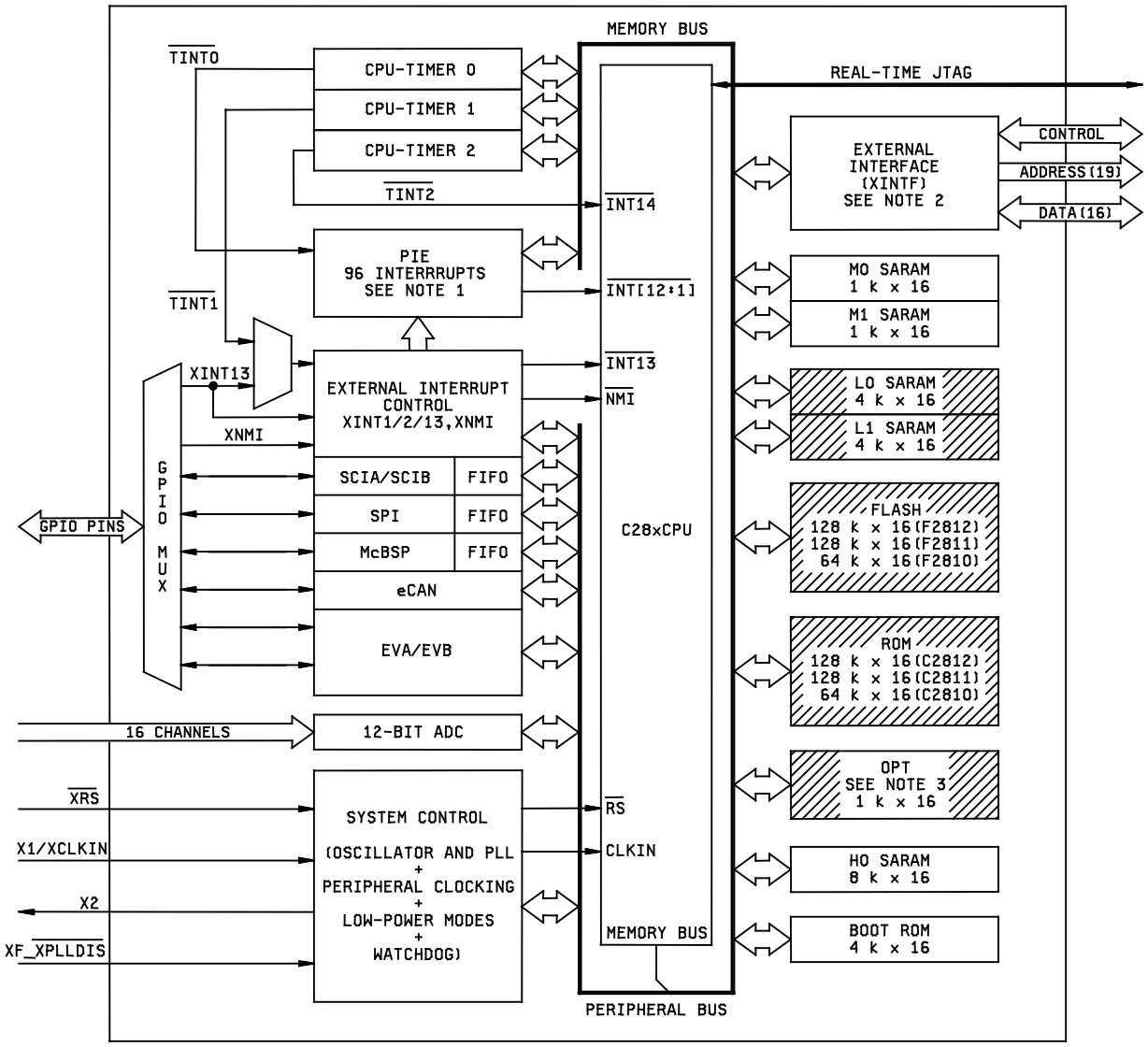
Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
		B1	ADCINB2	C1	ADCINB3	D1	ADCINB6	E1	AVDDREFBG
A2	V_{SSAIO}	B2	V_{DDAIO}	C2	ADCINB0	D2	ADCINB5	E2	ADCREFP
A3	ADCINA0	B3	ADCLO	C3	ADCINB1	D3	ADCINB4	E3	AVSSREFBG
A4	ADCINA4	B4	ADCINA3	C4	ADCINA2	D4	ADCINA1	E4	ADCREFM
A5	V_{DDA2}	B5	ADCINA7	C5	V_{SSA2}	D5	ADCINA6	E5	ADCINA5
A6	V_{DD1}	B6	XREADY	C6	V_{SS1}	D6	$\overline{XRS}$	E6	ADCBGREFIN
A7	SCIRXDA	B7	XA[17]	C7	SCITXDA	D7	XA[18]	E7	$\overline{XHOLD}$
A8	XA[16]	B8	V_{SS}	C8	V_{DD}	D8	XINT2_ADCSOC	E8	XNMI_XINT13
A9	XD[15]	B9	XA[15]	C9	EMU1	D9	XINT1_ $\overline{XBIO}$	E9	V_{DDIO}
A10	XA[14]	B10	V_{DD}	C10	V_{SS}	D10	V_{SS}	E10	XA[13]
A11	XF_ $\overline{XPLLDIS}$	B11	XD[14]	C11	XA[12]	D11	EMU0	E11	$\overline{C2TRIP}$
A12	TCK	B12	$\overline{TRST}$	C12	XA[10]	D12	TDO	E12	XA[8]
A13	TESTSEL	B13	$\overline{XZCS6AND7}$	C13	TDI	D13	TMS	E13	$\overline{C1TRIP}$
A14	XA[11]	B14	V_{SS}	C14	V_{DD}	D14	XA[9]	E14	V_{SS}
F1	XMP/ $\overline{MC}$	G1	MDXA			H1	V_{DD}	J1	MCLKXA
F2	ADCRESEXT	G2	MDRA			H2	MCLKRA	J2	MFSRA
F3	V_{SSA1}	G3	XD[0]			H3	XD[1]	J3	XD[3]
F4	V_{DDA1}	G4	V_{SS}			H4	MFSXA	J4	V_{DDIO}
F5	ADCINB7	G5	XA[0]			H5	XD[2]	J5	XD[5]
F10	$\overline{C3TRIP}$	G10	$\overline{T2CTRIP / EVASOC}$			H10	CAP1_QEP1	J10	XD[13]
F11	XCLKOUT	G11	V_{DDIO}			H11	CAP2_QEP2	J11	T1PWM_T1CMP
F12	XA[7]	G12	V_{DD}			H12	CAP3_QEPI1	J12	XA[4]
F13	TCLKINA	G13	V_{SS}			H13	XA[5]	J13	T2PWM_T2CMP
F14	TDIRA	G14	XA[6]			H14	$\overline{T1CTRIP _ PDPINTA}$	J14	V_{SS}
K1	V_{SS}	L1	V_{DD}	M1	SPISIMOA	N1	SPISOMIA	P1	$\overline{XZCS0AND1}$
K2	SPICLKA	L2	V_{SS}	M2	XA[1]	N2	PWM7	P2	PWM8
K3	XD[4]	L3	XD[6]	M3	$\overline{XRD}$	N3	PWM9	P3	PWM10
K4	SPISTEA	L4	PWM11	M4	PWM12	N4	XR/ $\overline{W}$	P4	V_{SS}
K5	T3PWM_T3CMP	L5	XD[7]	M5	CAP4_QEP3	N5	T4PWM_T4CMP	P5	V_{DD}
K6	V_{SS}	L6	$\overline{C5TRIP}$	M6	CAP5_QEP4	N6	$\overline{C4TRIP}$	P6	CAP6_QEPI2
K7	$\overline{C6TRIP}$	L7	V_{DDIO}	M7	TEST1	N7	TEST2	P7	XD[8]
K8	TCLKINB	L8	TDIRB	M8	XD[9]	N8	V_{DD3VFL}	P8	V_{SS}
K9	X1/XCLKIN	L9	XD[10]	M9	X2	N9	XD[11]	P9	V_{DD}
K10	$\overline{XHOLDA}$	L10	V_{DDIO}	M10	V_{SS}	N10	XA[2]	P10	$\overline{T3CTRIP _ PDPINTB}$
K11	PWM5	L11	V_{SS}	M11	XA[3]	N11	$\overline{XWE}$	P11	$\overline{T4CTRIP / EVBSOC}$
K12	V_{DD}	L12	PWM3	M12	PWM1	N12	CANTXA	P12	V_{DD}
K13	V_{SS}	L13	PWM4	M13	SCIRXDB	N13	CANRXA	P13	$\overline{XZCS2}$
K14	PWM6	L14	XD[12]	M14	PWM2	N14	V_{DDIO}	P14	SCITXDB

FIGURE 2. Terminal connections.

Case Z

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
1	V_{DDAIO}	37	V_{DD}	72	TCLKINB	107	CAP2_QEP2	142	V_{SS}
2	ADCINB0	38	V_{SS}	73	XD[10]	108	XA[5]	143	V_{DD}
3	ADCINB1	39	XD[6]	74	XD[11]	109	CAP3_QEPI1	144	XA[14]
4	ADCINB2	40	SPISIMOA	75	V_{DD}	110	$\overline{\text{T1CTRIP_PDPINTA}}$	145	V_{DDIO}
5	ADCINB3	41	SPISOMIA	76	X2	111	XA[6]	146	EMU1
6	ADCINB4	42	$\overline{\text{XRD}}$	77	X1/CLKIN	112	V_{DD}	147	XD[15]
7	ADCINB5	43	XA[1]	78	V_{SS}	113	V_{SS}	148	XA[15]
8	ADCINB6	44	$\overline{\text{XZCS0AND1}}$	79	$\overline{\text{T3CTRIP_PDPINTB}}$	114	V_{DDIO}	149	XINT1_$\overline{\text{XBIO}}$
9	ADCINB7	45	PWM7	80	XA[2]	115	$\overline{\text{T2CTRIP/EVASOC}}$	150	XNMI_XINT13
10	ADCREFM	46	PWM8	81	V_{DDIO}	116	TDIRA	151	XINT2_ADCSOC
11	ADCREFP	47	PWM9	82	$\overline{\text{XHOLDA}}$	117	TCLKINA	152	XA[16]
12	AVSSREFBG	48	PWM10	83	$\overline{\text{T4CTRIP/EVBSOC}}$	118	XA[7]	153	V_{SS}
13	AVDDREFBG	49	PWM11	84	$\overline{\text{XWE}}$	119	XCLKOUT	154	V_{DD}
14	V_{DDA1}	50	PWM12	85	XA[3]	120	V_{SS}	155	SCITXDA
15	V_{SSA1}	51	XR/$\overline{\text{W}}$	86	V_{SS}	121	XA[8]	156	XA[17]
16	ADCRESEXT	52	V_{SS}	87	CANTXA	122	$\overline{\text{C1TRIP}}$	157	SCIRXDA
17	XMP/$\overline{\text{MC}}$	53	T3PWM_T3CMP	88	$\overline{\text{XZCS2}}$	123	$\overline{\text{C2TRIP}}$	158	XA[18]
18	XA[0]	54	XD[7]	89	CANRXA	124	$\overline{\text{C3TRIP}}$	159	$\overline{\text{XHOLD}}$
19	V_{SS}	55	T4PWM_T4CMP	90	SCITXDB	125	XA[9]	160	$\overline{\text{XRS}}$
20	MDRA	56	V_{DD}	91	SCIRXDB	126	TMS	161	XREADY
21	XD[0]	57	CAP4_QEP3	92	PWM1	127	TDO	162	V_{DD1}
22	MDXA	58	V_{SS}	93	PWM2	128	V_{DD}	163	V_{SS1}
23	V_{DD}	58	CAP5_QEP4	94	PWM3	129	V_{SS}	164	ADCBGREFIN
24	XD[1]	60	CAP6_QEP12	95	PWM4	130	XA[10]	165	V_{SSA2}
25	MCLKRA	61	$\overline{\text{C4TRIP}}$	96	XD[12]	131	TDI	166	V_{DDA2}
26	MFSXA	62	$\overline{\text{C5TRIP}}$	97	XD[13]	132	XA[11]	167	ADCINA7
27	XD[2]	63	$\overline{\text{C6TRIP}}$	98	PWM5	133	$\overline{\text{XZCS6AND7}}$	168	ADCINA6
28	MCLKXA	64	V_{DDIO}	99	V_{SS}	134	TESTSEL	169	ADCINA5
29	MFSRA	65	XD[8]	100	V_{DD}	135	$\overline{\text{TRST}}$	170	ADCINA4
30	XD[3]	66	TEST2	101	PWM6	136	TCK	171	ADCINA3
31	V_{DDIO}	67	TEST1	102	T1PWM_T1CMP	137	EMU0	172	ADCINA2
32	V_{SS}	68	XD[9]	103	XA[4]	138	XA[12]	173	ADCINA1
33	XD[4]	69	V_{DD3VFL}	104	T2PWM_T2CMP	139	XD[14]	174	ADCINA0
34	SPICLKA	70	V_{SS}	105	V_{SS}	140	XF_$\overline{\text{XPLLDIS}}$	175	ADCLO
35	SPISTEA	71	TDIRB	106	CAP1_QEP1	141	XA[13]	176	V_{SSAIO}
36	XD[5]								

FIGURE 2. Terminal connections - Continued.



Notes:
1. 45 of the possible 96 interrupts are used on the devices.
2. XINTF is available on the device type 03 and 06 only.
3. On device type 04, 05,and 06, the OPT is replaced with a 1K x 16 block of ROM.

FIGURE 3. Block diagram.

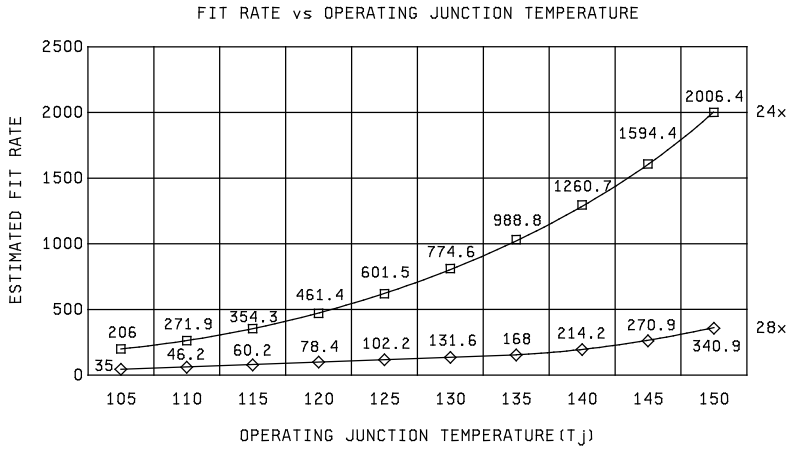


FIGURE 4. FIT rate versus operating junction temperature.

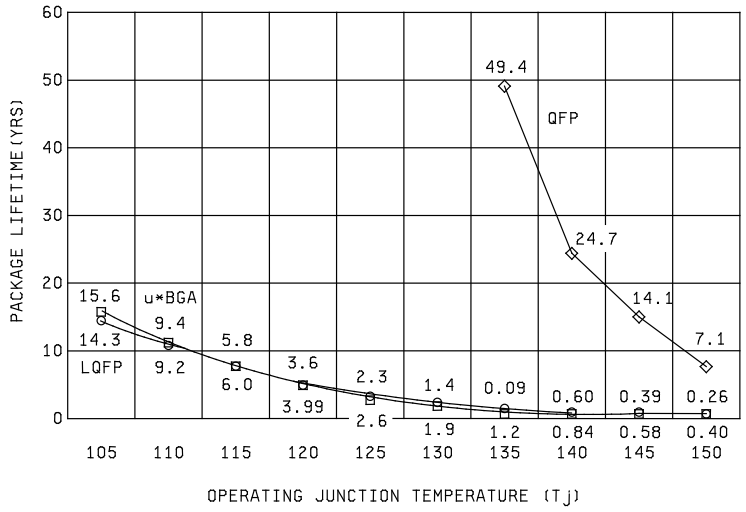


FIGURE 5. Package lifetime versus operating junction temperature.

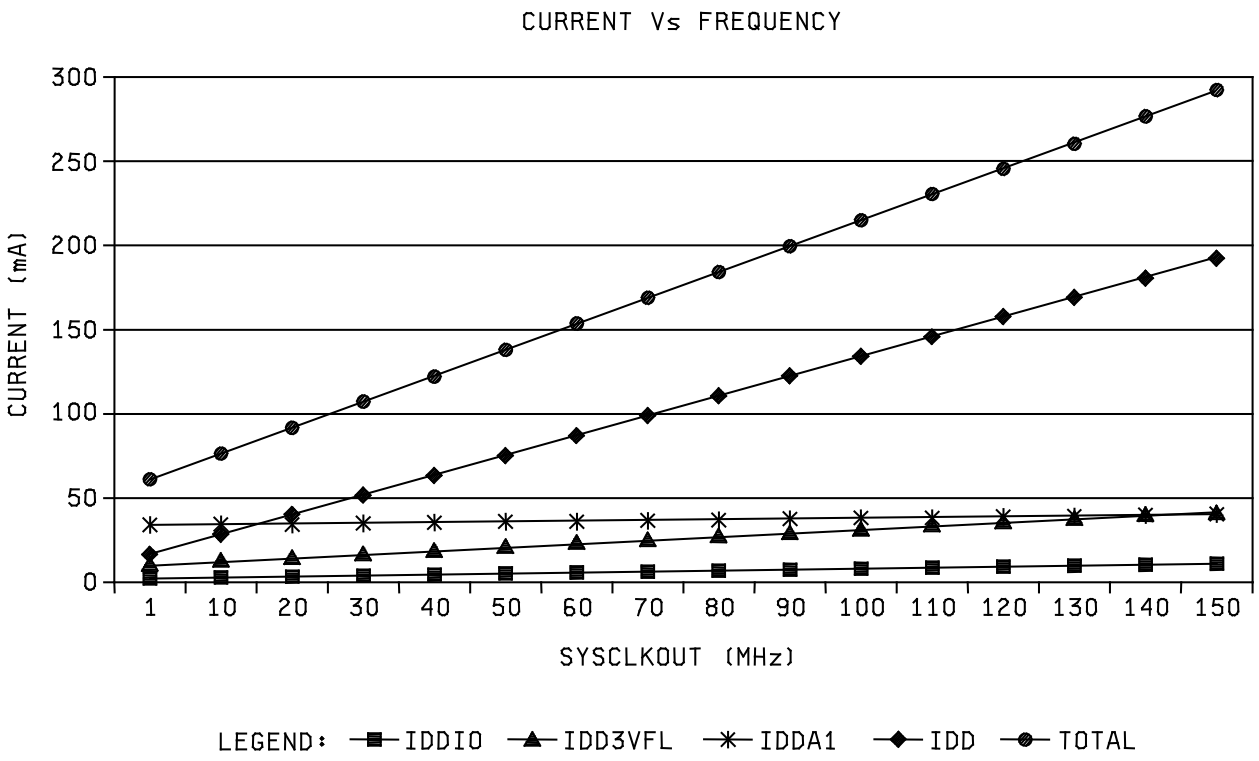
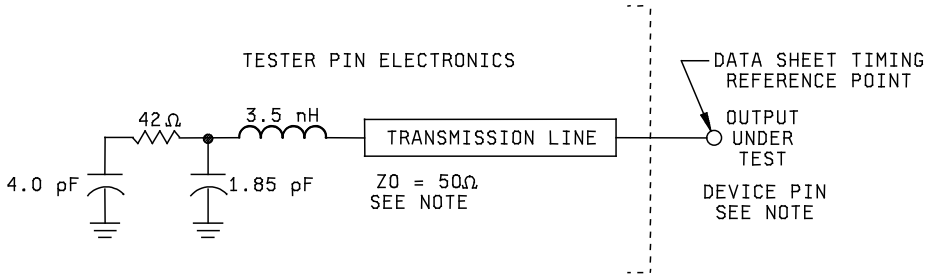


FIGURE 6. Current consumption graphs.

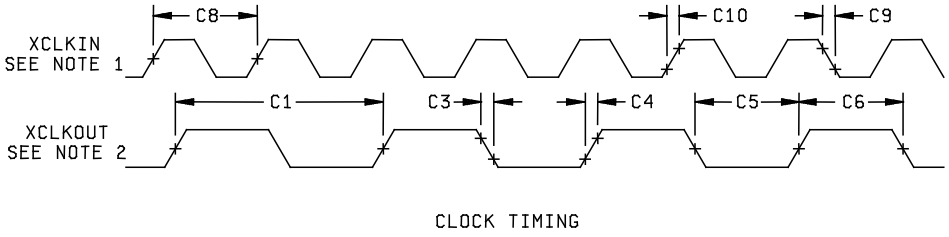


AC timing measurements for device type 03 and 04 only

Note:

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts pre nanosecond (4 V/ns) at the device pin.

FIGURE 7. Test load circuit.

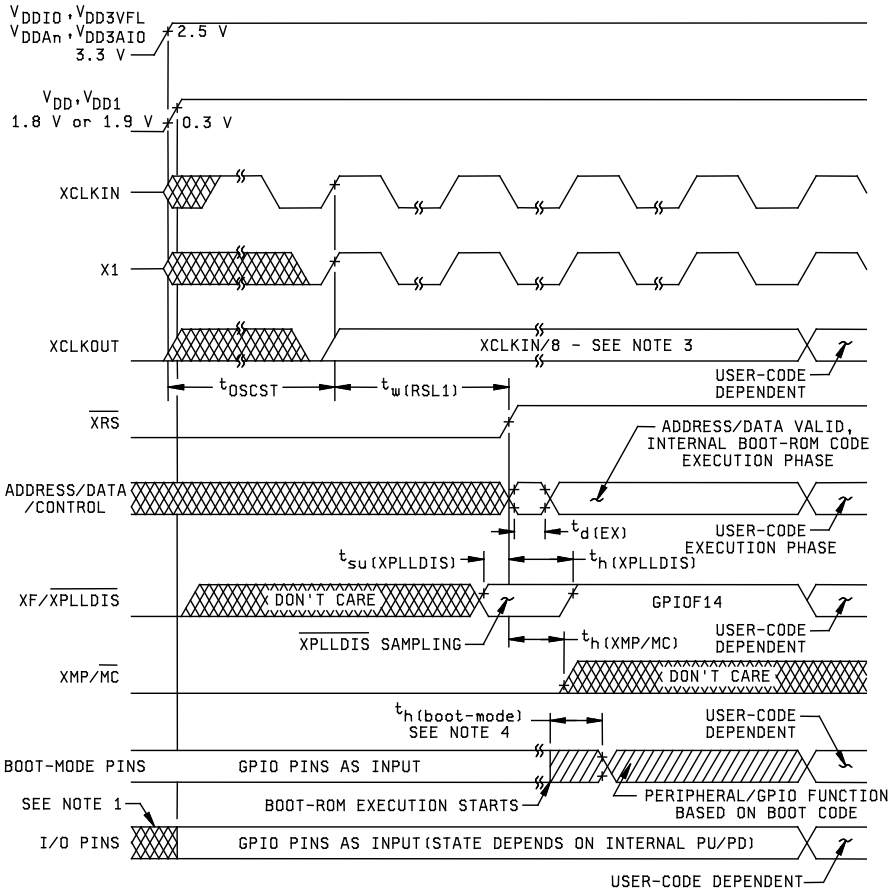


CLOCK TIMING

Note:

1. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship in this figure is intended to illustrate the timing parameters only and may differ based on configuration.
2. XCLKOUT configured to reflect SYSCLKOUT.

FIGURE 8 Timing waveforms.

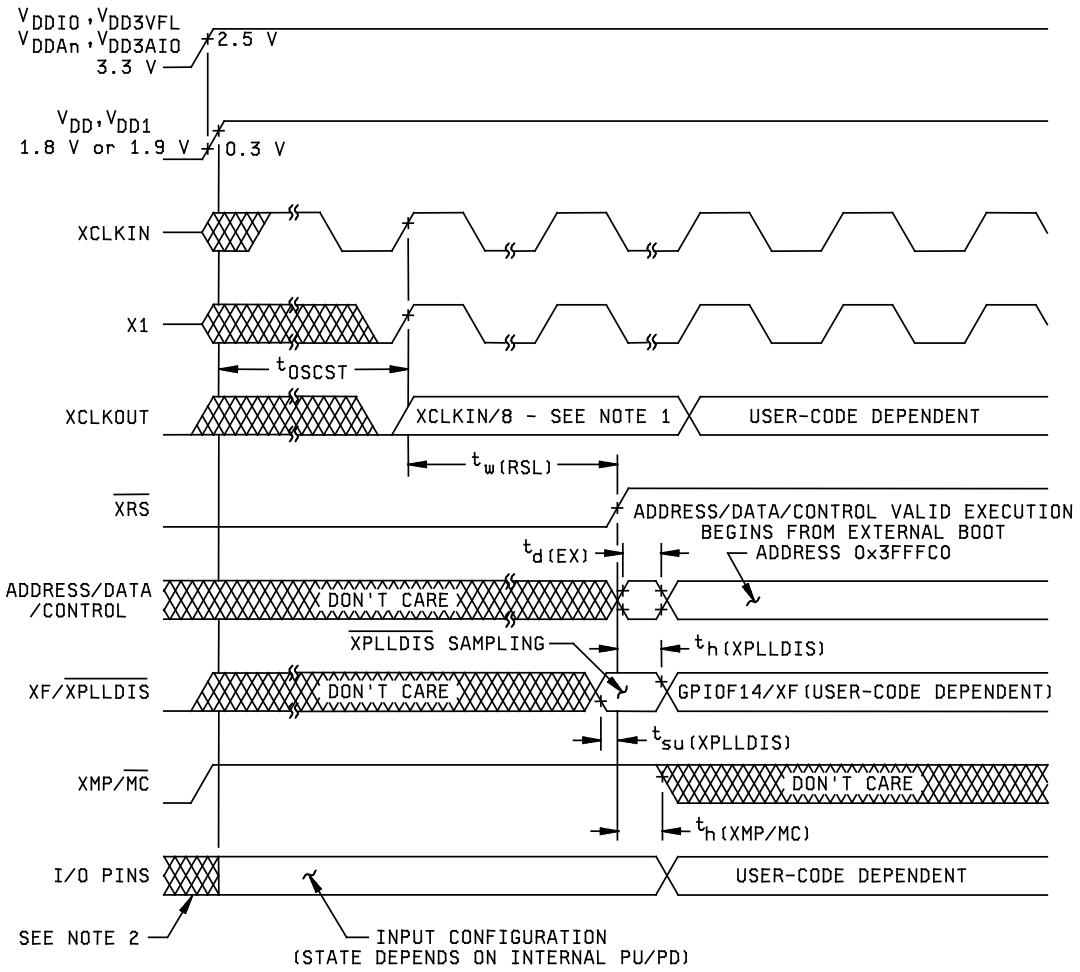


POWER-ON RESET IN MICROCOMPUTER MODE(XMP/MC=0) SEE NOTE 1

Notes:

1. The state of the GPIO pins is undefined (i.e., they could be input or output) until the 1.8 V (or 1.9 V) supply reaches at least 1 V and 3.3 V supply reaches 2.5 V.
2. V_{DDAn} – V_{DDA1}/V_{DDA2} and $AV_{DDREFBG}$.
3. Upon power up, SYSCLKOUT is XCLKIN/2 if the PLL is enabled. Since both the XTIMCLK and CLKMODE bits in the XINTCNF2 register come up with a reset state of 1, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = XCLKIN/8 during this phase.
4. After reset, the Boot ROM code executes instructions for 1260 SYSCKOUT cycles (SYSCLKOUT = XCLKIN/2) and then samples BOOT Mode pins. Based on the status of the Boot Mode pins, the boot code branches to destination memory or boot code function in ROM. The Boot mode pins should be held high/low fro at least 2520 XCLKIN cycles from boot ROM execution time for proper selection of Boot modes. If boot ROM code executes after power on conditions (in debugger environment) the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

FIGURE 9 Timing waveforms.

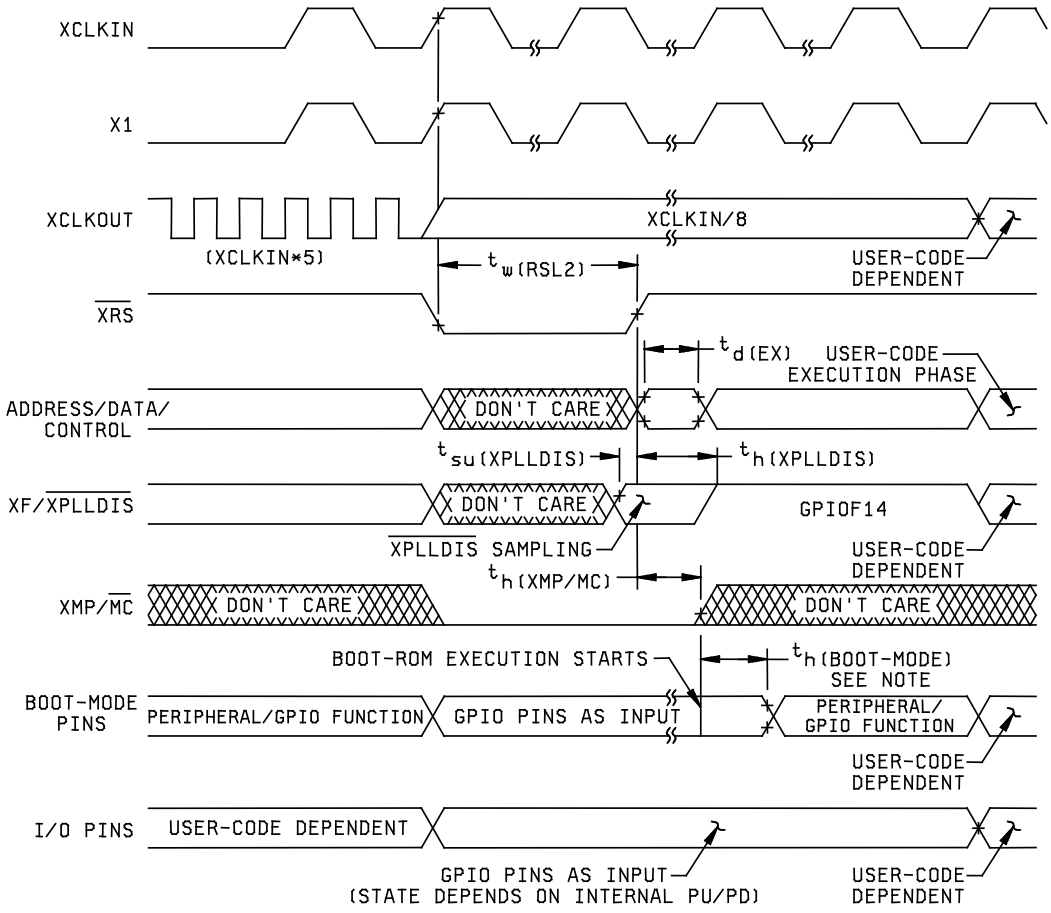


POWER-ON RESET IN MICROPROCESSOR MODE (XMP/$\overline{MC}$=1)

Notes:

1. Upon power up, SYSCLKOUT is XCLKIN/2 if the PLL is enabled. Since both the XTIMCLK and CLKMODE bits in the XINTCNF2 register come up with a reset state of 1, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = XCLKIN/8 during this phase.
2. The state of GPIO pins is undefined (i.e., they could be input or output) until the 1.8 V (or 1.9 V) supply reaches at least 1 V and 3.3 V supply reaches 2.5 V

FIGURE 10 Timing waveforms.



WARM RESET IN MICROCOMPUTER MODE

Notes:

1. After reset, the Boot ROM code executes instructions for 1260 SYSCKOUT cycles (SYSCLKOUT = XCLKIN/2) and then samples BOOT Mode pins. Based on the status of the Boot Mode pins, the boot code branches to destination memory or boot code function in ROM. The Boot mode pins should be held high/low fro at least 2520 XCLKIN cycles from boot ROM execution time for proper selection of Boot modes. If boot ROM code executes after power on conditions (in debugger environment) the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

FIGURE 11 Timing waveforms.

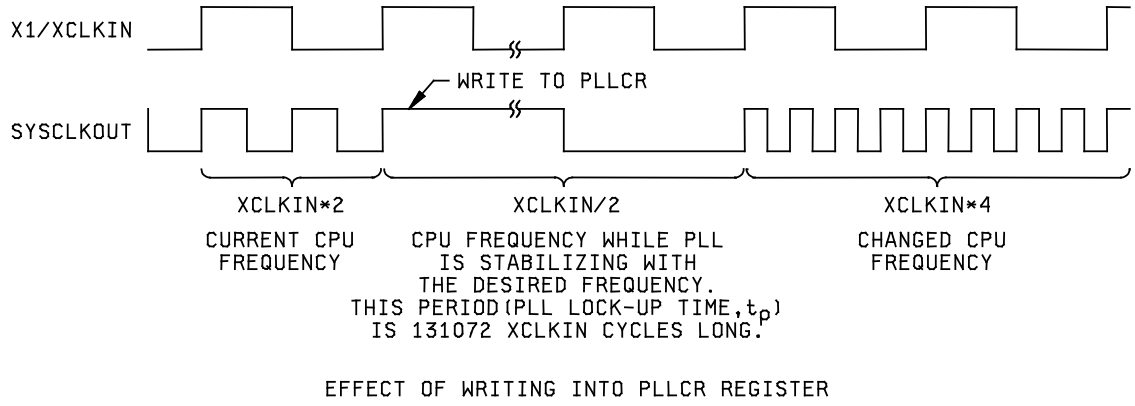


FIGURE 12 Timing waveforms.

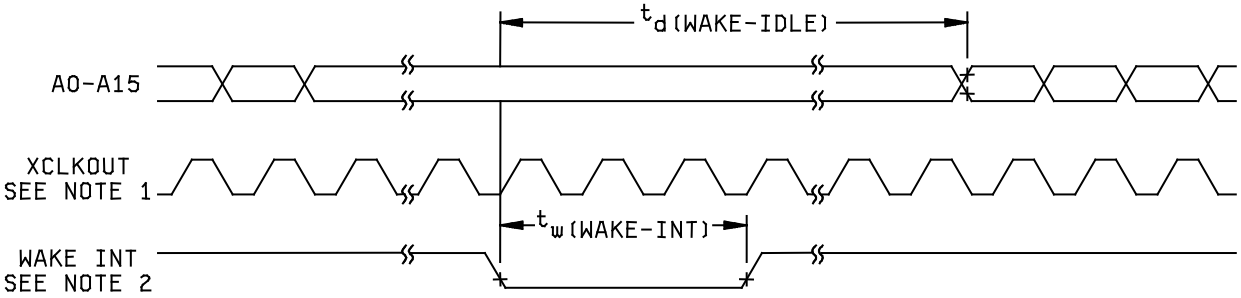
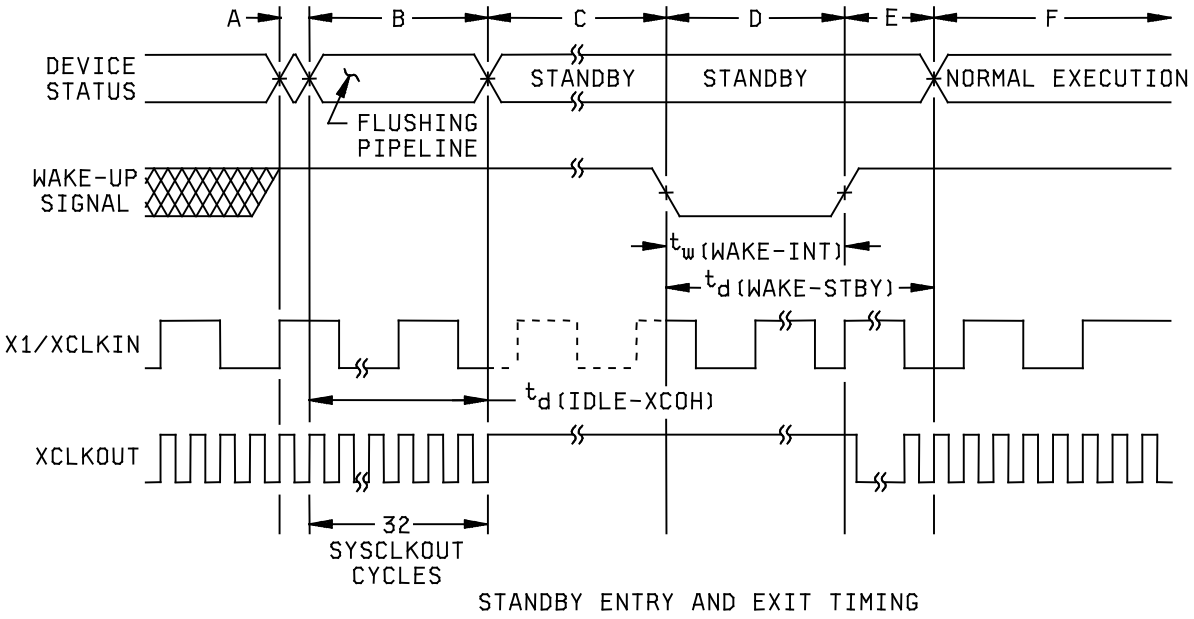


FIGURE 13 Timing waveforms.

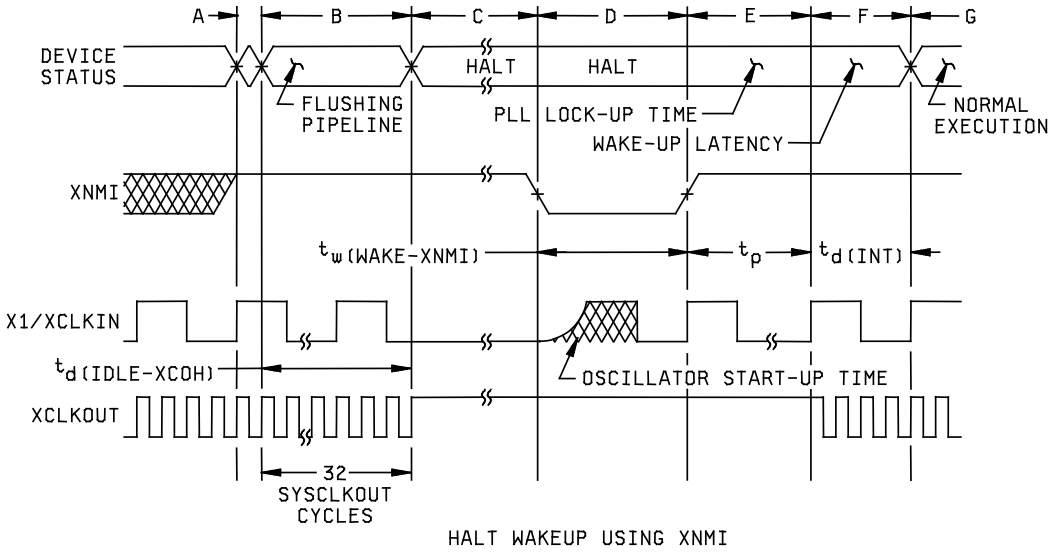


STANDBY ENTRY AND EXIT TIMING

Notes:

A. IDLE instruction is executed to put the device into STANBY mode.
B. The PLL block respond to the STANDBY signal. SYSCLKOUT is held for approximately 32 cycles before being turned off. This 32 cycle delay enables the CPU pipe and any other pending operations to flush properly.
C. The device is now in STANDBY mode.
D. The external wake up signal is driven active (negative edge triggered shown as a example).
E. After a latency period, the STANDBY mode is excited.
F. Normal operation resumes. The device will respond to the interrupt (if enabled).

FIGURE 14 Timing waveforms.



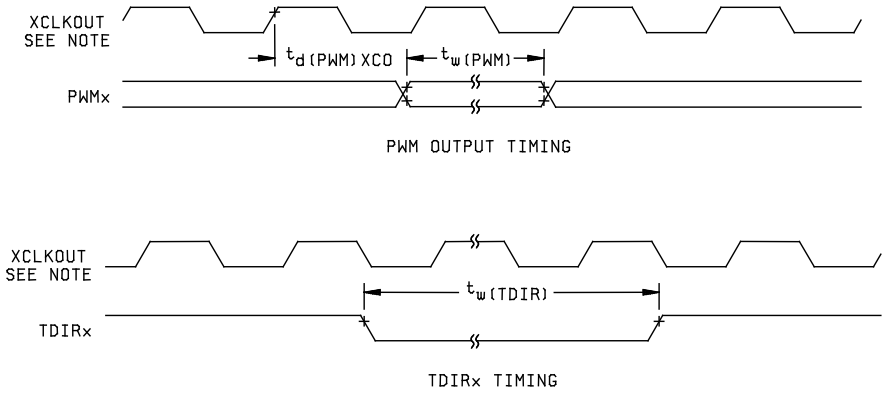
HALT WAKEUP USING XNMI

XCLKOUT = SYSCLKOUT

Notes:

A. IDLE instruction is executed to put the device into HALT mode.
B. The PLL block responds to the HALT signal. SYSCLKOUT is held for another 32 cycles before the oscillator is tuned off and the CLKIN to the core is stopped. This 32 cycle delay enables the CPU pipe and any other pending operation to flush properly.
C. Clocks to the device are turned off and the internal oscillator and PLL are shut down. The device is now in HALT mode and consumes absolute minimum power.
D. When XNMI is driven active (negative edge triggered shown, as an example), the oscillator is turned on; but the PLL is not activated.
E. When XNMI is deactivated, it initiates the PLL lock sequence, which takes 131,072 X1/XCLKIN cycles.
F. When CLKIN to the core is enabled, the device will response to the interrupt (if enabled), after a latency. The HALT mode is now exited.
G. Normal operation resumes.

FIGURE 15 Timing waveforms.



XCLKOUT = SYSCLKOUT

FIGURE 16 and 17 Timing waveforms.

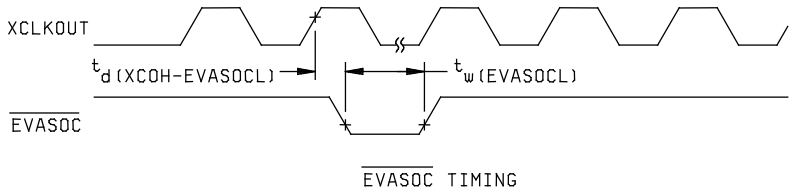


FIGURE 18 Timing waveforms.

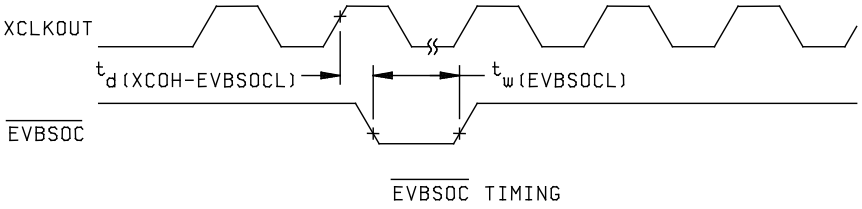
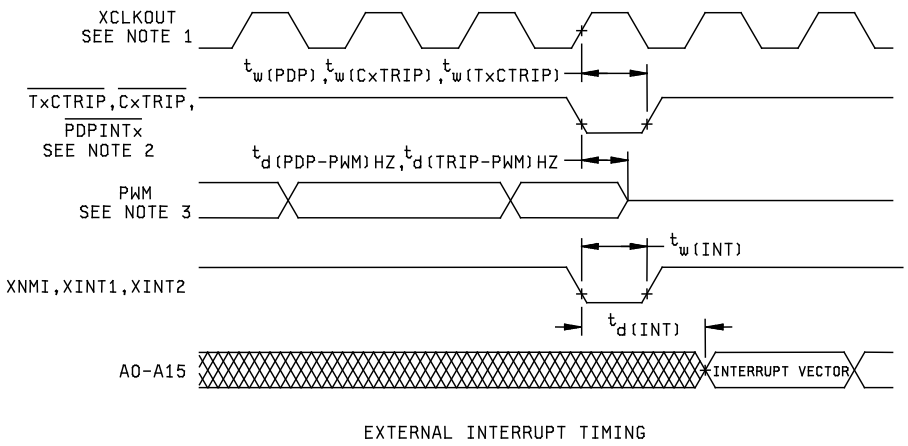


FIGURE 19 Timing waveforms.

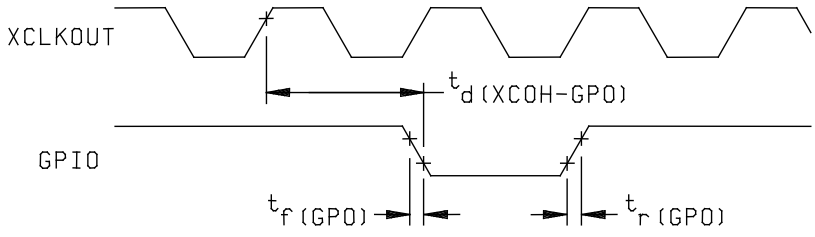


EXTERNAL INTERRUPT TIMING

Notes:

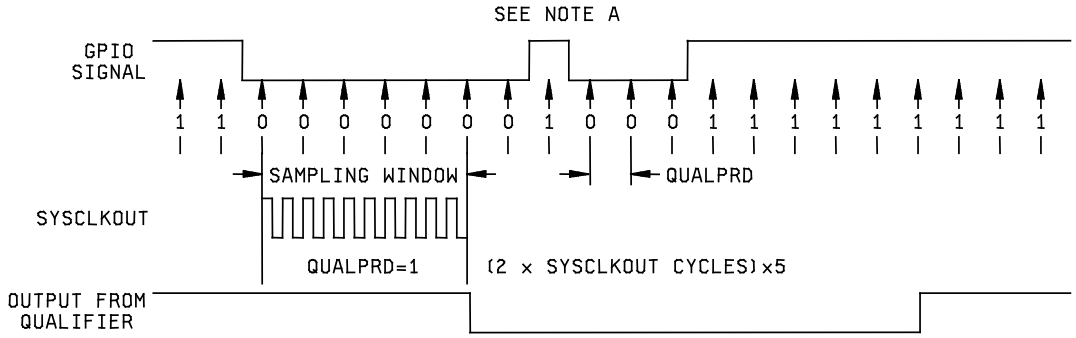
1. XCLOUT = SYSCLKOUT
2. $\overline{\text{TxCTRIP}}$ - $\overline{\text{T1CTRIP}}$, $\overline{\text{T2CTRIP}}$, $\overline{\text{T3CTRIP}}$, $\overline{\text{T4CTRIP}}$
   $\overline{\text{CxTRIP}}$ - $\overline{\text{C1TRIP}}$, $\overline{\text{C2TRIP}}$, $\overline{\text{C3TRIP}}$, $\overline{\text{C4TRIP}}$, $\overline{\text{C5TRIP}}$, or $\overline{\text{C6TRIP}}$
   $\overline{\text{PDPINTx}}$ - $\overline{\text{PDPINTA}}$ or $\overline{\text{PDPINTB}}$
3. PWM refers to all the PWM pins in the device (I.e., PWMn and TnPWM pins or PWM pin pair relevant to each $\overline{\text{CxTRIP}}$ pin.). The state of the PWNM pins after $\overline{\text{PDPINTx}}$ is taken high depends on the state of the FCOMPOE bit.

FIGURE 20 Timing waveforms.



GENERAL-PURPOSE OUTPUT TIMING

FIGURE 21 Timing waveforms.

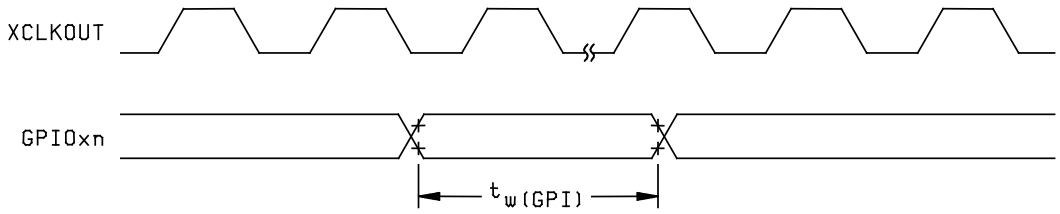


GPIO INPUT QUALIFIER-EXAMPLE DIAGRAM FOR QUALPRD=1

Notes:

A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. Input qualification is not applicable when QUALPRD = 00. For any other value 'n', the qualification sampling period in 2n SYSCLKOUT cycles (i.e., at every 2n SYSCLKOUT cycle, the GPIO pin will be sampled). Six consecutive samples must be of the same value for a given input to recognized.

B. For the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLOUT cycles. This would ensure six sampling windows for detection to occur. Since external signals are driven asynchronously, an 11 SYSCLKOUT wide pulse ensures reliable recognition.

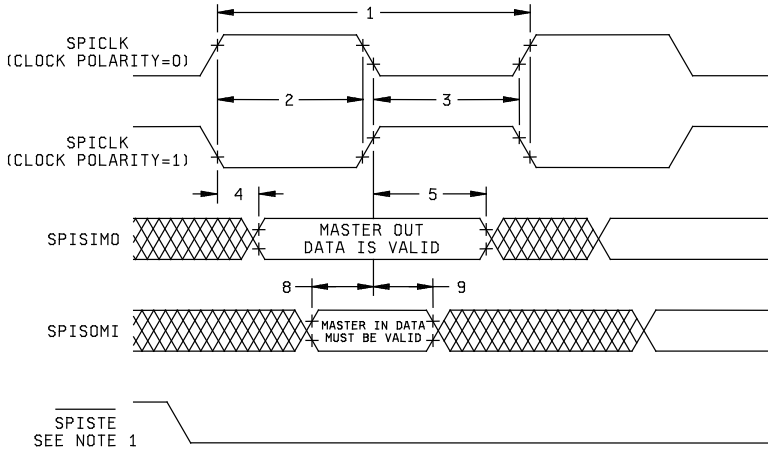


GENERAL-PURPOSE INPUT TIMING

Note:

The pulse width requirement for general purpose input is applicable for the $\overline{\text{XBIO}}$ and ADCSOC pins as well.

FIGURE 22 Timing waveforms.

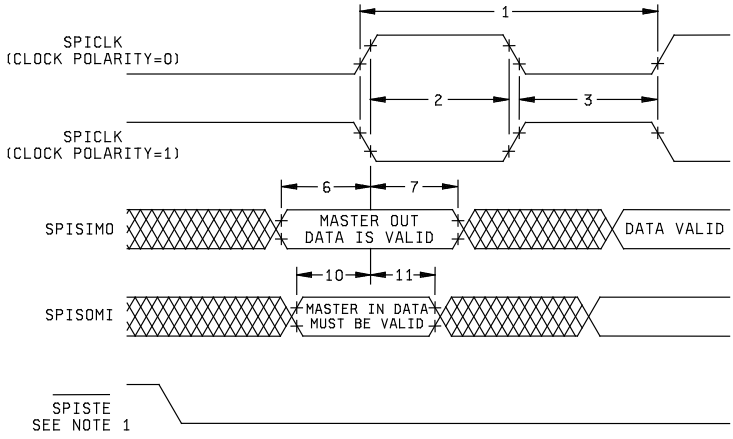


SPI MASTER MODE EXTERNAL TIMING(CLOCK PHASE=0)

Note:

1. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ before valid SPI clock edge. On the trailing end of the word, the SPITE will go inactive $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

FIGURE 23 Timing waveforms.

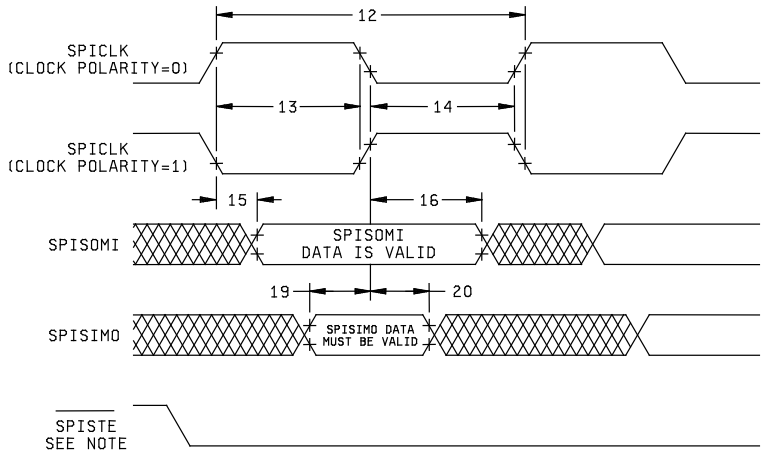


SPI SLAVE MODE EXTERNAL TIMING(CLOCK PHASE=1)

Note:

1. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ before valid SPI clock edge. On the trailing end of the word, the SPITE will go inactive $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

FIGURE 24 Timing waveforms.

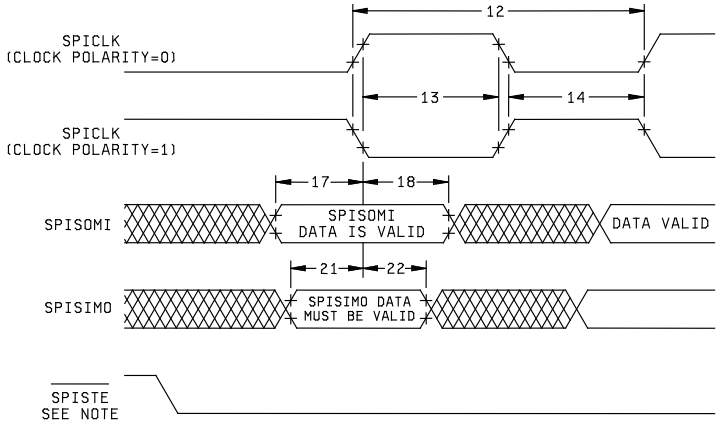


SPI SLAVE MODE EXTERNAL TIMING(CLOCK PHASE=0)

Note:

1. In the slave mode, $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

FIGURE 25. Timing waveforms.

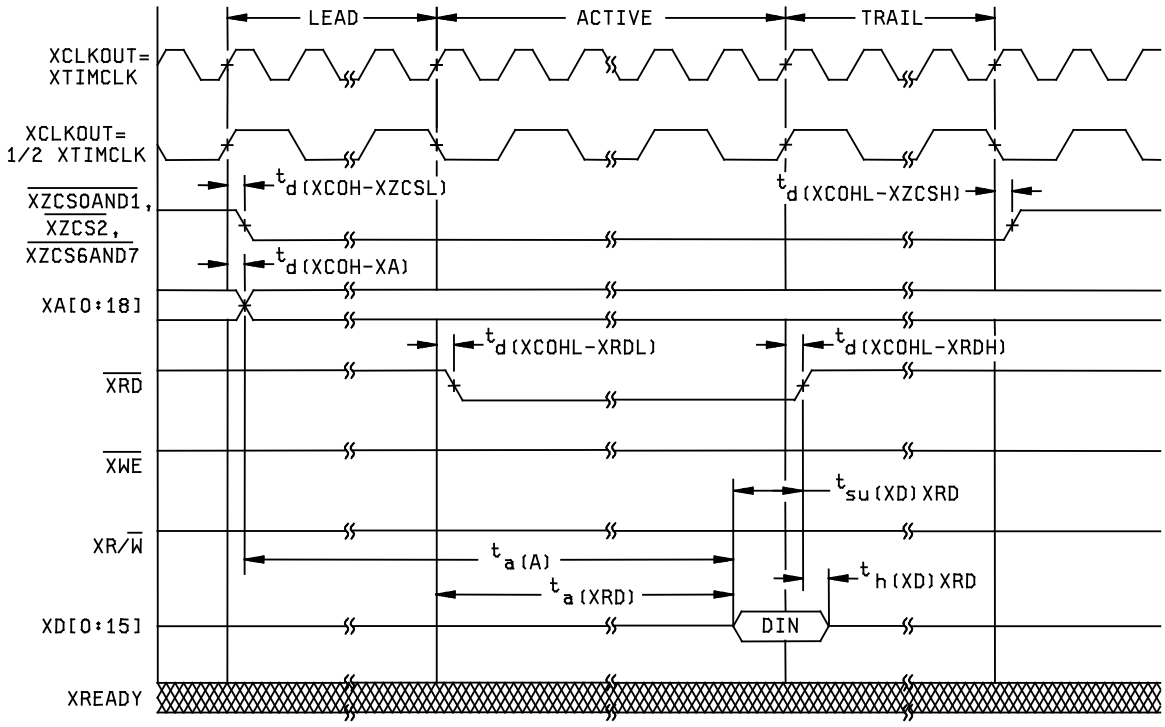


SPI SLAVE MODE EXTERNAL TIMING(CLOCK PHASE=1)

Note:

1. In the slave mode, $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after receiving edge (SPICLK) of the last data bit.

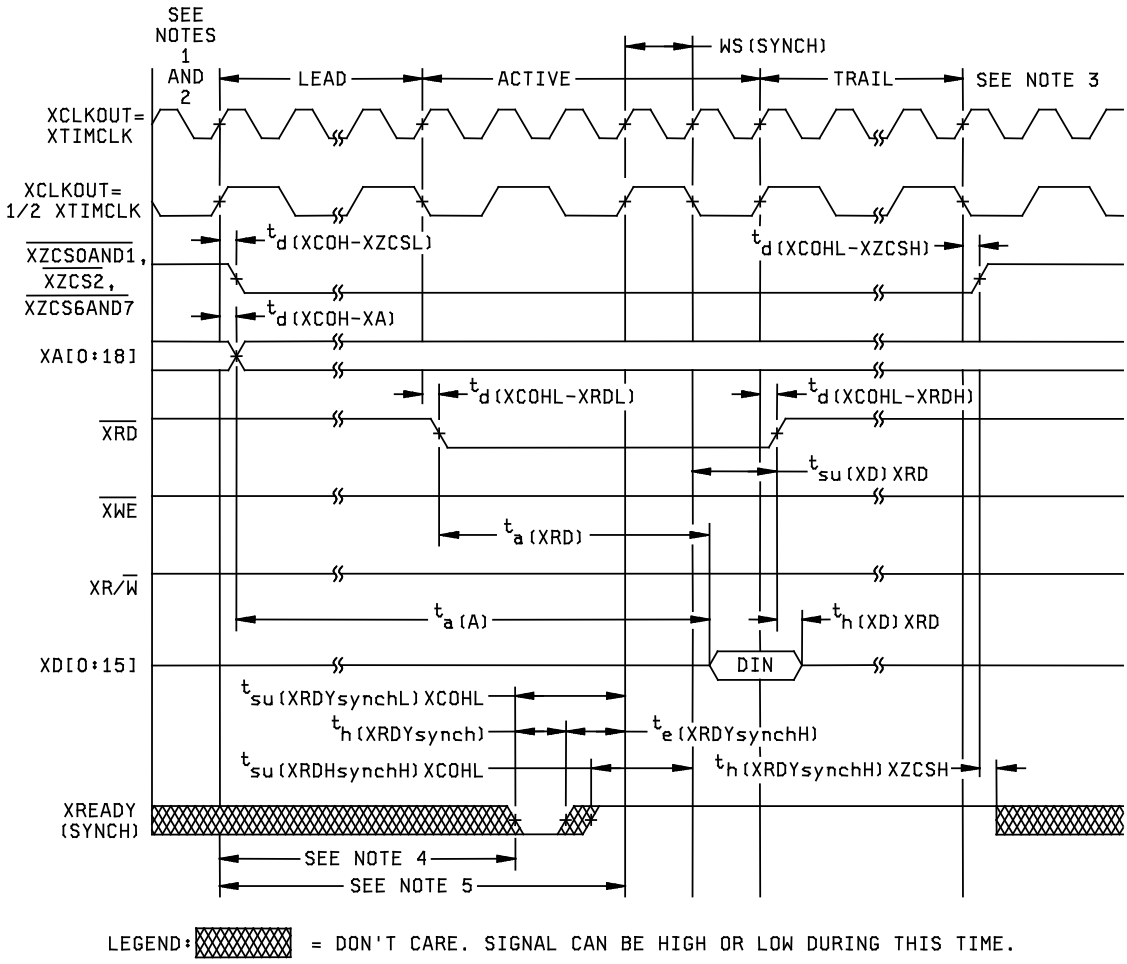
FIGURE 26. Timing waveforms.



EXAMPLE READ ACCESS

Notes:
1. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
2. During alignment cycles, all signals will transition to their inactive state.
3. For USEREADY = 0, the external XREADY input signal is ignored.
4. XA[0:18] will hold the last address put on the bus during inactive cycles, including alignment cycles.

FIGURE 27. Timing waveforms.

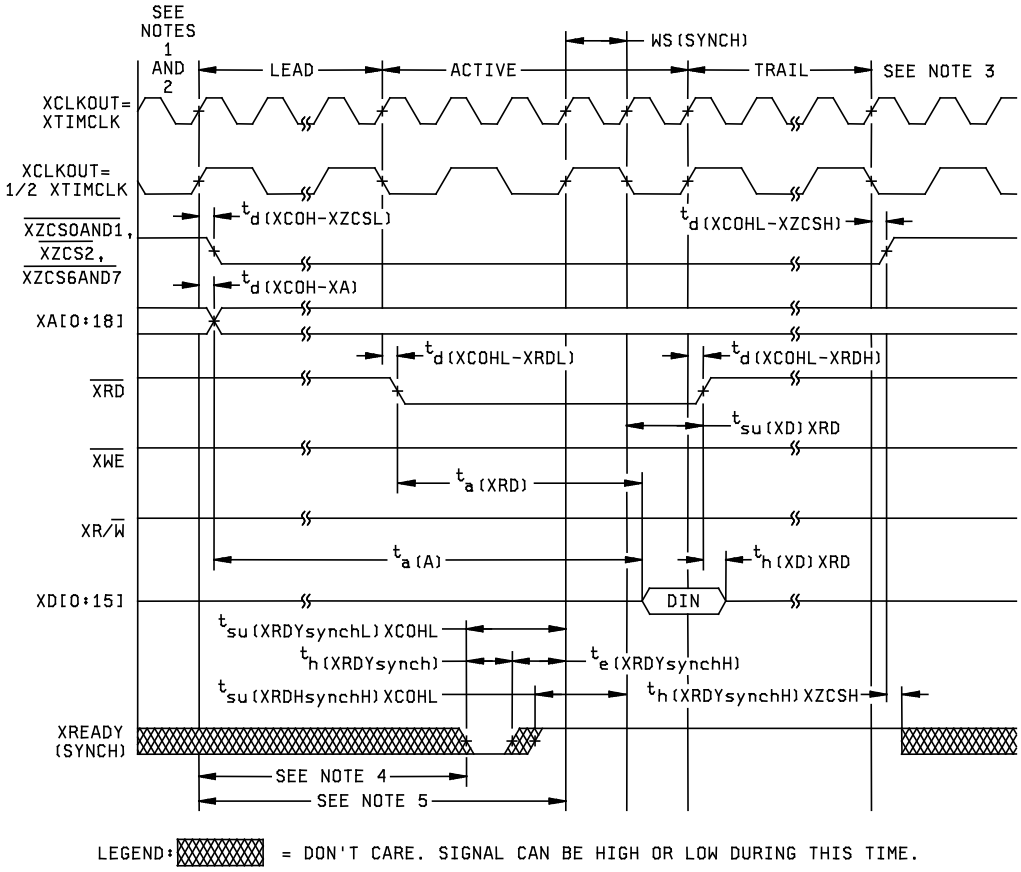


EXAMPLE READ WITH SYNCHRONOUS XREADY ACCESS

Notes:

1. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
2. During alignment cycles, all signals will transition to their inactive state.
3. For USEREADY = 0, the external XREADY input signal is ignored.
4. XA[0:18] will hold the last address put on the bus during inactive cycles, including alignment cycles.

FIGURE 28. Timing waveforms.

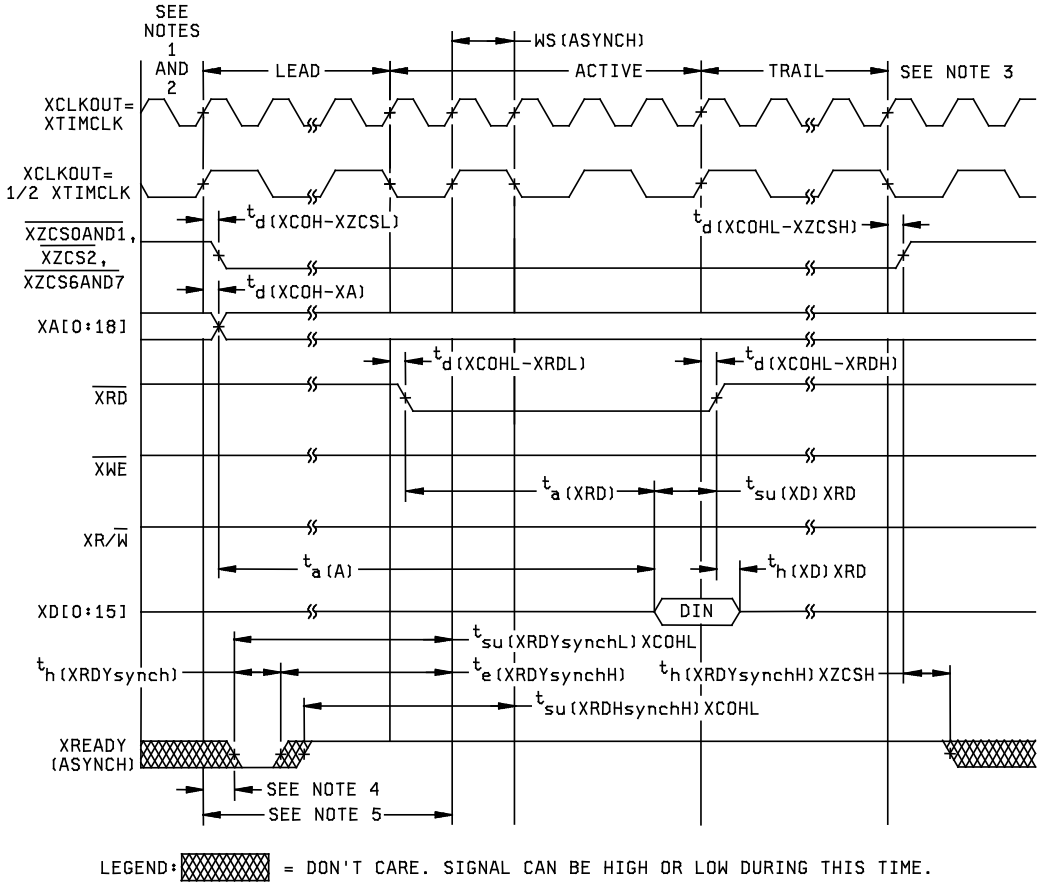


EXAMPLE READ WITH SYNCHRONOUS XREADY ACCESS

Notes:

1. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
2. During alignment cycles, all signals will transition to their inactive state
3. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.
4. For each sample, setup time from the beginning of the access (D) can be calculated as:
   $D = (XRDLEAD + XRACTIVE + n - 1)t_{c(XTIM)} - t_{su(XRDYsybnchL)XCOHL}$.
5. Reference for the first sample is with respect to this point
   $E = (XRDLEAD + XRDACTIVE)t_{c(XTIM)}$ where n is the sample number: n = 1, 2, 3, and so fourth.

FIGURE 29. Timing waveforms.



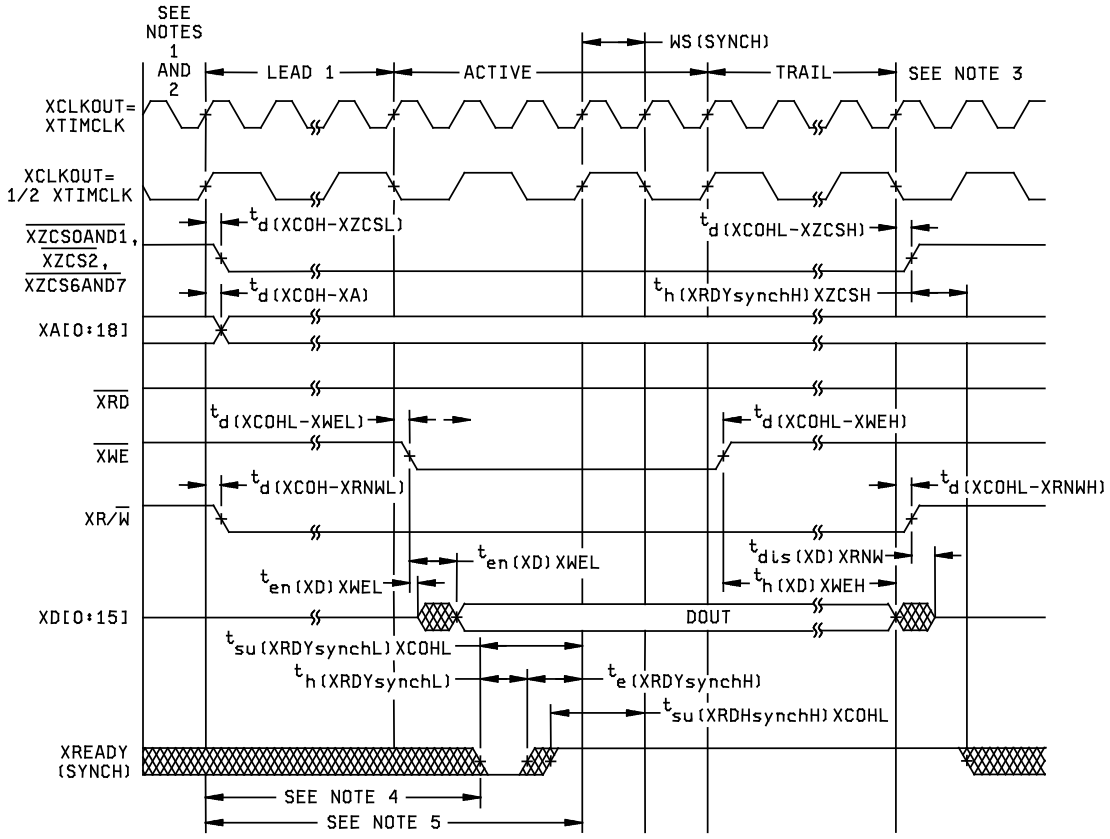
LEGEND: ▨ = DON'T CARE. SIGNAL CAN BE HIGH OR LOW DURING THIS TIME.

EXAMPLE READ WITH ASYNCHRONOUS XREADY ACCESS

Notes:

1. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
2. During alignment cycles, all signals will transition to their inactive state
3. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.
4. For each sample, setup time from the beginning of the access can be calculated as:
   D = (XRDLEAD + XRACTIVE – 3 + n)$t_{c(XTIM)}$ – $t_{su(XRDYasybnchL)XCOHL}$ where n is the sample number: n = 1, 2, 3, and so fourth.
5. Reference for the first sample is with respect to this point
   E = (XRDLEAD + XRDACTIVE - 2)$t_{c(XTIM)}$.

FIGURE 30. Timing waveforms.

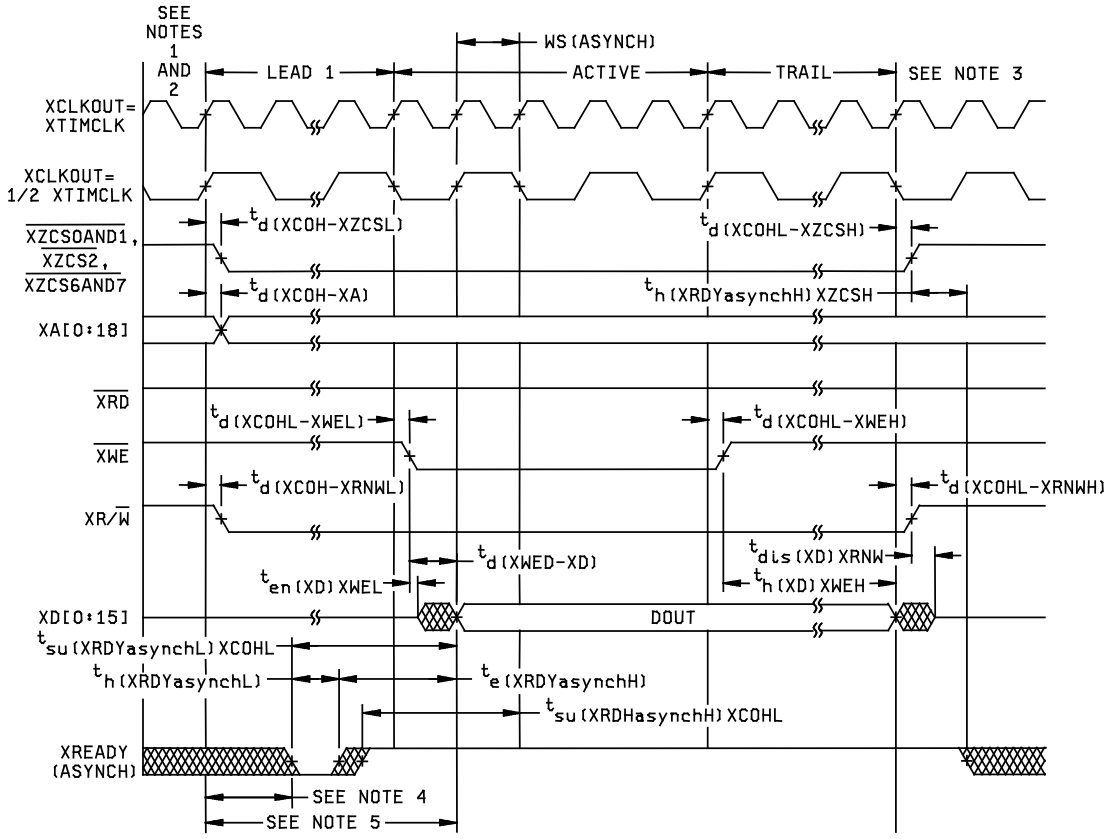


WRITE WITH SYNCHRONOUS XREADY ACCESS

Notes:

1. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
2. During alignment cycles, all signals will transition to their inactive state
3. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.
4. For each sample, setup time from the beginning of the access can be calculated as:
   D = (XRDLEAD + XRACTIVE – 3 + n)$t_{c(XTIM)}$ – $t_{su(XRDYasybnchL)XCOHL}$ where n is the sample number: n = 1, 2, 3, and so fourth.
5. Reference for the first sample is with respect to this point
   E = (XRDLEAD + XRDACTIVE - 2)$t_{c(XTIM)}$.

FIGURE 31. Timing waveforms.

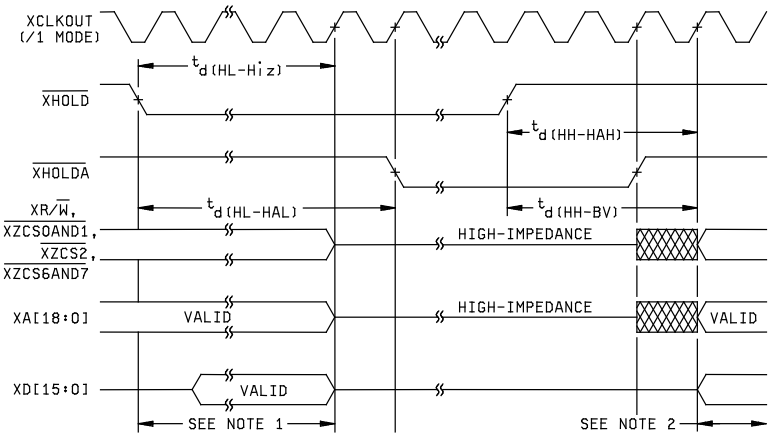


WRITE WITH ASYNCHRONOUS XREADY ACCESS

Notes:

1. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
2. During alignment cycles, all signals will transition to their inactive state
3. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.
4. For each sample, setup time from the beginning of the access can be calculated as:
   D = (XWRDLEAD + XWRACTIVE – 3 + n)$t_{c(XTIM)}$ – $t_{su(XRDYasybnchL)XCOHL}$ where n is the sample number: n = 1, 2, 3, and so fourth.
5. Reference for the first sample is with respect to this point
   E = (XWRDLEAD + XWRDACTIVE - 2)$t_{c(XTIM)}$.

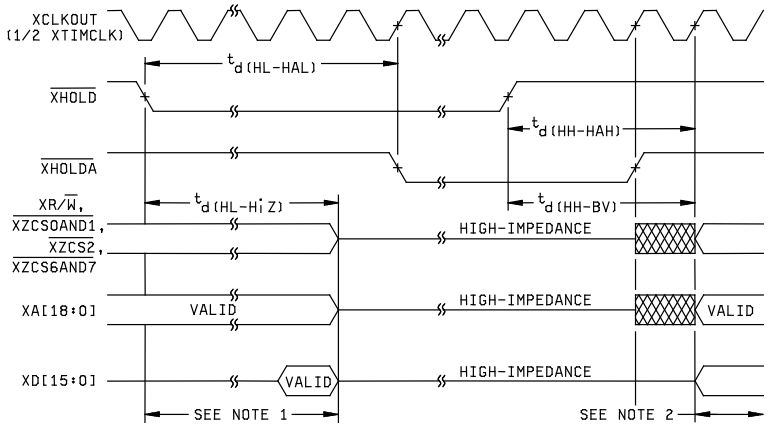
FIGURE 32. Timing waveforms.



EXTERNAL INTERFACE HOLD WAVEFORM

Notes:
1. All pending XINTF accesses are completed.
2. Normal XINTF operation resumes.

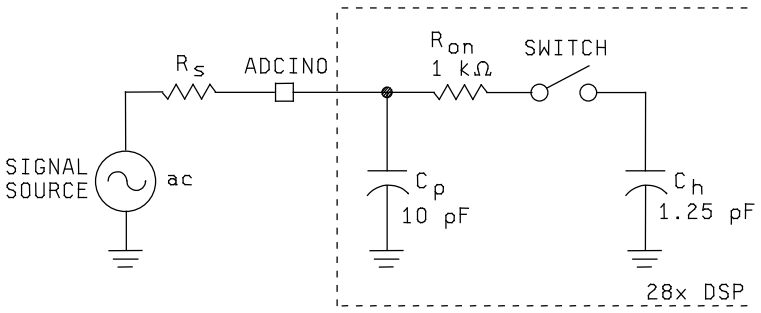
FIGURE 33. Timing waveforms.



XHOLD/XHOLDA TIMING REQUIREMENTS (XCLKOUT = 1/2 XTIMCLK)

Notes:
3. All pending XINTF accesses are completed.
4. Normal XINTF operation resumes.

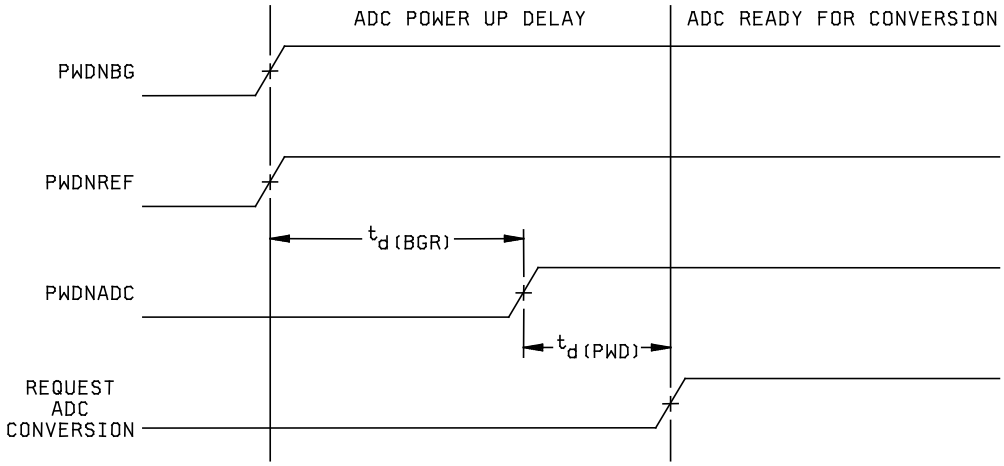
FIGURE 34. Timing waveforms.



ADC ANALOG INPUT IMPEDANCE MODEL

Typical values of the input circuit components:

Switch Resistance (R_{on}) : 1 kΩ
Sampling capacitance (C_h): 1.25 pF
Parasitic Capacitance (C_p): 10 pF
Source resistance (R_s): 50 Ω



ADC POWER-UP CONTROL BIT TIMING

FIGURE 35. Timing waveforms.

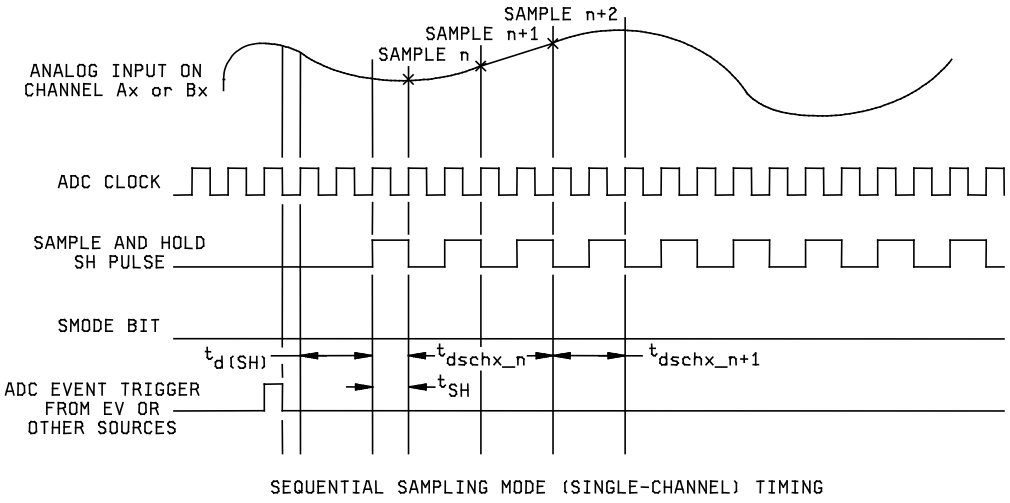


FIGURE 36. Timing waveforms.

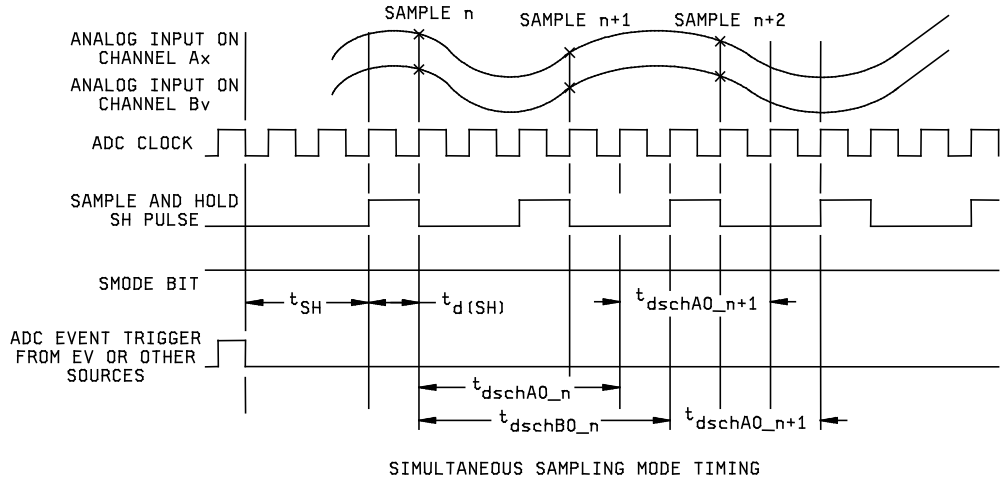


FIGURE 37. Timing waveforms.

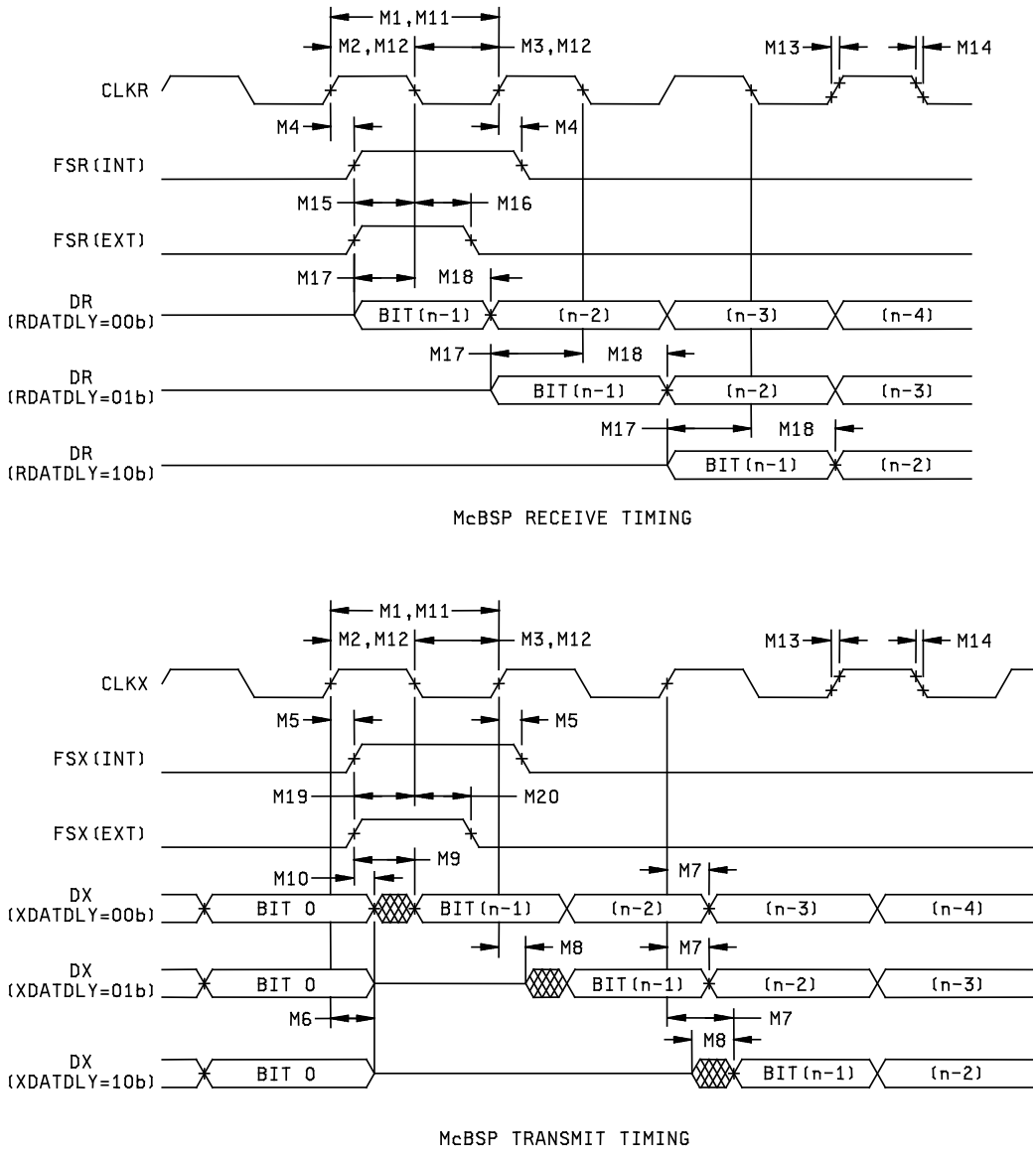
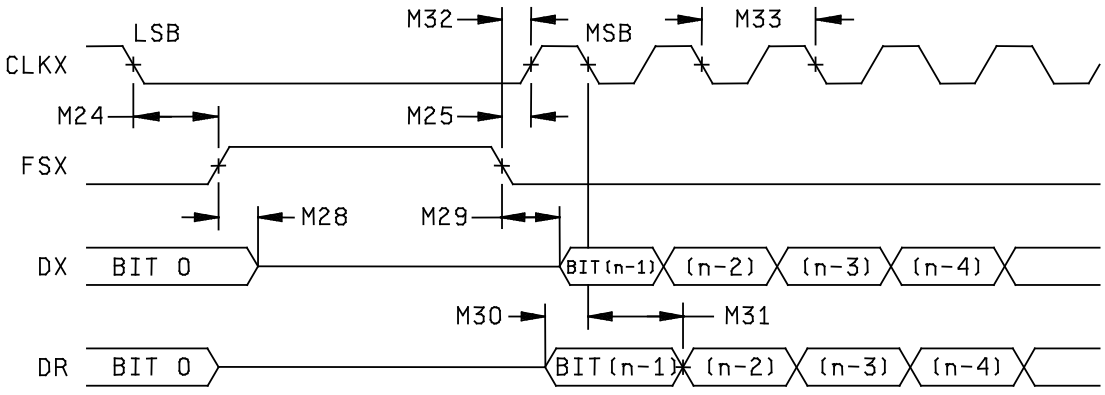
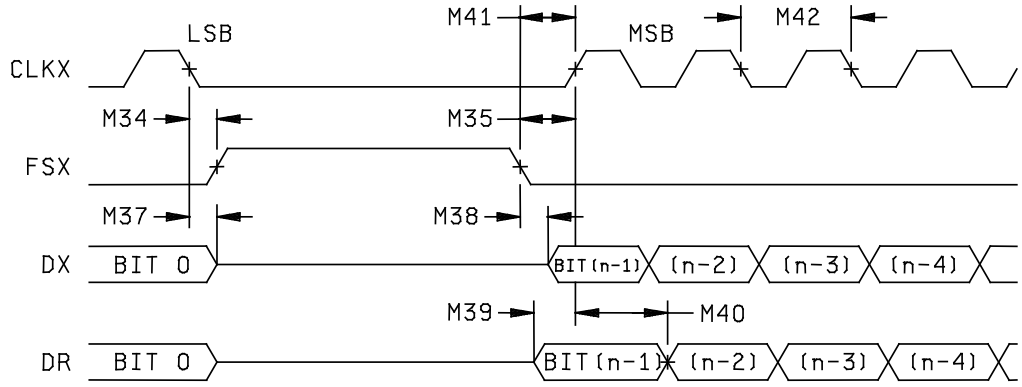


FIGURE 38. Timing waveforms.



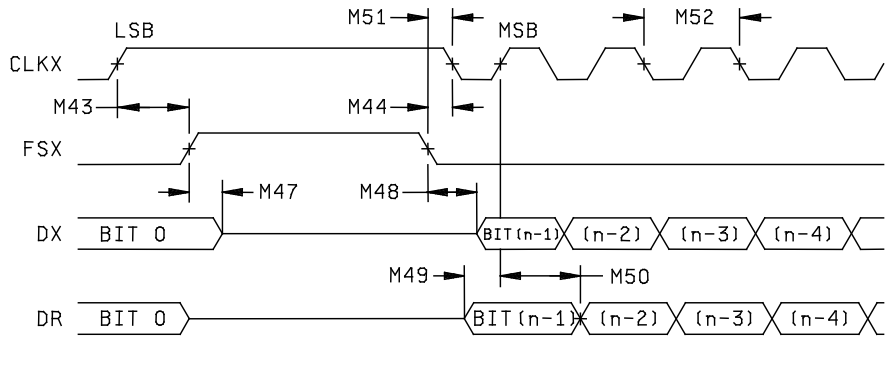
McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=10b, CLKXP=0

FIGURE 39. Timing waveforms.



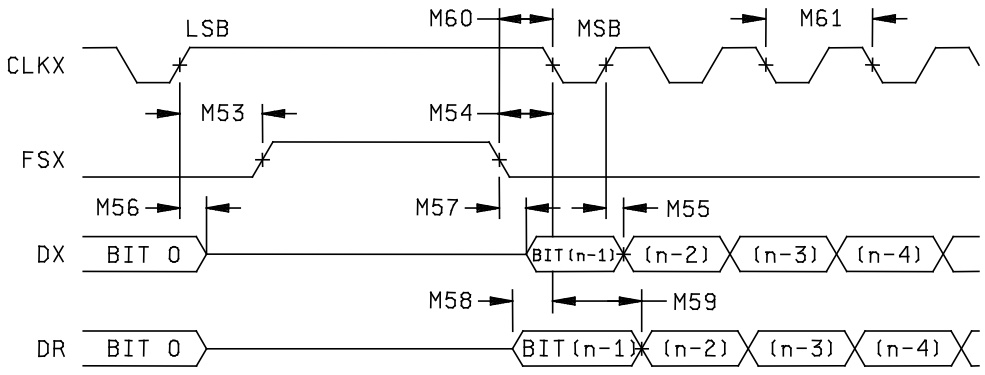
McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=11b, CLKXP=0

FIGURE 40. Timing waveforms.



McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=10b, CLKXP=1

FIGURE 41. Timing waveforms.



McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=11b, CLKXP=1

FIGURE 42. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/05601-01XE		2/
V62/05601-02XE		2/
V62/05601-03XA	01295	SM320F2812GHHMEP
V62/05601-03ZE	01295	SM320F2812PGFMEP
V62/05601-04XE		2/
V62/05601-05XE		2/
V62/05601-06XE		2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not available from a source of supplied.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243