REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device type 02. - CFS	06-07-18	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	13-09-12	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	21-01-19	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13					

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 04-12-20	**CHECKED BY** Charles F. Saffle **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, ADVANCED LOW-VOLTAGE CMOS, OCTAL 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/04763**
	REV B	**PAGE** 1 **OF** 13

AMSC N/A

5962-V021-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit bus transceiver with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C for device 01, and -55°C to +125°C for device 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04763	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74ALVCH16245-EP	16-bit bus transceiver with 3-state outputs
02	SN74ALVCH16245-EP	16-bit bus transceiver with 3-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	JEDEC MO-118	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 4.6 V
Input voltage range (V_I):
  Except I/O ports ..... -0.5 V to 4.6 V 2/
  I/O ports ..... -0.5 V to 4.6 V 2/ 3/
Output voltage range (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/ 3/
Input clamp current (I_{IK}) (V_I < 0) ..... –50 mA
Output clamp current (I_{OK}) (V_O < 0) ..... –50 mA
Continuous output current (I_O) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Package thermal impedance (θ_{JA}) ..... 63°C/W 4/
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}) ..... 1.65 V to 3.6 V
Minimum high-level input voltage (V_{IH}):
  V_{CC} = 1.65 V to 1.95 V ..... 0.65 x V_{CC}
  V_{CC} = 2.3 V to 2.7 V ..... 1.7 V
  V_{CC} = 2.7 V to 3.6 V ..... 2 V
Maximum low-level input voltage (V_{IL}):
  V_{CC} = 1.65 V to 1.95 V ..... 0.35 x V_{CC}
  V_{CC} = 2.3 V to 2.7 V ..... 0.7 V
  V_{CC} = 2.7 V to 3.6 V ..... 0.8 V
Input voltage range (V_I) ..... 0 V to V_{CC}
Output voltage range (V_O) ..... 0 V to V_{CC}
Maximum high-level output current (I_{OH}):
  V_{CC} = 1.65 V ..... -4 mA
  V_{CC} = 2.3 V ..... -12 mA
  V_{CC} = 2.7 V ..... -12 mA
  V_{CC} = 3 V ..... -24 mA
Maximum low-level output current (I_{OL}):
  V_{CC} = 1.65 V ..... 4 mA
  V_{CC} = 2.3 V ..... 12 mA
  V_{CC} = 2.7 V ..... 12 mA
  V_{CC} = 3 V ..... 24 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) ..... 10 ns/V
Operating free-air temperature range (T_A):
  Device 01 ..... -40°C to +85°C
  Device 02 ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ This value is limited to 4.6 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org .)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions Device 01: $-40°C \le T_A \le +85°C$ Device 02: $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -100 μA	1.65 V to 3.6 V	All	V_{CC} – 0.2		V
		I_{OH} = -4 mA	1.65 V		1.2		
		I_{OH} = -6 mA	2.3 V		2		
		I_{OH} = -12 mA	2.3 V		1.7		
			2.7 V		2.2		
			3 V		2.4		
		I_{OH} = -24 mA	3 V		2		
Low level output voltage	V_{OL}	I_{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 6 mA	2.3 V			0.4	
		I_{OL} = 12 mA	2.3 V			0.7	
			2.7 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
Input current	I_I	$V_I = V_{CC}$ or GND	3.6V			±5	μA
Input hold current	$I_{I(hold)}$	V_I = 0.58 V	1.65 V		25		μA
		V_I = 1.07 V	1.65 V		-25		
		V_I = 0.7 V	2.3 V		45		
		V_I = 1.7 V	2.3 V		-45		
		V_I = 0.8 V	3 V		75		
		V_I = 2 V	3 V		-75		
		V_I = 0 to 3.6 V 2/	3.6 V			±500	
Off-state output current	I_{OZ} 3/	$V_O = V_{CC}$ or GND	3.6 V			±10	μA
Quiescent supply current	I_{CC}	$V_I = V_{CC}$ or GND I_O = 0 A	3.6 V			40	μA
Quiescent supply current delta	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions Device 01: $-40°C \le T_A \le +85°C$ Device 02: $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Input capacitance	C_I	Control inputs $V_I = V_{CC}$ or GND $T_A = 25°C$	3.3 V	All	4 TYP		pF
Input/output capacitance	C_{IO}	A or B ports $V_O = V_{CC}$ or GND $T_A = 25°C$	3.3 V		8 TYP		pF
Power dissipation capacitance	C_{pd}	Outputs enabled $C_L = 50$ pF f = 10 MHz $T_A = 25°C$	2.5 V		22 TYP		pF
			3.3 V		29 TYP		
		Outputs disabled $C_L = 50$ pF f = 10 MHz $T_A = 25°C$	2.5 V		4 TYP		
			3.3 V		5 TYP		
Propagation delay time, A or B to B or A	t_{pd}	See figure 5.	2.5 V ±0.2 V	01	1	3.7	ns
			2.7 V			3.6	
			3.3 V ±0.3 V		1	3	
Propagation delay time, output enable, OE to A or B	t_{en}	See figure 5.	2.5 V ±0.2 V		1	5.7	ns
			2.7 V			5.4	
			3.3 V ±0.3 V		1	4.4	
Propagation delay time, output disable, OE to A or B	t_{dis}	See figure 5.	2.5 V ±0.2 V		1	5.2	ns
			2.7 V			4.6	
			3.3 V ±0.3 V		1	4.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

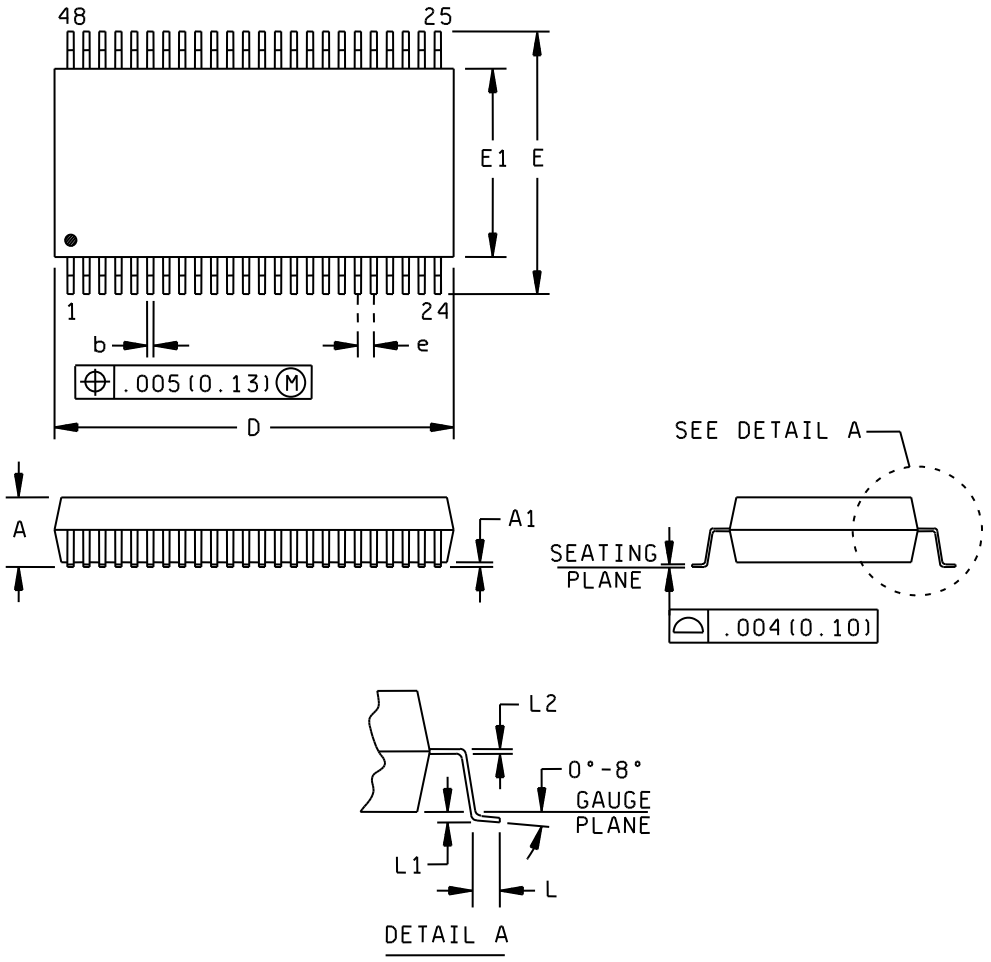
Test	Symbol	Conditions Device 01: $-40°C \le T_A \le +85°C$ Device 02: $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Propagation delay time, A or B to B or A	t_{pd}	See figure 5.	2.5 V ±0.2 V	02	1	4.5	ns
			3.3 V ±0.3 V		1	4.0	
Propagation delay time, output enable, $\overline{OE}$ to A or B	t_{en}	See figure 5.	2.5 V ±0.2 V		1	8.2	ns
			3.3 V ±0.3 V		1	5.5	
Propagation delay time, output disable, $\overline{OE}$ to A or B	t_{dis}	See figure 5.	2.5 V ±0.2 V		1	7.5	ns
			3.3 V ±0.3 V		1	5.0	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

3/ For I/O ports, the parameter I_{OZ} includes the input leakage current.

Case X



NOTES:
1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-118.
3. All linear dimensions are shown in inches (millimeters). Millimeters equivalents are given for general information only.
4. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 millimeters).

FIGURE 1. Case outline.

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.110	---	2.79
A1	0.008	---	0.20	---
b	0.008	0.0135	0.203	0.343
D	0.620	0.630	15.75	16.00
E	0.395	0.420	10.03	10.67
E1	0.291	0.299	7.39	7.59
e	0.025 BSC		0.635 BSC	
L	0.020	0.040	0.51	1.02
L1	0.010 TYP		0.25 TYP	
L2	0.005	0.010	0.13	0.25

FIGURE 1. Case outline - Continued.

(each 8-bit section)

Inputs		Operation
$\overline{OE}$	DIR	
L	H	B data to A bus
L	L	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage level
X = Immaterial

FIGURE 2. Function table.

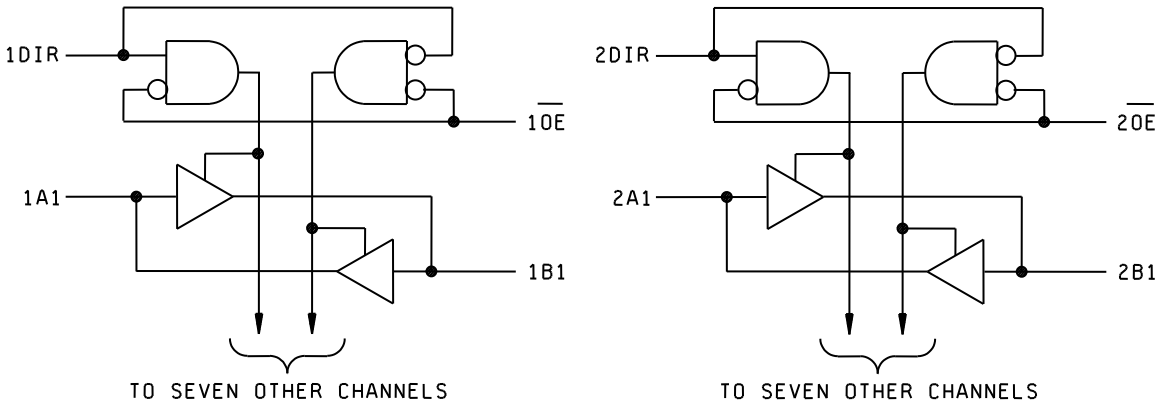
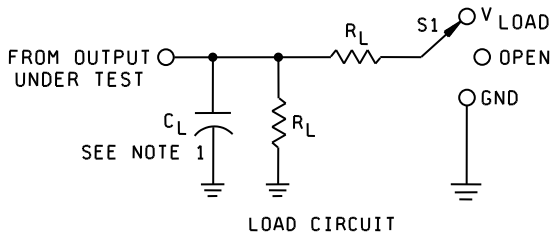


FIGURE 3. Logic diagram.

Device types:	01 and 02		
Case outlines:	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1DIR	25	$\overline{2OE}$
2	1B1	26	2A8
3	1B2	27	2A7
4	GND	28	GND
5	1B3	29	2A6
6	1B4	30	2A5
7	V_{CC}	31	V_{CC}
8	1B5	32	2A4
9	1B6	33	2A3
10	GND	34	GND
11	1B7	35	2A2
12	1B8	36	2A1
13	2B1	37	1A8
14	2B2	38	1A7
15	GND	39	GND
16	2B3	40	1A6
17	2B4	41	1A5
18	V_{CC}	42	V_{CC}
19	2B5	43	1A4
20	2B6	44	1A3
21	GND	45	GND
22	2B7	46	1A2
23	2B8	47	1A1
24	2DIR	48	$\overline{1OE}$

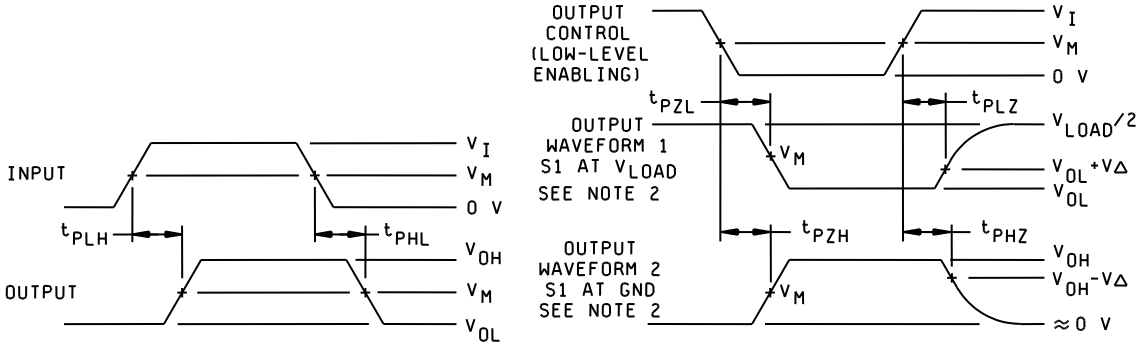
FIGURE 4. Terminal connections.



LOAD CIRCUIT

TEST	S1
t_{pd}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	30 pF	500Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
3 V ±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V



NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50Ω.
4. The outputs are measured one at a time, with one input transition per measurement.
5. t_{PLH} and t_{PHL} are the same as t_{pd}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

FIGURE 5. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04763-01XE	01295	CALVCH16245IDLREP	ALVCH16245
V62/04763-02XE	01295	CALVCH16245MDLREP	ALCH16245M

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243