

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-09-19	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-11-28	Thomas M. Hess



CURRENT DESIGN ACTIVITY CAGE CODE 16236
 HAS CHANGED NAMES TO:
 DLA LAND AND MARITIME
 COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	PREPARED BY Charles F. Saffle	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 04-12-09	CHECKED BY Charles F. Saffle	TITLE MICROCIRCUIT, DIGITAL, ADVANCED HIGH SPEED CMOS, OCTAL BUFFER/DRIVER, WITH 3-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/04761
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal buffer/driver with 3-state outputs, TTL compatible inputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/04761</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74AHCT541-EP	Octal buffer/driver with 3-state outputs, TTL compatible inputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	JEDEC MS-013	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Output voltage range (V_O)	-0.5 V to $V_{CC} + 0.5 V$ 2/
Input clamp current (I_{IK}) ($V_I < 0$)	-20 mA
Output clamp current (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current (I_O) ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Package thermal impedance (θ_{JA})	58°C/W 3/
Storage temperature range (T_{STG})	-65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Minimum high-level input voltage (V_{IH}).....	2 V
Maximum low-level input voltage (V_{IL}).....	0.8 V
Input voltage range (V_I).....	0 V to 5.5 V
Output voltage range (V_O).....	0 V to V_{CC}
Maximum high-level output current (I_{OH})	-8 mA
Maximum low-level output current (I_{OL}).....	8 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$)	20 ns/V
Operating free-air temperature range (T_A)	-40°C to +85°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	I _{OH} = -50 μA	4.5 V	25°C, -40°C to 85°C	4.4		V
		I _{OH} = -8 mA	4.5 V	25°C	3.94		
				-40°C to 85°C	3.8		
Low level output voltage	V _{OL}	I _{OL} = 50 μA	4.5 V	25°C, -40°C to 85°C		0.1	V
		I _{OL} = 8 mA	4.5 V	25°C		0.36	
				-40°C to 85°C		0.44	
Input current	I _I	V _I = 5.5 V or GND	0 V to 5.5 V	25°C		±0.1	μA
				-40°C to 85°C		±1	
Off-state output current	I _{oz}	V _O = V _{CC} or GND	5.5 V	25°C		±0.25	μA
				-40°C to 85°C		±2.5	
Quiescent supply current	I _{CC}	V _I = V _{CC} or GND I _O = 0 A	5.5 V	25°C		4	μA
				-40°C to 85°C		40	
Quiescent supply current delta	ΔI _{CC} 2/	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V	25°C		1.35	mA
				-40°C to 85°C		1.5	
Input capacitance	C _I	V _I = V _{CC} or GND	5 V	25°C	2 TYP 3/		pF
				-40°C to 85°C		10	
Output capacitance	C _O	V _O = V _{CC} or GND	5 V	25°C	4 TYP		pF
Power dissipation capacitance	C _{pd}	C _L = 50 pF f = 1 MHz	5 V	25°C	12 TYP		pF
Propagation delay time, A to Y	t _{PLH}	C _L = 15 pF See figure 5.	4.5 V and 5.5 V	25°C		6	ns
				-40°C to 85°C	1	6.5	
	t _{PHL}	C _L = 15 pF See figure 5.	4.5 V and 5.5 V	25°C		5.5	ns
				-40°C to 85°C	1	6.5	
	t _{PLH}	C _L = 50 pF See figure 5.	4.5 V and 5.5 V	25°C		8.5	ns
				-40°C to 85°C	1	9.5	
	t _{PHL}	C _L = 50 pF See figure 5.	4.5 V and 5.5 V	25°C		8.5	ns
				-40°C to 85°C	1	9.5	
Propagation delay time, output enable, OE to Y	t _{PZH}	C _L = 15 pF See figure 5.	4.5 V and 5.5 V	25°C		7	ns
				-40°C to 85°C	1	8	
	t _{PZL}	C _L = 15 pF See figure 5.	4.5 V and 5.5 V	25°C		7	ns
				-40°C to 85°C	1	8	
	t _{PZH}	C _L = 50 pF See figure 5.	4.5 V and 5.5 V	25°C		10	ns
				-40°C to 85°C	1	12	
	t _{PZL}	C _L = 50 pF See figure 5.	4.5 V and 5.5 V	25°C		10	ns
				-40°C to 85°C	1	12	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Limits		Unit
					Min	Max	
Propagation delay time, output disable, OE to Y	t _{PZH}	C _L = 15 pF See figure 5.	4.5 V and 5.5 V	25°C		7	ns
				-40°C to 85°C	1	8	
	t _{PZL}		4.5 V and 5.5 V	25°C		7	
				-40°C to 85°C	1	8	
	t _{PZH}	C _L = 50 pF See figure 5.	4.5 V and 5.5 V	25°C		10	
				-40°C to 85°C	1	12	
	t _{PZL}		4.5 V and 5.5 V	25°C		10	
				-40°C to 85°C	1	12	
Output skew time	t _{sk(o)}	C _L = 50 pF	4.5 V and 5.5 V	25°C		1	ns
				-40°C to 85°C		1	

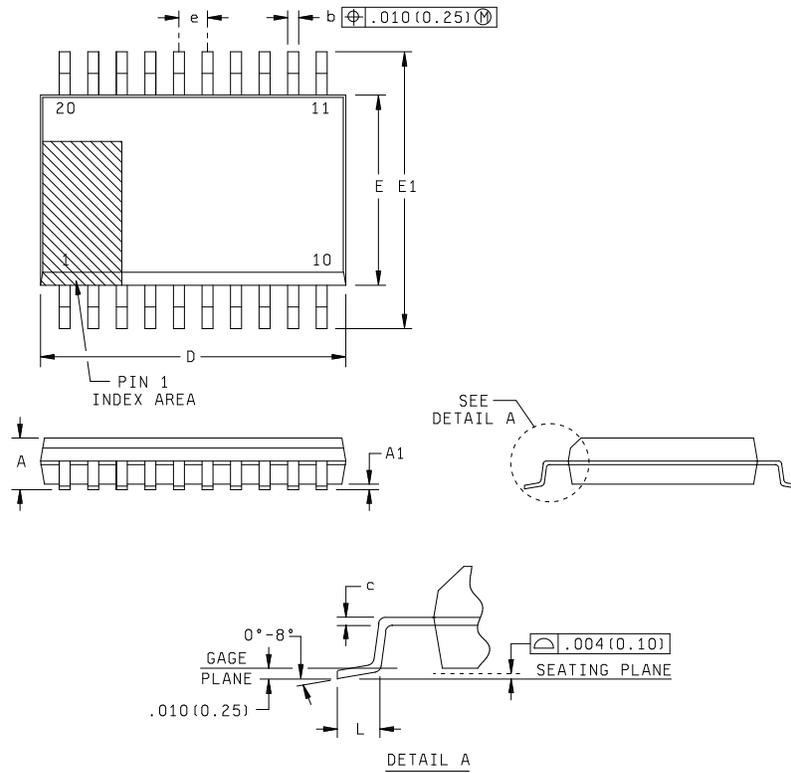
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

3/ The maximum limit is 10 pF.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	.104	---	2.65	E	.291	.299	7.40	7.60
A1	.004	.012	0.10	0.30	E1	.393	.419	9.97	10.63
b	.012	.020	0.31	0.51	e	.050 BSC		1.27 BSC	
c	.008	.013	0.20	0.33	L	.016	.050	0.40	1.27
D	.496	.512	12.60	13.00					

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-013.
3. All linear dimensions are shown in inches (millimeters). Millimeters equivalents are given for general information only.
4. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 millimeters).

FIGURE 1. Case outline.

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(each buffer/driver)

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = High voltage level
L = Low voltage level

X = Immaterial
Z = High impedance state

FIGURE 2. Function table.

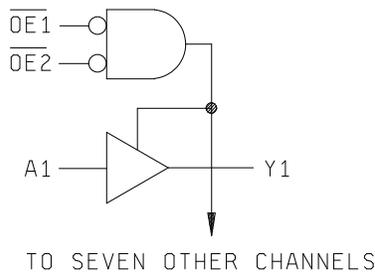
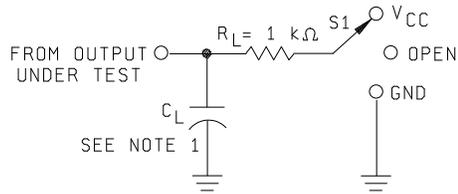


FIGURE 3. Logic diagram.

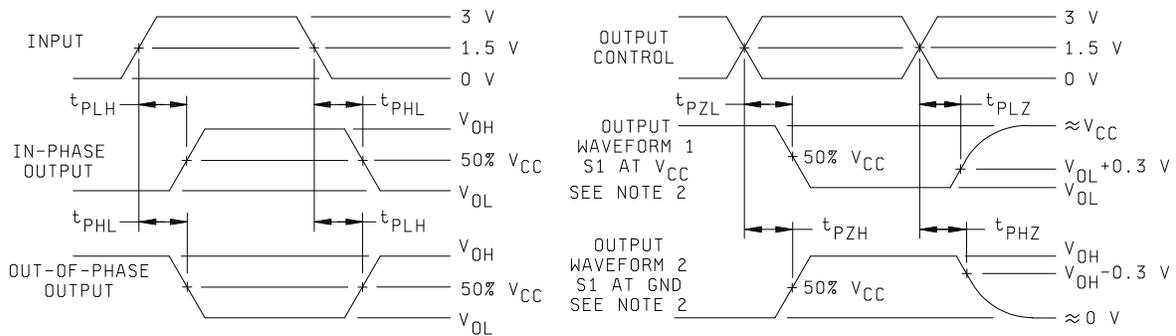
Device type		01	
Case outline		X	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{OE1}$	11	Y8
2	A1	12	Y7
3	A2	13	Y6
4	A3	14	Y5
5	A4	15	Y4
6	A5	16	Y3
7	A6	17	Y2
8	A7	18	Y1
9	A8	19	$\overline{OE2}$
10	GND	20	V _{CC}

FIGURE 4. Terminal connections.

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TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V _{CC}
t_{PHZ}/t_{PZH}	GND



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_o = 50\Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
4. The outputs are measured one at a time, with one input transition per measurement.

FIGURE 5. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04761-01XE	01295	SN74AHCT541IDWREP	AHCT541EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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