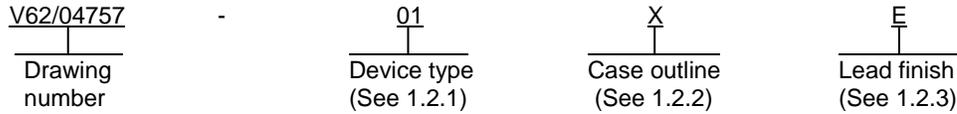


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1-line to 10-line clock driver with 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	CDC2351-EP	1-line to 10-line clock driver with 3-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	24	JEDEC MO-150	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 4.6 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high state or power-off state (V_O)	-0.5 V to 3.6 V 2/
Current into any output in the low state (I_O)	24 mA
Input clamp current (I_{IK}) ($V_I < 0$)	-18 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (P_D) (in still air)	0.65 W 3/
Storage temperature range (T_{STG})	-65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

3/ The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	3 V to 3.6 V
Minimum high-level input voltage (V_{IH}).....	2 V
Maximum low-level input voltage (V_{IL}).....	0.8 V
Input voltage range (V_I).....	0 V to 5.5 V
Maximum high-level output current (I_{OH})	-12 mA
Maximum low-level output current (I_{OL}).....	12 mA
Maximum input clock frequency (f_{clock})	100 MHz
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

4/ Unused pins (input or I/O) must be held high or low.

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3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit	
						Min	Max		
Input clamp voltage	V _{IK}	I _I = -18 mA	3 V	25°C, -55°C to 125°C	All		-1.2	V	
High level output voltage	V _{OH}	I _{OH} = -12 mA	3 V			2		V	
Low level output voltage	V _{OL}	I _{OL} = 12 mA	3 V				0.8	V	
Input current	I _I	V _I = V _{CC} or GND	3.6 V				±1	μA	
Output current	I _O <u>2/</u>	V _O = 2.5 V	3.6 V				-7	-70	mA
Off-state output current	I _{OZ}	V _O = 3 V or 0 V	3.6 V					±10	μA
Quiescent supply current	I _{CC}	Outputs high. V _I = V _{CC} or GND I _O = 0 A	3.6 V					0.3	mA
		Outputs low. V _I = V _{CC} or GND I _O = 0 A				15			
		Outputs disabled. V _I = V _{CC} or GND I _O = 0 A				0.3			
Input capacitance	C _i	V _I = V _{CC} or GND f = 10 MHz	3.3 V	25°C	4 TYP		pF		
Output capacitance	C _o	V _O = V _{CC} or GND f = 10 MHz			6 TYP		pF		
Propagation delay time, A to Y	t _{PLH}	C _L = 50 pF See figure 5.	3.3 V	25°C	3.8	4.8	ns		
			3 V to 3.6 V	-55°C to 125°C	1.1	11			
	3.3 V		25°C	3.6	4.6				
	3 V to 3.6 V		-55°C to 125°C	1	9.7				
Propagation delay time, output enable, \overline{OE} to Y	t _{PZH}	C _L = 50 pF See figure 5.	3.3 V	25°C	2.4	6	ns		
			3 V to 3.6 V	-55°C to 125°C	1	12			
	3.3 V		25°C	2.4	6				
	3 V to 3.6 V		-55°C to 125°C	1	11.1				

See footnotes at end of table.

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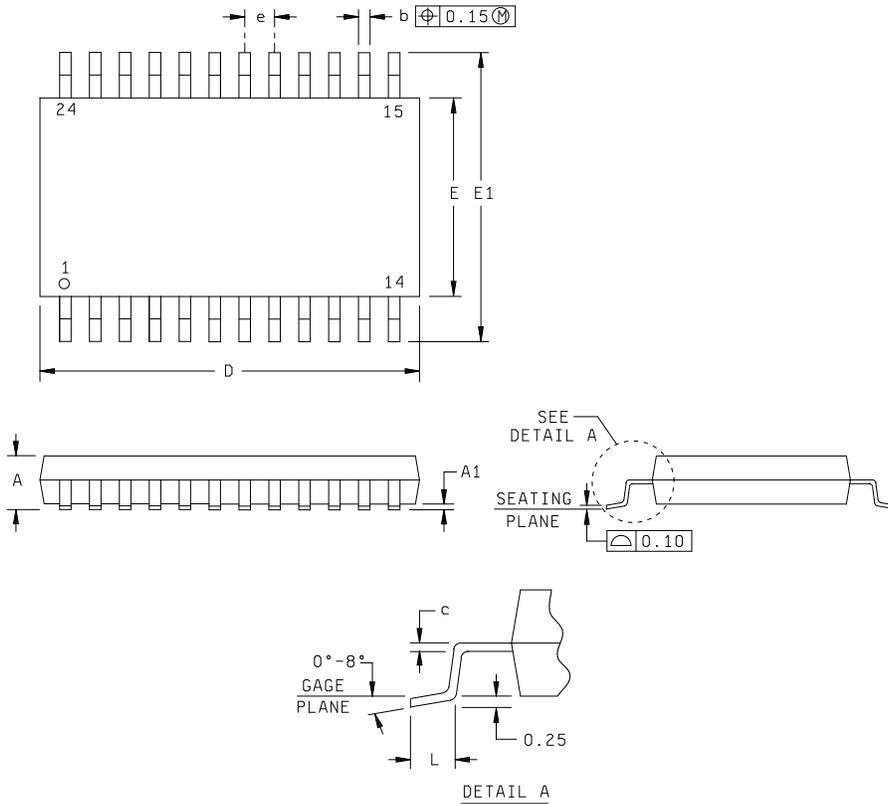
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Propagation delay time, output disable, OE to Y	t _{PHZ}	C _L = 50 pF See figure 5.	3.3 V	25°C	All	2.2	6.3	ns
			3 V to 3.6 V	-55°C to 125°C		1	11.1	
	t _{PLZ}		3.3 V	25°C		2.2	6.3	
			3 V to 3.6 V	-55°C to 125°C		1	11.5	
Output skew time, A to Y	t _{sk(o)}	C _L = 50 pF See figure 5.	3.3 V	25°C			0.5	ns
			3 V to 3.6 V	-55°C to 125°C			2.5	
Pulse skew time, A to Y	t _{sk(p)}	C _L = 50 pF See figure 5.	3.3 V	25°C			0.8	ns
			3 V to 3.6 V	-55°C to 125°C			3	
Process skew time, A to Y	t _{sk(pr)}	C _L = 50 pF See figure 5.	3.3 V	25°C		1	ns	
Rise time, A to Y	t _r	C _L = 50 pF See figure 5.	3 V to 3.6 V	-55°C to 125°C		2.5	ns	
Fall time, A to Y	t _f	C _L = 50 pF See figure 5.	3 V to 3.6 V	-55°C to 125°C		2.5	ns	
Average temperature coefficient of low-to-high propagation delay, A to Y	∞t _{PLH} (T) <u>3/ 4/</u>		3 V to 3.6 V	25°C, -55°C to 125°C		85	ps/ 10°C	
Average temperature coefficient of high-to-low propagation delay, A to Y	∞t _{PHL} (T) <u>3/ 4/</u>		3 V to 3.6 V	25°C, -55°C to 125°C		50	ps/ 10°C	
Average V _{CC} coefficient of low-to-high propagation delay, A to Y	∞t _{PLH} (V _{CC}) <u>3/ 5/</u>		3 V to 3.6 V	25°C, -55°C to 125°C		-145	ps/ 100 mV	
Average V _{CC} coefficient of high-to-low propagation delay, A to Y	∞t _{PHL} (V _{CC}) <u>3/ 5/</u>		3 V to 3.6 V	25°C, -55°C to 125°C		-100	ps/ 100 mV	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- 3/ This data was extracted from characterization material and has not been tested at the factory.
- 4/ ∞t_{PLH}(T) and ∞t_{PHL}(T) are virtually independent of V_{CC}.
- 5/ ∞t_{PLH}(V_{CC}) and ∞t_{PHL}(V_{CC}) are virtually independent of temperature.

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Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	2.00	---	.079	E	5.00	5.60	.197	.220
A1	0.05	---	.002	---	E1	7.40	8.20	.291	.323
b	0.22	0.38	.009	.015	e	0.65 BSC		.026 BSC	
c	0.09	0.25	.004	.010	L	0.55	0.95	.022	.037
D	7.90	8.50	.311	.335					

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-150.
3. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.
4. Body dimensions do not include mold flash or protrusion not to exceed 0.15 millimeters (0.006 inches).

FIGURE 1. Case outline.

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Inputs		Outputs Yn
A	\overline{OE}	
L	H	Z
H	H	Z
L	L	L
H	L	H

H = High voltage level
L = Low voltage level
Z = High impedance state

FIGURE 2. Function table.

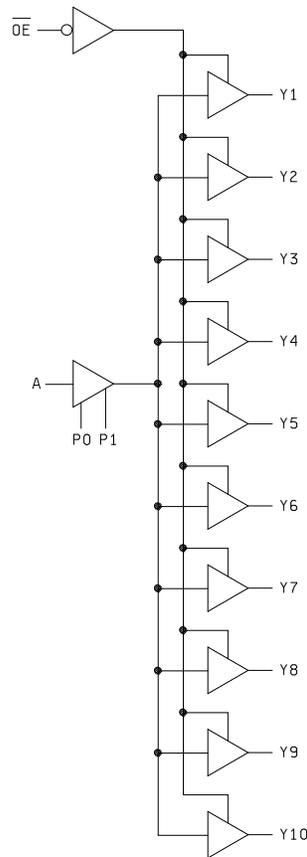


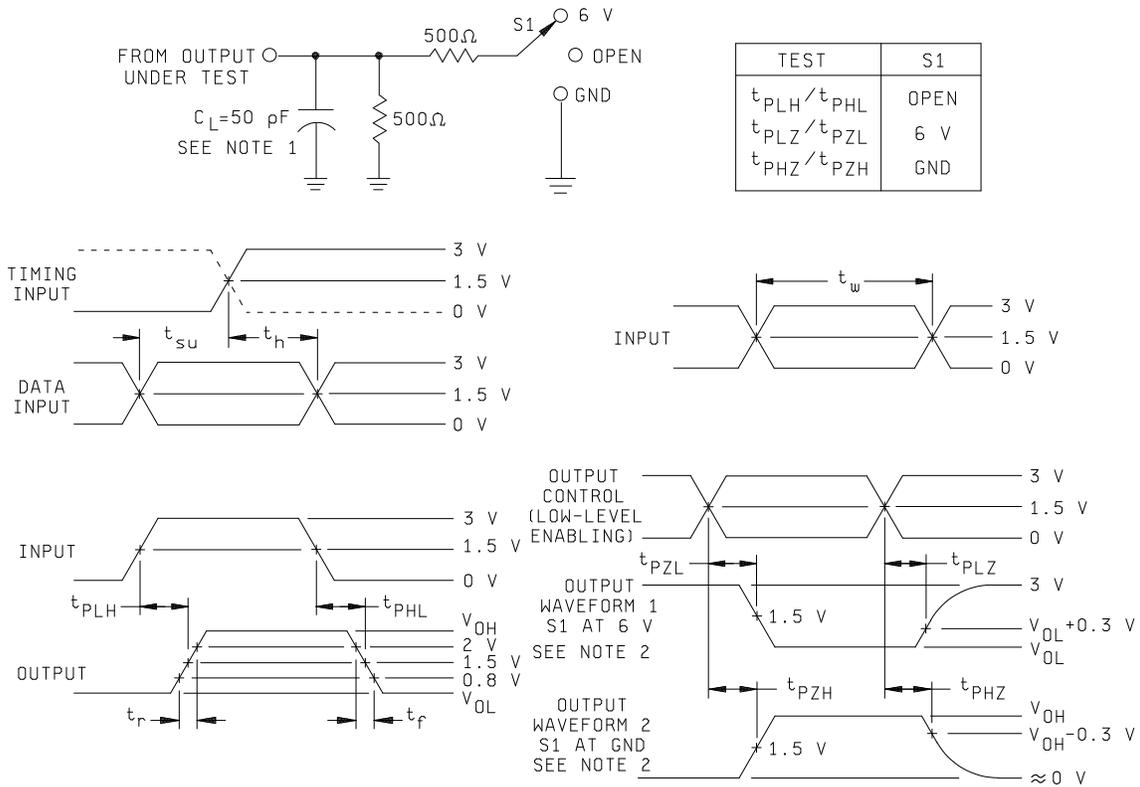
FIGURE 3. Logic diagram.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	GND
2	Y10
3	V _{CC}
4	Y9
5	\overline{OE}
6	A
7	P0
8	P1
9	Y8
10	V _{CC}
11	Y7
12	GND
13	GND
14	Y6
15	V _{CC}
16	Y5
17	GND
18	Y4
19	Y3
20	GND
21	Y2
22	V _{CC}
23	Y1
24	GND

FIGURE 4. Terminal connections.

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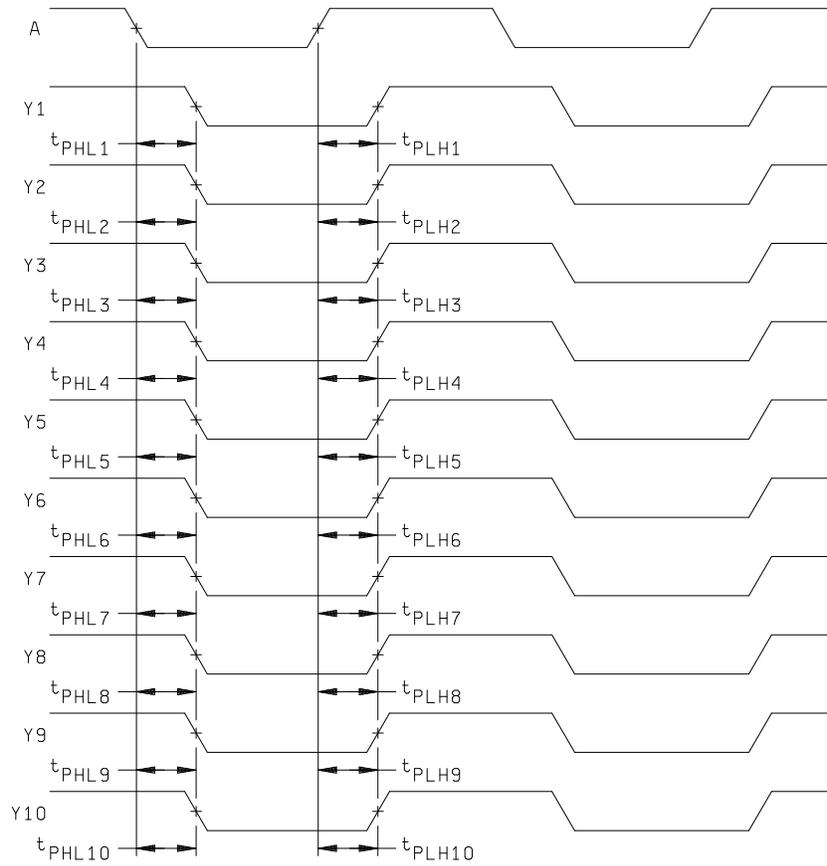


NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
4. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Timing waveforms and test circuit.

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NOTES:

- A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
 - The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$).
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$).
- B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$).
- C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
 - The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$) across multiple devices under identical operating conditions.
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$) across multiple devices under identical operating conditions.

FIGURE 5. Timing waveforms and test circuit - Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04757-01XE	01295	CDC2351MDBREP	CK2351MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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