| REVISIONS | | | |
|---|---|---|---|
| **LTR** | **DESCRIPTION** | **DATE** | **APPROVED** |
| A | Add device type 02. Update boilerplate to current revision. - CFS | 06-07-06 | Thomas M. Hess |
| B | Update boilerplate paragraphs to current requirements. - PHN | 13-09-12 | Thomas M. Hess |
| C | Under paragraph 1.3, add ESD ratings, and Thermal information. Replace Continuous total power dissipation and Package thermal impedance limits with a table. Add JEDEC references under section 2. Under paragraph 6.3, add Mode of transportation column. Update document paragraphs to current requirements. - ro | 20-03-11 | James R. Eschmeyer |

**CURRENT DESIGN ACTIVITY CAGE CODE 16236**
**HAS CHANGED NAMES TO:**
**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **REV** | | | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | | | | | | | | | | | | | | | | | | | | | | |
| **REV** | | | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | | | | | | | | | | | | | | | | | | | | | | |
| **REV STATUS OF PAGES** | **REV** | | | C | C | C | C | C | C | C | C | C | C | C | | | | | | | | |
| | **PAGE** | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | | | |

| | | |
|---|---|---|
| **PMIC N/A** | **PREPARED BY**<br>Charles F. Saffle | **DEFENSE SUPPLY CENTER COLUMBUS**<br>**COLUMBUS, OHIO 43218-3990** |
| Original date of drawing<br>YY-MM-DD<br>04-11-04 | **CHECKED BY**<br>Charles F. Saffle | **TITLE**<br>MICROCIRCUIT, LINEAR, PRECISION PROGRAMMABLE REFERENCE, MONOLITHIC SILICON |
| | **APPROVED BY**<br>Thomas M. Hess | |
| | **SIZE** **A** / **CODE IDENT. NO.** **16236** | **DWG NO.** **V62/04756** |
| | **REV** **C** | **PAGE** 1 **OF** 11 |

AMSC N/A

5962-V008-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance precision programmable reference microcircuit, with an operating temperature range of -40°C to +125°C for device 01, and -55°C to +125°C for device 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/04756 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | TL1431-EP | Precision programmable reference |
| 02 | TL1431-EP | Precision programmable reference |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 8 | MS-012-AA | Plastic small-outline |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy (BGA/CGA) |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Cathode voltage ($V_{KA}$) ..... 37 V 2/
Continuous cathode current range ($I_{KA}$) ..... -100 mA to 150 mA
Reference input current range ($I_{(ref)}$) ..... -50 μA to 10 mA
Operating virtual junction temperature ($T_J$) ..... 150°C
Soldering lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C
Thermal resistance, junction to ambient ($\theta_{JA(high)}$) (high K board) ..... 97°C/W
Thermal resistance, junction to ambient ($\theta_{JA(low)}$) (low K board) ..... 165°C/W
Electrostatic discharge (ESD) rating:
Human body model (HDM), per JEDEC JS-001, all pins ..... ±4000 V 3/
Charge device model (CDM), per JEDEC JESD22-C101 ..... ±2000 V 4/

1.4 Recommended operating conditions. 5/

Cathode voltage range ($V_{KA}$) ..... $V_{I(ref)}$ to 36 V
Cathode current range ($I_{KA}$) ..... 1 mA to 100 mA
Operating free-air temperature range ($T_A$):
Device 01 ..... -40°C to +125°C
Device 02 ..... -55°C to +125°C

1.5 Dissipation ratings.

| Package | Power rating $T_A < 25°C$ | Package thermal impedance | Derating factor above $T_A = 25°C$ | Power rating $T_A = 70°C$ | Power rating $T_A = 85°C$ | Power rating $T_A = 125°C$ |
|---|---|---|---|---|---|---|
| Case X | 1102 mW | 97°C/W (high K board) | 10 mW/°C | 824 mW | 670 mW | 257 mW |
| | | 165°C/W (low K board) | 6 mW/°C | 484 mW | 393 mW | 151 mW |

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values are with respect to Anode, unless otherwise noted.

3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

| | | |
|---|---|---|
| JEDEC JS-001 | – | Human Body Model Testing of Integrated Circuits |
| JESD22-C101 | – | Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components |
| JEDEC PUB 95 | – | Registered and Standard Outlines for Semiconductor Devices |
| JEDEC JEP 155 | – | Recommended ESD Target Levels for HBM/MM Qualification |
| JEDEC JEP 157 | – | Recommended ESD-CDM Target Levels |

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Functional block diagram. The functional block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Test circuits. The test circuits shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions | Temperature, $T_A$ 2/ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Reference input voltage | $V_{I(ref)}$ | $V_{KA} = V_{I(ref)}$, see figure 4, test circuit 1 | 25°C | 01, 02 | 2490 | 2510 | mV |
| | | | Full range | | 2470 | 2530 | |
| Deviation of reference input voltage over full temperature range | $V_{I(dev)}$ 3/ | $V_{KA} = V_{I(ref)}$, see figure 4, test circuit 1 | Full range | 01, 02 | 17 typical | | mV |
| Ratio of change in reference input voltage to the change in cathode voltage | $\Delta V_{I(ref)} / \Delta V_{KA}$ | $\Delta V_{KA}$ = 3 V to 36 V, see figure 4, test circuit 2 | Full range | 01, 02 | | -2 | mV/V |
| Reference input current | $I_{I(ref)}$ | R1 = 10 kΩ, R2 = ∞, see figure 4, test circuit 2 | 25°C | 01, 02 | | 2.5 | μA |
| | | | Full range | | | 4 | |
| Deviation of reference input current over full temperature range | $I_{I(dev)}$ 3/ | R1 = 10 kΩ, R2 = ∞, see figure 4, test circuit 2 | Full range | 01, 02 | 0.5 typical | | μA |
| Minimum cathode current for regulation | $I_{min}$ | $V_{KA} = V_{I(ref)}$, see figure 4, test circuit 1 | 25°C | 01, 02 | | 1 | mA |
| Off-state cathode current | $I_{off}$ | $V_{KA}$ = 36 V, $V_{I(ref)}$ = 0 V, see figure 4, test circuit 3 | 25°C | 01, 02 | | 0.5 | μA |
| | | | Full range | | | 2 | |
| Output impedance | $\lvert z_{KA} \rvert$ 4/ | $V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, $I_{KA}$ = 1 mA to 100 mA, see figure 4, test circuit 1 | 25°C | 01, 02 | | 0.4 | Ω |

See notes on next sheet.

TABLE I. Electrical performance characteristics. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

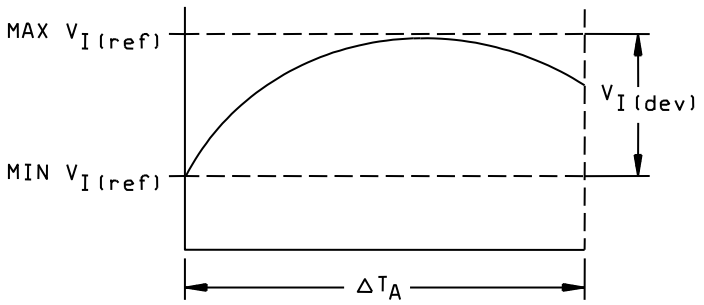
2/ Full range is -40°C to +125°C for device 01, and -55°C to +125°C for device 02.

3/ The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{V_{I(ref)}}$ is defined as:

$$|\alpha_{V_{I(ref)}}|(\text{ ppm/°C }) = \frac{(\ V_{I(dev)}/V_{I(ref)} \text{ at } 25°C\ ) \times 10^6}{\Delta T_A}$$

where: $\Delta T_A$ is the rated operating temperature range of the device.

$\alpha_{V_{I(ref)}}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

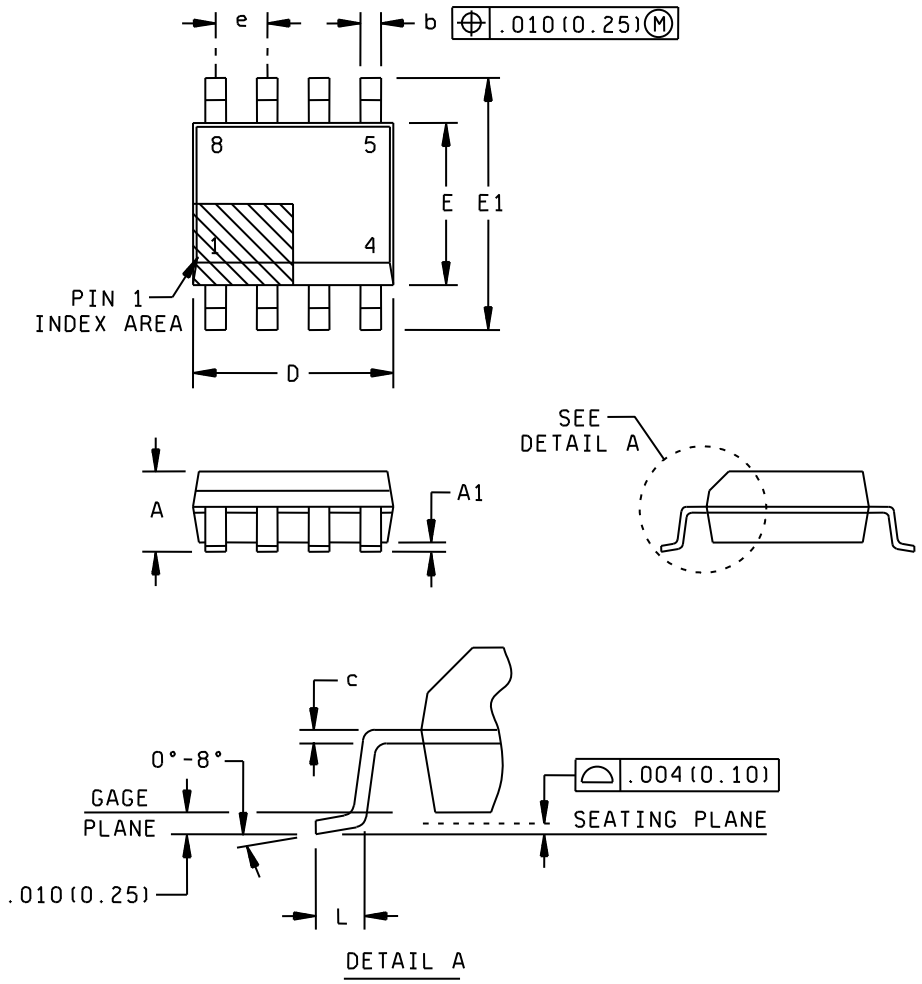



4/ The output impedance is defined as: $|z_{KA}| = \Delta V_{KA}/\Delta I_{KA}$.

When the device is operating with two external resistors (see test circuit 2 of figure 4), the total dynamic impedance of the circuit is given by:

$|z'| = \Delta V/\Delta I$, which is approximately equal to $|z_{KA}|( 1 + R1/R2 )$.

Case X




NOTES:
1. All linear dimensions are shown in inches (millimeters). Millimeters equivalents are given for general information only.
2. This drawing is subject to change without notice.
3. Dimension D does not include mold flash, protrusion, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch (0.15 millimeters) per side.
4. Dimension E does not include interlead flash.
5. Falls within JEDEC MS-012-AA.

FIGURE 1. Case outline.

Case X

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | --- | .069 | --- | 1.75 |
| A1 | .004 | .010 | 0.10 | 0.25 |
| b | .012 | .020 | 0.31 | 0.51 |
| c | .005 | .010 | 0.13 | 0.25 |
| D | .189 | .197 | 4.80 | 5.00 |
| E | .150 | .157 | 3.80 | 4.00 |
| E1 | .228 | .244 | 5.80 | 6.20 |
| e | .050 TYP | | 1.27 TYP | |
| L | .016 | .050 | 0.40 | 1.27 |

FIGURE 1. Case outline - Continued.

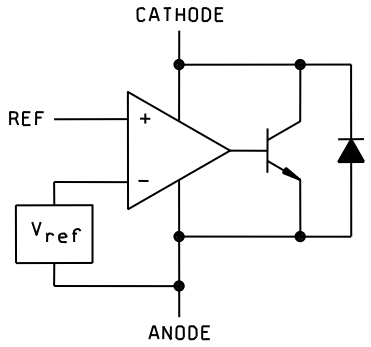



FIGURE 2. Functional block diagram.

| Device types | 01, 02 |
|---|---|
| Case outline | X |
| Terminal number | Terminal symbol |
| 1 | CATHODE |
| 2 | ANODE |
| 3 | ANODE |
| 4 | NC |
| 5 | NC |
| 6 | ANODE |
| 7 | ANODE |
| 8 | REF |

NC = No internal connection.
ANODE terminals are connected internally.

FIGURE 3. Terminal connections.

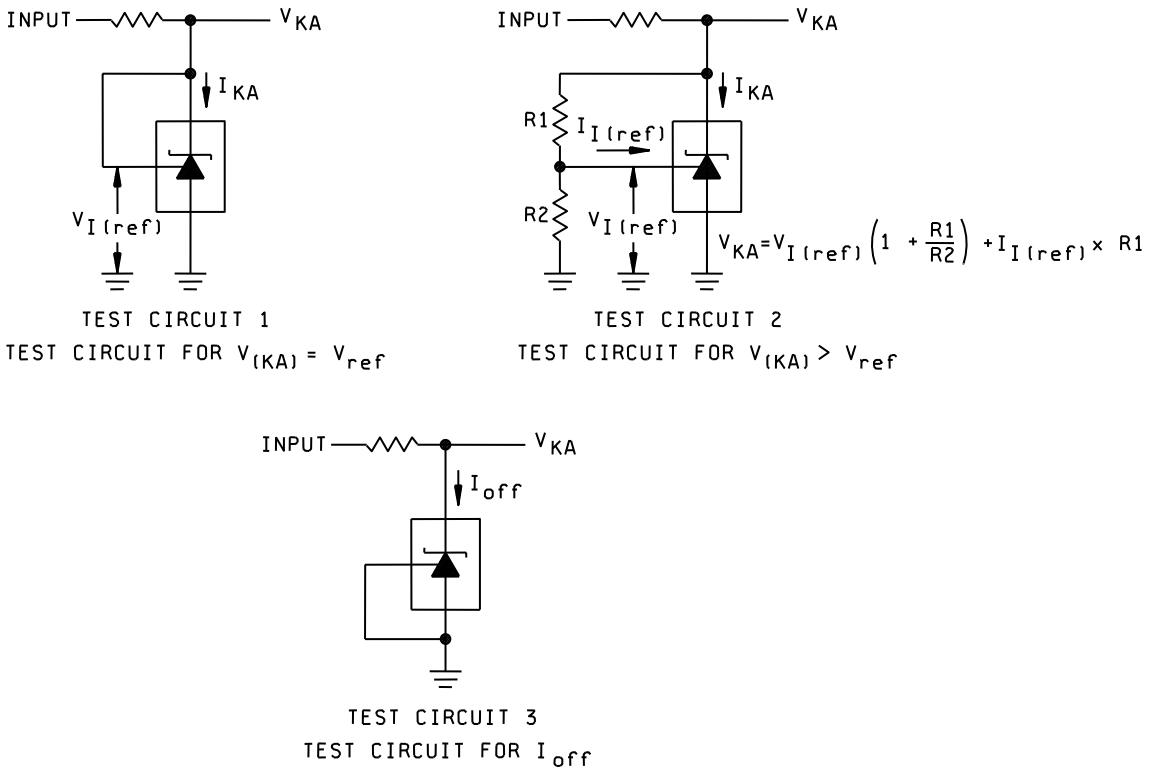



FIGURE 4. Test circuits.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Mode of transportation | Top side marking | Vendor part number |
|---|---|---|---|---|
| V62/04756-01XE | 01295 | Tape and reel | 1431QE | TL1431QDREP |
| V62/04756-02XE | 01295 | Tape and reel | 1431ME | TL1431MDREP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest lane<br>P.O. Box 660199<br>Dallas, TX 75243 |