REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct lead finish for device 03. Update boilerplate. - CFS	05-12-02	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	13-09-12	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV	B	B	B	B	B	B	B	B	B	B	B	B	B									
PAGE	40	41	42	43	44	45	46	47	48	49	50	51	52									
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
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REV STATUS OF PAGES																		
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 05-01-11	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, FLOATING POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/04754**
	REV B	**PAGE** 1 **OF** 52

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Floating-Point Digital Signal Processor microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04754	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device type	Generic	Circuit function
01	SM320C6712-EP	Floating Point Digital Signal Processor
02	SM320C6712C-EP	Floating Point Digital Signal Processor
03	SM320C6712D-EP	Floating Point Digital Signal Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	256	JEDEC MO-151	Plastic ball grid array
Y	272	JEDEC MO-151	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

1.3 Absolute maximum ratings. 2/

Supply voltage ranges, (CV_{DD}): 3/
Device type 02 and 03 only ..... -0.3 V to +1.8 V
Device type 01..... -0.3 V to +2.3 V
Supply voltage ranges, (DV_{DD}) ..... -0.3 V to +4.0 V 3/
Input voltage ranges: (V_I):
Device type 02 and 03 only ..... -0.3 V to DV_{DD} + 0.5 V
Device type 01 ..... -0.3 V to +4.0 V
Output voltage ranges: (V_O)
Device type 02 and 03 only ..... -0.3 V to DV_{DD} + 0.5 V
Device type 01 ..... -0.3 V to +4.0 V
Operating case temperature ranges, (T_C) ..... -40°C to +105°C
Storage temperature range, (T_{STG})..... -65°C to +150°C

1.4 Recommended operating conditions.

			Min	Max	Unit
Supply voltage, Core (CV_{DD}) 4/	Device type 02 and 03 only		1.14 5/	1.32	V
	Device type 01		1.71	1.89	
Supply voltage, I/O (DV_{DD}) 4/	Device type 02 and 03 only		3.13	3.47	V
	Device type 01		3.14	3.46	
Supply ground, (V_{SS})			0	0	V
High level input voltage, (V_{IH})	Device type 02 and 03 only	All signals except CLKS1, DR1, $\overline{RESET}$	2		V
		CLKS1, DR1, $\overline{RESET}$	2		
	Device type 01 and 02		2		
Low level input voltage, (V_{IL})	Device type 02 and 03 only	All signals except CLKS1, DR1, $\overline{RESET}$		0.8	V
		CLKS1, DR1, $\overline{RESET}$		0.3*DV_{DD}	
	Device type 01			0.8	

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3/ All voltage values are with respect to V_{SS}.
4/ For device type 01, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O supply. For device type 02 and 03, the core supply should be powered up prior to (and powered down after), the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.
5/ These values are compatible with existing 1.26 V designs.

1.4 Recommended operating conditions - Continued.

			Min	Max	Unit
High level output current, (I_{OH})	Device type 01	All signals except CLKOUT1, CLKOUT2, and ECLKOUT		-4	mA
		CLKOUT1, CLKOUT2, and ECLKOUT		-8	
	Device type 02 6/	All signals except ECKLOUT, CLKOUT2, CLKOUT3, CLKS1, and DR1		-8	mA
		ECKLOUT, CLKOUT2, CLKOUT3		-16	
	Device type 03 5/	All signals except ECKLOUT, CLKOUT2, CLKS1, and DR1		-8	mA
		ECKLOUT and CLKOUT2		-16	
Low level output current, (I_{OL})	Device type 01	All signals except CLKOUT1, CLKOUT2, and ECLKOUT		4	mA
		CLKOUT1, CLKOUT2, and ECLKOUT		8	
	Device type 02 5/	All signals except ECLKOUT, CLKOUT2, CLKOUT3, CLKS1, and DR1		8	mA
		ECKLOUT, CLKOUT2, CLKOUT3		16	
		CLKS1 and DR1		3	
	Device type 03 5/	All signals except ECKLOUT, CLKOUT2, CLKS1, and DR1		8	mA
		ECKLOUT and CLKOUT2		16	
		CLKS1 and DR1		3	
Operating case temperature, (T_C)			-40	105	°C

Thermal resistance characteristics for case X (device type 01 only)

	Air Flow (m/s) 7/	°C/W
Junction to case, ($R_{\theta JC}$)	N/A	6.4
Junction to free air, ($R_{\theta JA}$)	0.0	25.5
Junction to free air, ($R_{\theta JA}$)	0.5	23.1
Junction to free air, ($R_{\theta JA}$)	1.0	22.3
Junction to free air, ($R_{\theta JA}$)	2.0	21.2

6/ Refers to DC (or steady state) currents only, actual switching currents are higher. For more details, see manufacturer data device specific IBIS models.

7/ m/s = meters per second.

1.4 Recommended operating conditions - Continued.

Thermal resistance characteristics for case Y (device type 02 and 03 only)

	Air Flow (m/s) 7/	°C/W
Junction to case, ($R_{\theta JC}$)	N/A	9.7
Junction to package top (P_{siJT})	0.0	1.5
Junction to board, ($R_{\theta JB}$)	N/A	19
Junction to free air, ($R_{\theta JA}$)	0.0	22
Junction to free air, ($R_{\theta JA}$)	0.5	21
Junction to free air, ($R_{\theta JA}$)	1.0	20
Junction to free air, ($R_{\theta JA}$)	2.0	19
Junction to free air, ($R_{\theta JA}$)	4.0	18
Junction to board, (Psi_{JB})	0.0	16

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 Test load circuits. The test load circuits shall be as specified in figure 4.

3.5.5 Board level input/output timings. The board level input/output timings shall be as specified in figure 5.

3.5.6 Timing waveforms. The timing waveforms shall be as shown in figure 6-40.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test condition 2/		Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	All signals	DV_{DD} = min, I_{OH} = max	01	2.4		V
		All signals except CLKS1 and DR1		02, 03	2.4		
Low level output voltage	V_{OL}	All signals	DV_{DD} = min, I_{OL} = max	01		0.4	V
		All signals except CLKS1 and DR1		02, 03		0.4	
		CLKS1 and DR1		02, 03		0.4	
Input current	I_I	All signals	$V_I = V_{SS}$ to DV_{DD}	01		±150	µA
		All signals except CLKS1 and DR1		02, 03		±170	
		CLKS1 and DR1		02, 03		±10	
Off state output current	I_{OZ}	All signals	$V_O = DV_{DD}$ or 0 V	01		±10	µA
		All signals except CLKS1 and DR1		02, 03		±170	
		CLKS1 and DR1		02, 03		±10	
Supply current, CPU + CPU memory access 3/	I_{DD2V}	CV_{DD} = NOM, CPU clock = 100 MHz		01	336 Typ		mA
Supply current, peripherals 3/	I_{DD2V}			01	180 Typ		
Core supply current	I_{DD2V}	CV_{DD} = 1.26 V, CPU clock = 150 MHz		02	430 Typ		mA
		CV_{DD} = 1.26 V, CPU clock = 167 MHz		03	475 Typ		
Supply current, I/O pins 3/	I_{DD3V}	DV_{DD} = NOM, CPU clock = 100 MHz		01	50 Typ		mA
I/O supply current	I_{DD3V}	DV_{DD} = 3.3 V, EMIF speed = 100 MHz		02, 03	75 Typ		mA
Input capacitance	C_i			All		7	pF
Output capacitance	C_o			All		7	pF

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
	INPUT AND OUTPUT CLOCKS							
	Timing requirements for CLKIN 4/ 5/ [device type 01]			-100				
				CLKMODE = x4		CLKMODE = x1		
1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	40		10		ns
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.45C		
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.45C		
4	Transaction time, CLKIN	$t_{t(CLKIN)}$			5		1	
	Timing requirements for CLKIN 4/ 5/ 6/ [device type 02 and 03]			-167				
				PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		
1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	6	83.3	6		ns
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.4C		
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.4C		
4	Transaction time, CLKIN	$t_{t(CLKIN)}$			5		5	
	Switching characteristics for CLKOUT1 7/ 8/ 9/ [device type 01 only]			-100				
				CLKMODE = x4		CLKMODE = x4		
1	Cycle time, CLKOUT1	$t_{c(CKO1)}$	See figure 7	P-0.7	P+0.7	P-0.7	P+0.7	ns
2	Pulse duration, CLKOUT1 high	$t_{w(CKO1H)}$		(P/2)-0.7	(P/2)+0.7	PH-0.7	PH+0.7	
3	Pulse duration, CLKOUT1 low	$t_{w(CKO1L)}$		(P/2)-0.7	(P/2)+0.7	PH-0.7	PH+0.7	
4	Transition time, CLKOUT1	$t_{t(CKO1)}$			0.6		0.6	
	Switching characteristics for CLKOUT2 7/ 9/ [device type 01]			-100				
1	Cycle time, CLKOUT2	$t_{c(CKO2)}$	See figure 8	2P-0.7		2P+0.7		ns
2	Pulse duration, CLKOUT2 high	$t_{w(CKO2H)}$		P-0.7		P+0.7		
3	Pulse duration, CLKOUT2 low	$t_{w(CKO2L)}$		P-0.7		P+0.7		
4	Transition time, CLKOUT2	$t_{t(CKO2)}$				0.6		
	Switching characteristics for CLKOUT2 7/ 10/ [device type 02 and 03]			-167				
1	Cycle time, CLKOUT2	$t_{c(CKO2)}$	See figure 8	C2-0.8		C2+0.8		ns
2	Pulse duration, CLKOUT2 high	$t_{w(CKO2H)}$		(C2/2)-0.8		(C2/2)+0.8		
3	Pulse duration, CLKOUT2 low	$t_{w(CKO2L)}$		(C2/2)-0.8		(C2/2)+0.8		
4	Transition time, CLKOUT2	$t_{t(CKO2)}$				2		

See notes at end of table.

TABLE I. Electrical performance characteristics – Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
INPUT AND OUTPUT CLOCKS (Continued)								
Switching characteristics for CLKOUT3 7/ 11/ [device type 02 and 03]				Device type 02-167		Device type 03-167		
1	Cycle time, CLKOUT3	$t_{c(CKO3)}$	See figure 9	C3-0.6	C3+0.6	C3-0.9	C3+0.9	ns
2	Pulse duration, CLKOUT3 high	$t_{w(CKO3H)}$		(C3/2)-0.6	(C3/2)+0.6	(C3/2)-0.9	(C3/2)+0.9	
3	Pulse duration, CLKOUT3 low	$t_{w(CKO3L)}$		(C3/2)-0.6	(C3/2)+0.6	(C3/2)-0.9	(C3/2)+0.9	
4	Transition time, CLKOUT3	$t_{t(CKO3)}$			2		3	
5	Delay time, CLKIN high to CLKOUT3 valid	$t_{d(CKINH-CKO3V)}$		1.5	6.5	1.5	7.5	
Timing requirements for ECLKIN 4/				-100		-167		ns
1	Cycle time, ECLKIN	$t_{c(EKI)}$	See figure 10	15		10		
2	Pulse duration, ECLKIN high	$t_{w(ECKIH)}$		6.8		4.5		
3	Pulse duration, ECLKIN low	$t_{w(ECKIL)}$		6.8		4.5		
4	Transaction time, ECLKIN	$t_{t(EKI)}$			3		3	
Switching characteristics for ECLKOUT 7/ 12/ 13/				-100		-167		
1	Cycle time, CLKOUT	$t_{c(EKO)}$	See figure 11	E-0.7	E+0.7	E-0.9	E+0.9	ns
2	Pulse duration, ECLKOUT high	$t_{w(ECKOH)}$		EH-0.7	EH+0.7	EH-09	EH+0.9	
3	Pulse duration, ECLKOUT low	$t_{w(ECKOL)}$		EL-0.7	EL+0.7	EL-09	EL+0.9	
4	Transition time, ECLKOUT	$t_{t(EKO)}$			0.6		2	
5	Delay time, ECLKIN high to ECLKOUT high	$t_{d(EKIH-EKOH)}$		1	7	1	6.5	
6	Delay time, ECLKIN low to ECLKOUT low	$t_{d(EKIL-EKOL)}$		1	7	1	6.5	

See notes at end of table.

TABLE I. Electrical performance characteristics – Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
	ASYNCHRONOUS MEMORY TIMING							
Timing requirements for asynchronous memory cycles 14/ 15/				-100		-167		
3	Setup time, EDx valid before $\overline{ARE}$ high	$t_{su(EDV-AREH)}$	See figure 12	13		6.5		ns
4	Hold time, EDx valid after $\overline{ARE}$ high	$t_{h(AREH-EDV)}$		1		1		
6	Setup time, ARDY valid before ECLKOUT high	$t_{su(ARDY-EKOH)}$		6		3		
7	Hold time, ARDY valid after ECLKOUT high	$t_{h(EKOH-ARDY)}$		1.7		2.3		
Switching characteristics for asynchronous memory cycles 15/ 16/ 17/				-100		-167		
1	Output setup time, select signals valid to $\overline{ARE}$ low	$t_{osu(SELV-AREL)}$	See figure 12	RS*E-3		RS*E-1.7		ns
2	Output hold time, $\overline{ARE}$ high to select signals invalid	$t_{oh(AREH-SELIV)}$		RH*E-3		RH*E-1.7		
5	Delay time, ECKLOUT high to $\overline{ARE}$ valid	$t_{d(EKOH-AREV)}$		1.5	11	1.5	7	
8	Output setup time, select signals valid to $\overline{AWE}$ low	$t_{osu(SELV-AWEL)}$		WS*E-3		WS*E-1.7		
9	Output hold time, $\overline{AWE}$ high to select signals and EDx invalid	$t_{oh(AWEH-SELIV)}$		WH*E-3		WH*E-1.7		
10	Delay time, ECLKOUT high to $\overline{AWE}$ valid	$t_{d(EKOH-AWEV)}$		1.5	11	1.5	7	
11	Output setup time, ED valid to $\overline{AWE}$ low	$t_{osu(EDV-AWEL)}$		(WS-1)*E-1.7		(WS-1)*E-1.7		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
SYNCHRONOUS BURST MEMORY TIMING								
Timing requirements for synchronous burst SRAM cycles 18/				-100		-167		
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 13	6		1.5		ns
7	Hold time, read EDx valid after ECLKOUT high	$t_{h(EKOH-EDV)}$		2.1 19/		2.5		
Switching characteristics for synchronous burst SRAM cycles 18/ 19/				-100		-167		
1	Delay time, ECKLOUT high to $\overline{CEx}$ valid	$t_{d(EKOH-CEV)}$	See figure 13	1.5	11 19/	1.2	7	ns
2	Delay time, ECKLOUT high to $\overline{BEx}$ valid	$t_{d(EKOH-BEV)}$			11 19/		7	
3	Delay time, ECKLOUT high to $\overline{BEx}$ invalid	$t_{d(EKOH-BEIV)}$		1.5		1.2		
4	Delay time, ECKLOUT high to EAx valid	$t_{d(EKOH-EAV)}$			11 19/		7	
5	Delay time, ECKLOUT high to EAx invalid	$t_{d(EKOH-EAIV)}$		1.5		1.2		
8	Delay time, ECKLOUT high to $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$ valid	$t_{d(EKOH-ADSV)}$		1.5	11 19/	1.2	7	
9	Delay time, ECKLOUT high to $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$ valid	$t_{d(EKOH-OEV)}$		1.5	11 19/	1.2	7	
10	Delay time, ECKLOUT high to $\overline{EDx}$ valid	$t_{d(EKOH-EDV)}$			11 19/		7	
11	Delay time, ECKLOUT high to $\overline{EDx}$ invalid	$t_{d(EKOH-EDIV)}$		1.5		1.2		
12	Delay time, ECKLOUT high to $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$ valid	$t_{d(EKOH-WEV)}$		1.5	11 19/	1.2	7	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
	SYNCHRONOUS DRAM TIMING							
Timing requirements for synchronous DRAM cycles 21/				-100		-167		
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 14	6		1.5		ns
7	Hold time, read EDx valid after ECLKOUT high	$t_{h(EKOH-EDV)}$		2.1		2.5		
Switching characteristics for synchronous DRAM cycles 21/ 22/				-100		-167		
1	Delay time, ECKLOUT high to $\overline{CEx}$ valid	$t_{d(EKOH-CEV)}$	See figure 15-17	1.5	11	1.5	7	ns
2	Delay time, ECKLOUT high to $\overline{BEx}$ valid	$t_{d(EKOH-BEV)}$			11		7	
3	Delay time, ECKLOUT high to $\overline{BEx}$ invalid	$t_{d(EKOH-BEIV)}$		1.5		1.5		
4	Delay time, ECKLOUT high to EAx valid	$t_{d(EKOH-EAV)}$			11		7	
5	Delay time, ECKLOUT high to EAx invalid	$t_{d(EKOH-EAIV)}$		1.5		1.5		
8	Delay time, ECKLOUT high to $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$ valid	$t_{d(EKOH-CASV)}$		1.5	11	1.5	7	
9	Delay time, ECKLOUT high to $\overline{EDx}$ valid	$t_{d(EKOH-EDV)}$			11		7	
10	Delay time, ECKLOUT high to $\overline{EDx}$ invalid	$t_{d(EKOH-EDIV)}$		1.5		1.5		
11	Delay time, ECKLOUT high to $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$ valid	$t_{d(EKOH-WEV)}$		1.5	11	1.5	7	
12	Delay time, ECKLOUT high to $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$ valid	$t_{d(EKOH-RAS)}$		1.5	11	1.5	7	
	$\overline{HOLD}$ / $\overline{HOLDA}$ TIMING							
Timing requirements for the $\overline{HOLD}$ / $\overline{HOLDA}$ cycles 12/						-100, -167		
3	Hold time $\overline{HOLD}$ low after $\overline{HOLDA}$ low	$t_{h(HOLDAL-HOLDL)}$	See figure 18			E		ns
Switching characteristics for the $\overline{HOLD}$ / $\overline{HOLDA}$ cycles 12/ 23/				-100, -167		Device type 03 -167		
1	Delay time, $\overline{HOLD}$ low to EMIF bus high impedance	$t_{d(HOLDL-EMHZ)}$	See figure 18	2E	24/	2E	24/	ns
2	Delay time, EMIF bus high impedance to $\overline{HOLDA}$ low	$t_{d(EMHZ-HOLDAL)}$		-0.1	2E	0	2E	
4	Delay time, $\overline{HOLD}$ high to EMIF bus low impedance	$t_{d(HOLDH-EMLZ)}$		2E	7E	2E	7E	
5	Delay time, EMIF bus low impedance to $\overline{HOLDA}$ high	$t_{d(EMLZ-HOLDAH)}$		-1.5	2E	0	2E	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits				Unit
				Min	Max	Min	Max	
BUSREQ TIMING								
				-100		-167		
1	Delay time, ECKLOUT high to BUSREQ valid	$t_{d(EKOH-BUSRV)}$	See figure 19	2	10	1.5	7.2	ns
RESET TIMING [device type 01]								
Timing requirements for reset 25/						-100		
1	Width of the $\overline{RESET}$ pulse (PLL stable) 26/	$t_{w(RST)}$	See figure 20			10P		ns
	Width of the $\overline{RESET}$ pulse (PLL needs to sync up) 27/					250		
14	Setup time, BOOTMODE[1:0] configuration bits valid before $\overline{RESET}$ high	$t_{su(BOOT)}$				2P		
15	Hold time, BOOTMODE[1:0] configuration bits valid after $\overline{RESET}$ high	$t_{su(BOOT)}$				2P		
Switching characteristics during reset 12/ 25/ 28/						-100		
2	Delay time, $\overline{RESET}$ low to ECLKIN synchronized internally	$t_{d(RSTL-ECKL)}$	See figure 20			2P+3E	3P+4E	ns
3	Delay time, $\overline{RESET}$ high to ECLKIN synchronized internally	$t_{d(RSTH-ECKI)}$				2P+3E	3P+4E	
4	Delay time, $\overline{RESET}$ low to EMIF Z group high impedance	$t_{d(RSTL-ENIFZHZ)}$				2P+3E		
5	Delay time, $\overline{RESET}$ high to EMIF Z group valid	$t_{d(RSTH-EMIFZV)}$					3P+4E	
6	Delay time, $\overline{RESET}$ low to EMIF high group invalid	$t_{d(RSTL-EMIFHIV)}$				2P+3E		
7	Delay time, $\overline{RESET}$ high to EMIF high group valid	$t_{d(RSTH-EMIFHV)}$					3P+4E	
8	Delay time, $\overline{RESET}$ low to EMIF low group invalid	$t_{d(RSTL-EMIFLIV)}$				2P+3E		
9	Delay time, $\overline{RESET}$ high to EMIF low group valid	$t_{d(RSTH-EMIFLV)}$					3P+4E	
12	Delay time, $\overline{RESET}$ low to Z group high impedance	$t_{d(RSTL-ZHZ)}$				2P		
13	Delay time, $\overline{RESET}$ high to Z group valid	$t_{d(RSTH-ZV)}$				2P		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits				Unit
				Min	Max	Min	Max	
RESET TIMING [device type 02 and 03]								
Timing requirements for reset 25/ 26/						-167, -		
1	Pulse duration, $\overline{\text{RESET}}$	$t_{w(RST)}$	See figure 24			100		ns
13	Setup time, boot configuration bits valid before $\overline{\text{RESET}}$ high 27/	$t_{su(BOOT)}$				2P		
14	Hold time, boot configuration bits valid after $\overline{\text{RESET}}$ high 27/	$t_{su(BOOT)}$				2P		
Switching characteristics during reset 29/						-167, -		
2	Delay time, external $\overline{\text{RESET}}$ high to internal reset high and all signal group valid 28/ 30/ — CLKMODE0 = 1	$t_{d(RSTH-ZV)}$	See figure 24				31/	ns
3a	Delay time, $\overline{\text{RESET}}$ low to ECLKOUT low (device 02)	$t_{d(RSTL-ECKOL)}$				0		
3b	Delay time, $\overline{\text{RESET}}$ low to ECLKOUT high impedance (device 03)	$t_{d(RSTL-ECKOL)}$				0		
4	Delay time, $\overline{\text{RESET}}$ high to ECLKOUT valid	$t_{d(RSTH-ECKOV)}$					6P	
5a	Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 invalid (device 02)	$t_{d(RSTL-CKO2IV)}$				0		
5b	Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 high impedance (device 03)	$t_{d(RSTL-CKO2IV)}$				0		
6	Delay time, $\overline{\text{RESET}}$ high to CLKOUT2 valid	$t_{d(RSTH-CKO2V)}$					6P	
7	Delay time, $\overline{\text{RESET}}$ low to CLKOUT3 low	$t_{d(RSTL-CKO3L)}$				0		
8	Delay time, $\overline{\text{RESET}}$ high to CLKOUT3 valid	$t_{d(RSTH-CKO3V)}$					6P	
9	Delay time, $\overline{\text{RESET}}$ low to EMIF Z group high impedance 28/	$t_{d(RSTL-EMIFZHZ)}$				0		
10	Delay time, $\overline{\text{RESET}}$ low to EMIF low group (BURSEQ) invalid 28/	$t_{d(RSTL-EMIFLIV)}$				0		
11	Delay time, $\overline{\text{RESET}}$ low to Z group 1 high impedance 28/	$t_{d(RSTL-Z1HV)}$				0		
EXTERNAL INTERRUPT TIMING								
Timing requirements for external interrupts 25/				-100		-167		
1	Width of the NMI interrupt pulse low	$t_{w(ILOW)}$	See figure 22	2P		2P		ns
	Width of the EXT_INT interrupt pulse low			2P		4P		
2	Width of the NMI interrupt pulse high	$t_{w(IHIGH)}$		2P		2P		
	Width of the EXT_INT interrupt pulse high			2P		4P		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING								
Timing requirements for McBSP 25/ 32/		**[Device type 01]**				-100		
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 23	CLKR/X ext		2P 33/		ns
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext		34/		
5	Setup, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int		20		
				CLKR ext		1		
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int		6		
				CLKR ext		3		
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int		22		
				CLKR ext		3		
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR int		3		
				CLKR ext		4		
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKX int		23		
				CLKX ext		1		
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-RXH)}$		CLKX int		6		
				CLKX ext		3		
Timing requirements for McBSP 25/ 32/		**[Device type 02 and 03]**				-167		
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 23	CLKR/X ext		2P 35/		ns
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext		34/ 36/		
5	Setup, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int		9		
				CLKR ext		1		
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int		6		
				CLKR ext		3		
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int		8		
				CLKR ext		0		
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR int		3		
				CLKR ext		4		
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKX int		9		
				CLKX ext		1		
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-RXH)}$		CLKX int		6		
				CLKX ext		3		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/		Limits Min	Limits Max	Limits Min	Limits Max	Unit
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued									
Switching characteristics for McBSP 32/ 37/			**[Device type 01]**				-100		
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	$t_{d(CKSH-CKRSH)}$	See figure 23				4	26	ns
2	Cycle time, CLKR/X 25/ 33/	$t_{c(CKRX)}$		CLKR/X int			2P		
3	Pulse duration, CLKR/X high or CLKR/X low 38/	$t_{w(CKRX)}$		CLKR/X int			C-1	C+1	
4	Delay time, CLKR high to internal FSR valid	$t_{d(CKRH-FRV)}$		CLKR int			-11	3	
9	Delay time, CLKX high to internal FSX valid	$t_{d(CKXH-FXV)}$		CLKX int			-11	3	
				CLKX ext			3	9	
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		CLKX int			-9	4	
				CLKX ext			3	9	
13	Delay time, CLKX high to DX valid 39/	$t_{d(CKXH-DXV)}$		CLKX int			-9+D1	7+D2	
				CLKX ext			3+D1	19+D2	
14	Delay time, FSX high to DX valid	$t_{d(FXH-DXV)}$		FSX int			-1	3	
	ONLY applies when in data delay 0 (XDATDLY = 00b) mode			FSX ext			3	9	

Switching characteristics for McBSP 32/ 37/			**[Device type 02 and 03]**		Device type 02 -167		Device type 03 -167		
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	$t_{d(CKSH-CKRSH)}$	See figure 23		1.8	10	1.8	10	ns
2	Cycle time, CLKR/X 25/ 33/	$t_{c(CKRX)}$		CLKR/X int	2P		2P		
3	Pulse duration, CLKR/X high or CLKR/X low 38/	$t_{w(CKRX)}$		CLKR/X int	C-1	C+1	C-1	C+1	
4	Delay time, CLKR high to internal FSR valid	$t_{d(CKRH-FRV)}$		CLKR int	-2	3	-2	3	
9	Delay time, CLKX high to internal FSX valid	$t_{d(CKXH-FXV)}$		CLKX int	-2	3	-2	3	
				CLKX ext	2	9	2	9	
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		CLKX int	-1	4	-1	4	
				CLKX ext	1.5	10	1.5	10	
13	Delay time, CLKX high to DX valid 39/	$t_{d(CKXH-DXV)}$		CLKX int	-3.2+D1	4+D2	-3.2+D1	4+D2	
				CLKX ext	0.5+D1	10+D2	0.5+D1	10+D2	
14	Delay time, FSX high to DX valid	$t_{d(FXH-DXV)}$		FSX int	-1.5	4.5	-1.5	7.5	
	ONLY applies when in data delay 0 (XDATDLY = 00b) mode			FSX ext	2	9	2	11.5	

Timing requirements for FSR when GSYNC = 1				-100, -167		
1	Setup time, FSR high before CLKS high	$t_{su(FRH-CKSH)}$	See figure 24	4		ns
2	Hold time, FSR high after CLKS high	$t_{h(CKSH_FRH)}$		4		

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 [Device type 01] 25/ 40/				-100				
				Master		Slave		
4	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 25	26		2-6P		ns
5	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		4		6+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 [Device type 02 and 03] 25/ 40/				-167				
				Master		Slave		
4	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 25	12		2-6P		ns
5	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		4		5+12P		
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 [Device type 01] 25/ 40/				-100				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX low 41/	$t_{h(CKXL-FXL)}$	See figure 25	T-9	T+9			ns
2	Delay time, FSX low to CLKX high 42/	$t_{d(FXL-CKXH)}$		L-9	L+9			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-9	9	6P+4	10P+20	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		L-9	L+9			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+3	6P+20	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+20	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 [Device type 02] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX low 41/	$t_{h(CKXL-FXL)}$	See figure 25	T-2	T+3			ns
2	Delay time, FSX low to CLKX high 42/	$t_{d(FXL-CKXH)}$		L-2	L+3			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+7	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		L-4	L+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+1.5	6P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 [Device type 03] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX low 41/	$t_{h(CKXL-FXL)}$	See figure 25	T-2	T+3			ns
2	Delay time, FSX low to CLKX high 42/	$t_{d(FXL-CKXH)}$		L-2	L+3			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+7	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		L-2	L+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+3	6P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 [Device type 01] 25/ 40/				-100				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 26	26		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		6+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 [Device type 02 and 03] 25/ 40/				-167				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 26	12		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+12P		
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 [Device type 01] 25/ 40/				-100				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX low 41/	$t_{h(CKXL-FXL)}$	See figure 26	L-9	L+9			ns
2	Delay time, FSX low to CLKX high 42/	$t_{d(FXL-CKXH)}$		T-9	T+9			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-9	9	6P+4	10P+20	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-9	9	6P+3	10P+20	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H-9	H+9	4P+2	8P+20	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 [Device type 02] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX low 41/	$t_{h(CKXL-FXL)}$	See figure 26	L-2	L+3			ns
2	Delay time, FSX low to CLKX high 42/	$t_{d(FXL-CKXH)}$		T-2	T+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-3	4	6P+1.5	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H-2	H+4	4P+2	8P+17	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 [Device type 03] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX low 53/	$t_{h(CKXL-FXL)}$	See figure 26	L-2	L+3			ns
2	Delay time, FSX low to CLKX high 54/	$t_{d(FXL-CKXH)}$		T-2	T+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-2	4	6P+3	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H-2	H+6.5	4P+2	8P+17	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1 [Device type 01] 25/ 40/				-100				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 27	26		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		6+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1 [Device type 02 and 03] 25/ 40/				-167				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 27	12		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+12P		
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1 [Device type 01] 25/ 40/				-100				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX high 41/	$t_{h(CKXH-FXL)}$	See figure 27	T-9	T+9			ns
2	Delay time, FSX low to CLKX low 42/	$t_{d(FXL-CKXL)}$		H-9	H+9			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-9	9	6P+4	10P+20	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		H-9	H+9			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+3	6P+20	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+20	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 [Device type 02] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX high 41/	$t_{h(CKXH-FXL)}$	See figure 27	T-2	T+3			ns
2	Delay time, FSX low to CLKX low 42/	$t_{d(FXL-CKXL)}$		H-2	H+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		H-3.6	H+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+1.5	6P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1 [Device type 03] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX high 41/	$t_{h(CKXH-FXL)}$	See figure 27	T-2	T+3			ns
2	Delay time, FSX low to CLKX low 42/	$t_{d(FXL-CKXL)}$		H-2	H+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		H-2	H+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+3	6P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1 [Device type 01] 25/ 40/				-100				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 28	26		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		6+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1 [Device type 02 and 03] 25/ 40/				-167				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 28	12		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+12P		
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1 [Device type 01] 25/ 40/				-100				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX high 41/	$t_{h(CKXH-FXL)}$	See figure 28	H-9	H+9			ns
2	Delay time, FSX low to CLKX low 42/	$t_{d(FXL-CKXL)}$		T-9	T+9			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-9	9	6P+4	10P+20	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		-9	9	6P+3	10P+20	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L-9	L+9	4P+2	8P+20	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1 [Device type 02] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX high 41/	$t_{h(CKXH-FXL)}$	See figure 28	H-2	H+3			ns
2	Delay time, FSX low to CLKX low 42/	$t_{d(FXL-CKXL)}$		T-2	T+3			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		-3.6	4	6P+1.5	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L-2	L+4	4P+2	8P+17	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1 [Device type 03] 25/ 40/				-167				
				Master 38/		Slave		
1	Hold time, FSX low after CLKX high 41/	$t_{h(CKXH-FXL)}$	See figure 28	H-2	H+3			ns
2	Delay time, FSX low to CLKX low 42/	$t_{d(FXL-CKXL)}$		T-2	T+3			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		-2	4	6P+3	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L-2	L+6.5	4P+2	8P+17	

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
	TIMER TIMING							
Timing requirements for timer inputs 25/						-100, -167		
1	Pulse duration, TNP high	$t_{w(TINPH)}$	See figure 29			2P		ns
2	Pulse duration, TNP low	$t_{w(TINPL)}$				2P		
Switching characteristics for time outputs 25/						-100, -167		
3	Pulse duration, TOUT high	$t_{w(TOUTH)}$	See figure 29			4P-3		ns
4	Pulse duration, TOUT low	$t_{w(TOUTL)}$				4P-3		
	GENERAL PURPOSE INPUT/OUTPUT (GPIO) PORT TIMING [Device type 03 and 04 only]							
Timing requirements for GPIO inputs 25/ 43/						-167		
1	Pulse duration, GPIx high	$t_{w(GPIH)}$	See figure 30			4P		ns
2	Pulse duration, GPIx low	$t_{w(GPIL)}$				4P		
Switching characteristics for GPIO outputs 25/ 44/						-167		
3	Pulse duration, GPOx high	$t_{w(GPOH)}$	See figure 30			12P-3		ns
4	Pulse duration, GPOx low	$t_{w(GPOL)}$				12P-3		
	JTAG TEST PORT TIMING							
Timing requirements for JTAG test port				-100		-167		
1	Cycle time, TCK	$t_{c(TCK)}$	See figure 36	35		35		ns
3	Setup time, TDI/TMS/ $\overline{TRST}$ valid before TCK high	$t_{su(TDIV-TCKH)}$		10		10		
4	Hold time, TDI/TMS/ $\overline{TRST}$ valid after TCK high	$t_{h(TCKH-TDIV)}$		5		7		
Switching characteristics for JTAG test port				-100		-167		
2	Delay time, TCK low to TDO valid	$t_{d(TCKL-TDOV)}$	See figure 36	-3	18	0	15	ns

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Test conditions are over recommended ranges of supply voltage and operating case temperature unless otherwise specified.

3/ For device type 01, these currents were measured with average cativity (50% high/50% low power). For more details on CPU, peripheral, and I/o cativity, see manufacturer report.
For device type 02 and 03, these currents were measured with average activity (50% high/50% low power) at 25°C case temperature and 100 MHz EMIF. This model represents a device performing high DSP activity operations 50% of the time, and the remainder performing low DSP activity operations. The high/low DSP activity models are defined as follow

High DSP activity model:
- CPU: 8 instructions/cycle with 2LDDW instructions [L1 Data Memory: 128 bits/cycle via LDDW instructions; L1 program memory: 256 bits/cycle; L2/EMIF EDMA: 50% writes, 50% reads to/from SDRAM (50% bit switching)]
- McBSP: 2 channels at E1 rate
- Times: 2 times at maximum rate.

Low DSP activity model:
- CPU: 2 instructions/cycle with 1 LDH instruction [L1 data memory: 16 bits/cycle; L1 program memory: 256 bits per 4 cycles; L2/EMIF EDMA: None]
- McBSP: 2 channels at E1 rate
- Times: 2 times at maximum rate.

The actual current draw is highly application dependent. For more details on core and I/O activity, refer to manufacturer report.

4/ The reference points for the rise and fall transactions are measured at V_{IL} max and V_{IH} min.

5/ C = CLKIN cycle time in nanoseconds (ns). For example, when CLKIN frequency is 25 MHz, use C = 40 ns.

6/ See PLL and PLL controller section from manufacturer data.

7/ The reference points for the rise and fall transactions are measured at V_{OL} max and V_{OH} min.

8/ PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.

9/ P = 1/CPU cloc frequency in nanoseconds (ns).

10/ C2 = CLKOUT2 period in ns. CLKOUT2 period is determined by the PLL controller output SYSCLK2 period, which must be set to CPU period divide by 2.

11/ C3 = CLKOUT3 period in ns. CLKOUT3 period is a divide down of the CPU clock, configurable via the RATIO field in the PLLDIV3 register.

12/ E = ECLKIN period in ns.

13/ EH is high period of ECLKIN in ns and EL is the low period of ECLKIN in ns.

14/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = 2E) to ensure setup and hold time is met.

15/ RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

16/ E = ECLKOUT period in ns.

17/ Select signals include: $\overline{CE[3:0]}$, $\overline{BE[1:0]}$, EA[21:2], and $\overline{AOE}$.

18/ Device type 01, 02, and 03 SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

19/ Make sure the external SBSRAM meets the timing specifications of the device type 01. Delays or buffers may be needed to compensate for any timing differences. IBIS analysis should be used to correctly model the system interface.

20/ $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$, and $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$ operate as $\overline{SSADSS}$, $\overline{SSOE}$, and $\overline{SSWE}$, respectively, during SBSRAM accesses.

21/ Device type 01, 02, and 03 SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

22/ $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$, and $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$ operate as $\overline{SDCAS}$, $\overline{SDWE}$, and $\overline{SDRAS}$, respectively, during SDRAM accesses.

23/ EMIF bus consists of $\overline{CE[3:0]}$, $\overline{BE[1:0]}$, ED[15:0], EA[21:2], $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$, and $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$.

24/ All pending EMIF transactions are allowed to complete before $\overline{HOLDA}$ is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.

25/ P = 1/CPU clock frequency in nanoseconds (ns). For example, when running parts at 100 MHz, use P = 10 ns.

26/ This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x4 when CLKIN and PLL are stable.

27/ This parameter applies to CLKMODE x4 only (it does not apply to CLKMODE x1). The $\overline{RESET}$ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 μs to stabilize following power up or after PLL configuration has been changed. During that time $\overline{RESET}$ must be asserted to ensure proper device operation. See the clock PLL in manufacturer data for PLL clock times.

28/ EMIF Z group consists of: EA[21:2], ED[15:0], $\overline{CE[3:0]}$, $\overline{BE[1:0]}$, $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$, and $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$

EMIF high group consists of: $\overline{HOLDA}$
EMIF low group consists of: BUSREQ
Z group consists of: CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, TOUT0, and TOUT1.

29/ P = 1/CPU clock frequency in ns. Note that while internal reset is asserted low, the CPU clock (SYSCLK1) period is equal to the input clock (CLKIN) period multiplied by 8. For example, if the CLKIN period is 20 ns, then the CPU clock (SYSCLK1) period is 20 ns x 8 = 160 ns. Therefore, P = SYSCLK1 = 160 ns while internal reset is asserted.

30/ The internal reset is stretched exactly 512 x CLKIN cycles if CLKIN is used (CLKMODE0 = 1). If the input clock (CLKIN) is not stable when RESET is deasserted, the actual delay may vary.

31/ 512 x CLKIN period.

32/ CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

33/ The minimum CLKR/X period is twice the CPU cycle time (2P). This means that the maximum bit rate for communications between the McBSP and other device is 50 Mbps for 100 MHz CPU clock; where the McBSP is either the master or slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP to McBSP communication is 33 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 30 ns (33 MHz), whichever value is larger. For example, when running parts at 100 MHz (P = 10 ns), use 30 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). The maximum bit rate for McBSP to McBSP communications applies when the serial port is a Master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

34/ $0.5t_{c(CKRX)}$-1

35/ The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other device is 75 Mbps for 150 MHz CPU clock; where the McBSP is either the master or slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP to McBSP communication is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP to McBSP communications applies when the serial port is a Master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

36/ This parameter is applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

37/ Minimum delay times also represent minimum output hold times.

38/ C = H or L
S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

39/ Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 2P, D2 = 4P

40/ For all SPI slave modes, CLKG is programmed as ½ of the CPU clock by setting CLKSM = CLKGDV = 1.

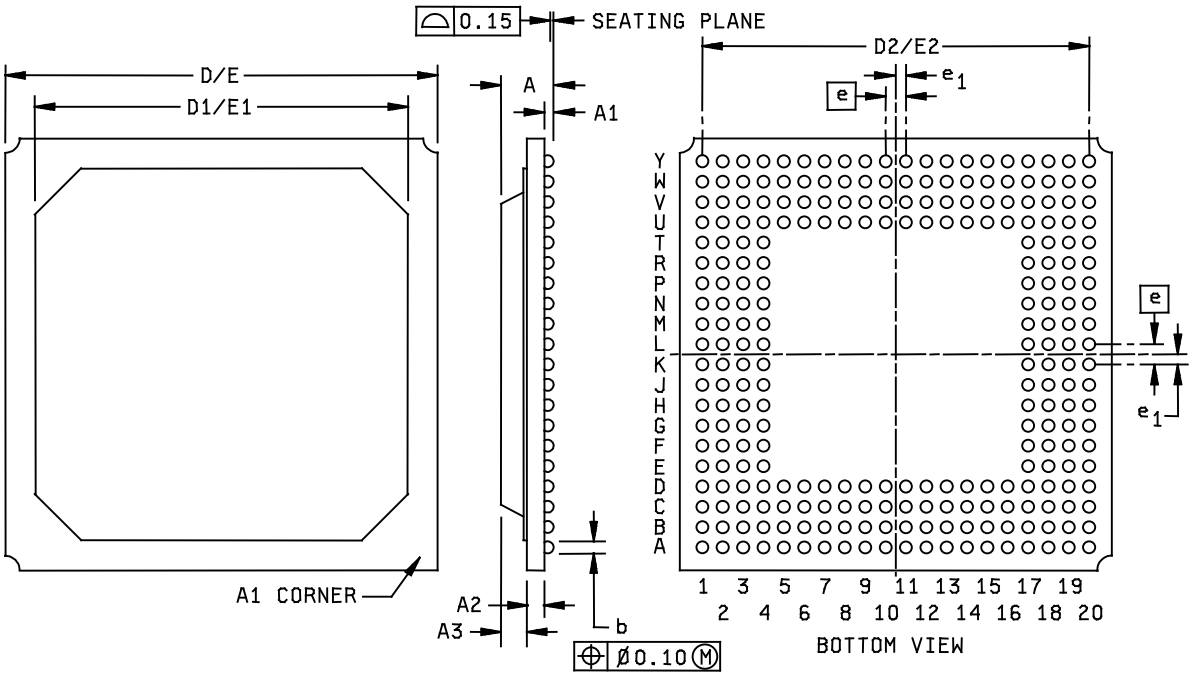
41/ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

42/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

43/ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the DSP recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to at least 24P to allow the DSP enough time to access the GPIO register through the CFGBUS.

44/ The number of CFGBUS cycles between two back-to-back CFGBUS writes to the GPIO register is 12 SYSCLK1 cycles; therefore, the minimum GPOx pulse width is 12P.

Case X



Notes:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-151.

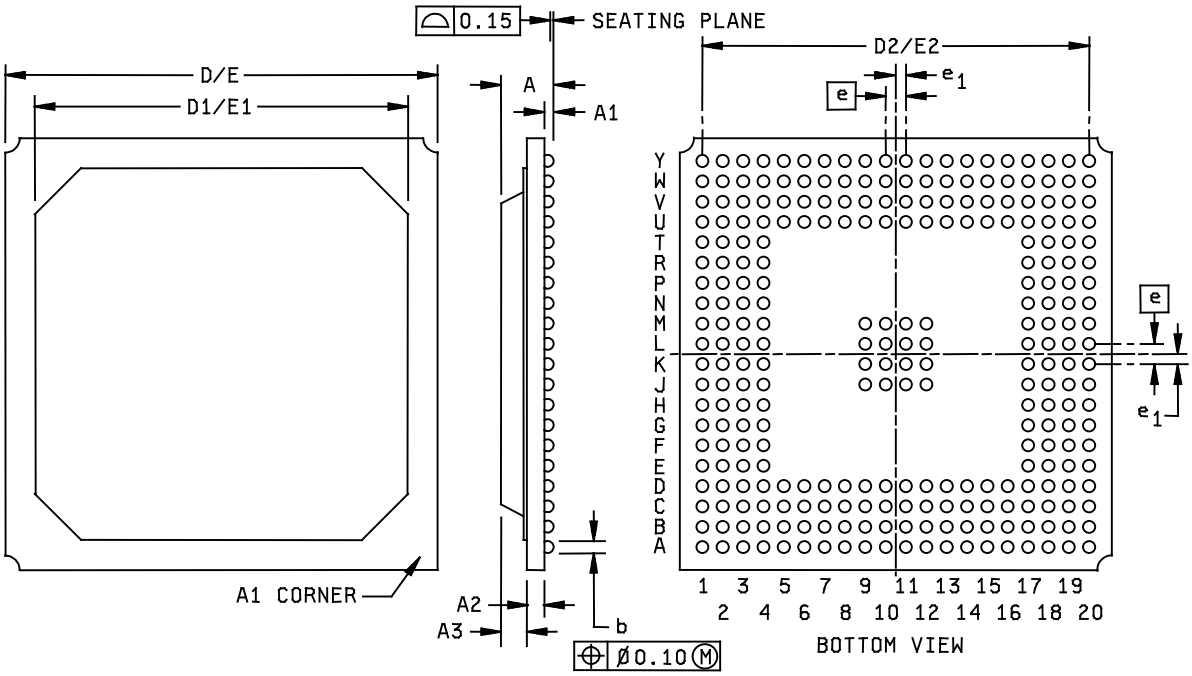
FIGURE 1. Case outlines.

Case X

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A		2.32		0.091
A1	0.50	0.70	0.020	0.028
A2	0.30	0.40	0.012	0.016
A3	1.17 TYP		0.046 TYP	
b	0.60	0.90	0.024	0.035
D/E	26.80	27.20	1.055	1.071
D1/E1	23.80	24.70	0.937	0.965
D2/E2	24.13 TYP		0.950 TYP	
e	1.27 NOM		0.050 NOM	
e1	0.635 NOM		0.025 NOM	

FIGURE 1. Case outline - Continued.

Case Y



Notes:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-151.

FIGURE 1. Case outline - Continued.

Case Y

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A		2.57		0.101
A1	0.50	0.70	0.020	0.028
A2	0.57	0.65	0.022	0.026
A3	1.12	1.22	0.044	0.048
b	0.60	0.90	0.024	0.035
D/E	26.80	27.20	1.055	1.071
D1/E1	23.80	24.20	0.937	0.953
D2/E2	24.13 TYP		0.950 TYP	
e	1.27 NOM		0.050 NOM	
e1	0.635 NOM		0.025 NOM	

FIGURE 1. Case outline - Continued.

Case X
[Device type 01 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
A1	V_{SS}	B1	V_{SS}	C1	EXT_INT5	D1	DV_{DD}
A2	V_{SS}	B2	CV_{DD}	C2	EXT_INT4	D2	EXT_INT6
A3	CLKIN	B3	DV_{DD}	C3	CV_{DD}	D3	RSV
A4	PLLV	B4	V_{SS}	C4	CLKMODE0	D4	V_{SS}
A5	RSV	B5	PLLF	C5	DV_{DD}	D5	CV_{DD}
A6	TCK	B6	$\overline{TRST}$	C6	PLLG	D6	CV_{DD}
A7	TDI	B7	TMS	C7	CV_{DD}	D7	CLKOUT1
A8	TDO	B8	DV_{DD}	C8	V_{SS}	D8	V_{SS}
A9	CV_{DD}	B9	EMU1	C9	V_{SS}	D9	EMU0
A10	CV_{DD}	B10	EMU3	C10	DV_{DD}	D10	EMU2
A11	V_{SS}	B11	V_{SS}	C11	EMU4	D11	CV_{DD}
A12	CV_{DD}	B12	EMU5	C12	RSV	D12	RSV
A13	$\overline{RESET}$	B13	DV_{DD}	C13	NMI	D13	V_{SS}
A14	V_{SS}	B14	RSV	C14	RSV	D14	CV_{DD}
A15	RSV	B15	V_{SS}	C15	RSV	D15	CV_{DD}
A16	RSV	B16	RSV	C16	RSV	D16	DV_{DD}
A17	DV_{DD}	B17	LENDIAN	C17	RSV	D17	V_{SS}
A18	RSV	B18	RSV	C18	CV_{DD}	D18	RSV
A19	V_{SS}	B19	CV_{DD}	C19	BOOTMODE1	D19	DV_{DD}
A20	V_{SS}	B20	V_{SS}	C20	BOOTMODE0	D20	RSV
E1	CLKS1	F1	TOUT1	G1	TOUT0	H1	FSX0
E2	V_{SS}	F2	TINP1	G2	TINP0	H2	DX0
E3	EXT_INT7	F3	DV_{DD}	G3	CLKX0	H3	CLKR0
E4	V_{SS}	F4	CV_{DD}	G4	V_{SS}	H4	V_{SS}
E17	V_{SS}	F17	CV_{DD}	G17	V_{SS}	H17	V_{SS}
E18	RSV	F18	RSV	G18	RSV	H18	DV_{DD}
E19	RSV	F19	V_{SS}	G19	RSV	H19	RSV
E20	RSV	F20	RSV	G20	RSV	H20	RSV

FIGURE 2. Terminal connections.

Case X
[Device type 01 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
J1	DR0	K1	CV_{DD}	L1	FSX1	M1	CLKR1
J2	DV_{DD}	K2	V_{SS}	L2	DX1	M2	DR1
J3	FSR0	K3	CLKS0	L3	CLKX1	M3	FSR1
J4	V_{SS}	K4	CV_{DD}	L4	CV_{DD}	M4	V_{SS}
J17	$\overline{HOLD}$	K17	CV_{DD}	L17	CV_{DD}	M17	V_{SS}
J18	$\overline{HOLDA}$	K18	ED0	L18	ED2	M18	DV_{DD}
J19	BUSREQ	K19	ED1	L19	ED3	M19	ED4
J20	RSV	K20	V_{SS}	L20	CV_{DD}	M20	ED5

FIGURE 2. Terminal connections - Continued.

Case X
[Device type 01 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
N1	DV_{DD}	P1	RSV	R1	DV_{DD}	T1	RSV
N2	RSV	P2	RSV	R2	RSV	T2	RSV
N3	RSV	P3	RSV	R3	RSV	T3	DV_{DD}
N4	V_{SS}	P4	V_{SS}	R4	CV_{DD}	T4	V_{SS}
N17	V_{SS}	P17	V_{SS}	R17	CV_{DD}	T17	V_{SS}
N18	ED6	P18	ED9	R18	DV_{DD}	T18	ED13
N19	ED7	P19	V_{SS}	R19	ED11	T19	ED15
N20	ED8	P20	ED10	R20	ED12	T20	ED14
U1	RSV	V1	RSV	W1	V_{SS}	Y1	V_{SS}
U2	RSV	V2	RSV	W2	CV_{DD}	Y2	V_{SS}
U3	RSV	V3	CV_{DD}	W3	DV_{DD}	Y3	RSV
U4	V_{SS}	V4	RSV	W4	RSV	Y4	RSV
U5	DV_{DD}	V5	RSV	W5	V_{SS}	Y5	ARDY
U6	CV_{DD}	V6	$\overline{CE3}$	W6	$\overline{CE2}$	Y6	EA2
U7	DV_{DD}	V7	EA3	W7	EA4	Y7	DV_{DD}
U8	V_{SS}	V8	EA5	W8	EA6	Y8	EA7
U9	V_{SS}	V9	EA8	W9	DV_{DD}	Y9	EA9
U10	CV_{DD}	V10	EA10	W10	$\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$	Y10	ECLKOUT
U11	CV_{DD}	V11	$\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$	W11	V_{SS}	Y11	ECLKIN
U12	DV_{DD}	V12	$\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$	W12	DV_{DD}	Y12	CLKOUT2/GP[2]
U13	V_{SS}	V13	DV_{DD}	W13	EA11	Y13	V_{SS}
U14	CV_{DD}	V14	EA12	W14	EA13	Y14	EA14
U15	CV_{DD}	V15	DV_{DD}	W15	EA15	Y15	EA16
U16	DV_{DD}	V16	EA17	W16	V_{SS}	Y16	EA18
U17	V_{SS}	V17	$\overline{CE0}$	W17	EA19	Y17	DV_{DD}
U18	EA21	V18	CV_{DD}	W18	$\overline{CE1}$	Y18	EA20
U19	$\overline{BE1}$	V19	DV_{DD}	W19	CV_{DD}	Y19	V_{SS}
U20	V_{SS}	V20	$\overline{BE0}$	W20	V_{SS}	Y20	RSV

FIGURE 2. Terminal connections - Continued.

Case Y
[Device type 02 and 03 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
A1	V_{SS}	B1	V_{SS}	C1	GP[5](EXT_INT5)	D1	DV_{DD}
A2	V_{SS}	B2	CV_{DD}	C2	GP[4](EXT_INT4)	D2	GP[6](EXT_INT6)
A3	CLKIN	B3	DV_{DD}	C3	CV_{DD}	D3	EMU2
A4	CV_{DD}	B4	V_{SS}	C4	CLKMODE0	D4	V_{SS}
A5	RSV	B5	RSV	C5	PLLHV	D5	CV_{DD}
A6	TCK	B6	$\overline{TRST}$	C6	V_{SS}	D6	CV_{DD}
A7	TDI	B7	TMS	C7	CV_{DD}	D7	RSV
A8	TDO	B8	DV_{DD}	C8	V_{SS}	D8	V_{SS}
A9	CV_{DD}	B9	EMU1	C9	V_{SS}	D9	EMU0
A10	CV_{DD}	B10	EMU3	C10	DV_{DD}	D10	CLKOUT3
A11	V_{SS}	B11	RSV	C11	EMU4	D11	CV_{DD}
A12	RSV	B12	EMU5	C12	RSV	D12	RSV
A13	$\overline{RESET}$	B13	DV_{DD}	C13	NMI	D13	V_{SS}
A14	V_{SS}	B14	RSV	C14	RSV	D14	CV_{DD}
A15	RSV	B15	V_{SS}	C15	$\overline{EMIFBE}$	D15	CV_{DD}
A16	RSV	B16	RSV	C16	RSV	D16	DV_{DD}
A17	DV_{DD}	B17	LENDIAN	C17	RSV	D17	V_{SS}
A18	RSV	B18	RSV	C18	CV_{DD}	D18	RSV
A19	V_{SS}	B19	CV_{DD}	C19	BOOTMODE1	D19	DV_{DD}
A20	V_{SS}	B20	V_{SS}	C20	BOOTMODE0	D20	RSV
E1	CLKS1	F1	TOUT1	G1	TOUT0	H1	FSX0
E2	V_{SS}	F2	TINP1	G2	TINP0	H2	DX0
E3	GP[7](EXT_INT7)	F3	DV_{DD}	G3	CLKX0	H3	CLKR0
E4	V_{SS}	F4	CV_{DD}	G4	V_{SS}	H4	V_{SS}
E17	V_{SS}	F17	CV_{DD}	G17	V_{SS}	H17	V_{SS}
E18	RSV	F18	RSV	G18	RSV	H18	DV_{DD}
E19	RSV	F19	V_{SS}	G19	RSV	H19	RSV
E20	RSV	F20	RSV	G20	RSV	H20	RSV

FIGURE 2. Terminal connections – Continued.

Case Y
[Device type 02 and 03 only]

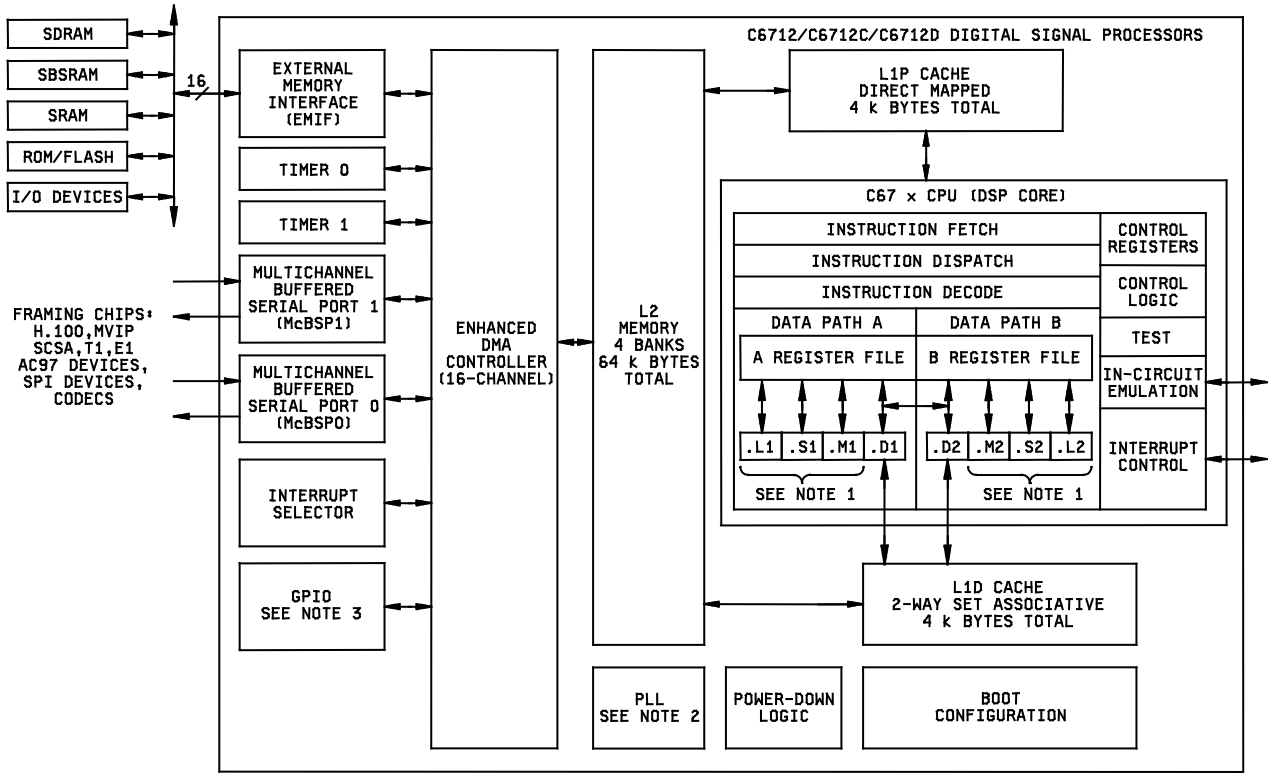
Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
J1	DR0	K1	CV_{DD}	L1	FSX1	M1	CLKR1
J2	DV_{DD}	K2	V_{SS}	L2	DX1	M2	DR1
J3	FSR0	K3	CLKS0	L3	CLKX1	M3	FSR1
J4	V_{SS}	K4	CV_{DD}	L4	CV_{DD}	M4	V_{SS}
J9	V_{SS}	K9	V_{SS}	L9	V_{SS}	M9	V_{SS}
J10	V_{SS}	K10	V_{SS}	L10	V_{SS}	M10	V_{SS}
J11	V_{SS}	K11	V_{SS}	L11	V_{SS}	M11	V_{SS}
J12	V_{SS}	K12	V_{SS}	L12	V_{SS}	M12	V_{SS}
J17	$\overline{HOLD}$	K17	CV_{DD}	L17	CV_{DD}	M17	V_{SS}
J18	$\overline{HOLDA}$	K18	ED0	L18	ED2	M18	DV_{DD}
J19	BUSREQ	K19	ED1	L19	ED3	M19	ED4
J20	RSV	K20	V_{SS}	L20	CV_{DD}	M20	ED5

FIGURE 2. Terminal connections - Continued.

Case Y
[Device type 02 and 03 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
N1	RSV	P1	RSV	R1	DV_{DD}	T1	RSV
N2	RSV	P2	RSV	R2	RSV	T2	RSV
N3	RSV	P3	RSV	R3	RSV	T3	DV_{DD}
N4	V_{SS}	P4	V_{SS}	R4	CV_{DD}	T4	V_{SS}
N17	V_{SS}	P17	V_{SS}	R17	CV_{DD}	T17	V_{SS}
N18	ED6	P18	ED9	R18	DV_{DD}	T18	ED13
N19	ED7	P19	V_{SS}	R19	ED11	T19	ED15
N20	ED8	P20	ED10	R20	ED12	T20	ED14
U1	RSV	V1	RSV	W1	V_{SS}	Y1	V_{SS}
U2	RSV	V2	RSV	W2	CV_{DD}	Y2	V_{SS}
U3	RSV	V3	CV_{DD}	W3	DV_{DD}	Y3	RSV
U4	V_{SS}	V4	RSV	W4	RSV	Y4	RSV
U5	DV_{DD}	V5	RSV	W5	V_{SS}	Y5	ARDY
U6	CV_{DD}	V6	$\overline{CE3}$	W6	$\overline{CE2}$	Y6	EA2
U7	DV_{DD}	V7	EA3	W7	EA4	Y7	DV_{DD}
U8	V_{SS}	V8	EA5	W8	EA6	Y8	EA7
U9	V_{SS}	V9	EA8	W9	DV_{DD}	Y9	EA9
U10	CV_{DD}	V10	EA10	W10	$\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$	Y10	ECLKOUT
U11	CV_{DD}	V11	$\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$	W11	V_{SS}	Y11	ECLKIN
U12	DV_{DD}	V12	$\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$	W12	DV_{DD}	Y12	CLKOUT2/GP[2]
U13	V_{SS}	V13	DV_{DD}	W13	EA11	Y13	V_{SS}
U14	CV_{DD}	V14	EA12	W14	EA13	Y14	EA14
U15	CV_{DD}	V15	DV_{DD}	W15	EA15	Y15	EA16
U16	DV_{DD}	V16	EA17	W16	V_{SS}	Y16	EA18
U17	V_{SS}	V17	$\overline{CE0}$	W17	EA19	Y17	DV_{DD}
U18	EA21	V18	CV_{DD}	W18	$\overline{CE1}$	Y18	EA20
U19	$\overline{BE1}$	V19	DV_{DD}	W19	CV_{DD}	Y19	V_{SS}
U20	V_{SS}	V20	$\overline{BE0}$	W20	V_{SS}	Y20	V_{SS}

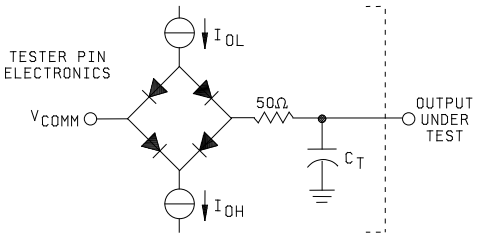
FIGURE 2. Terminal connections - Continued.



Notes:

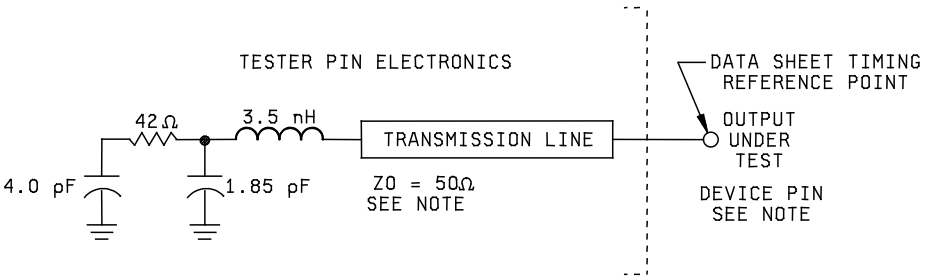
1. In addition to fixed point instructions, these functional units execute floating point instructions.
2. Device type 02 or 03 has a software configurable PLL (with x4 through x25 multiplier and /1 through /32 divider) and a PLL controller which is different from the hardware PLL peripheral on the device type 01.
3. Applicable to the device type 02 and 03 only.

FIGURE 3. Block diagram.



AC timing measurements for device type 01 only

Where: I_{OL} = 2 mA
I_{OH} = 2 mA
V_{comm+} = 0.8 V
C_T = 10-15 pF typical load capacitance



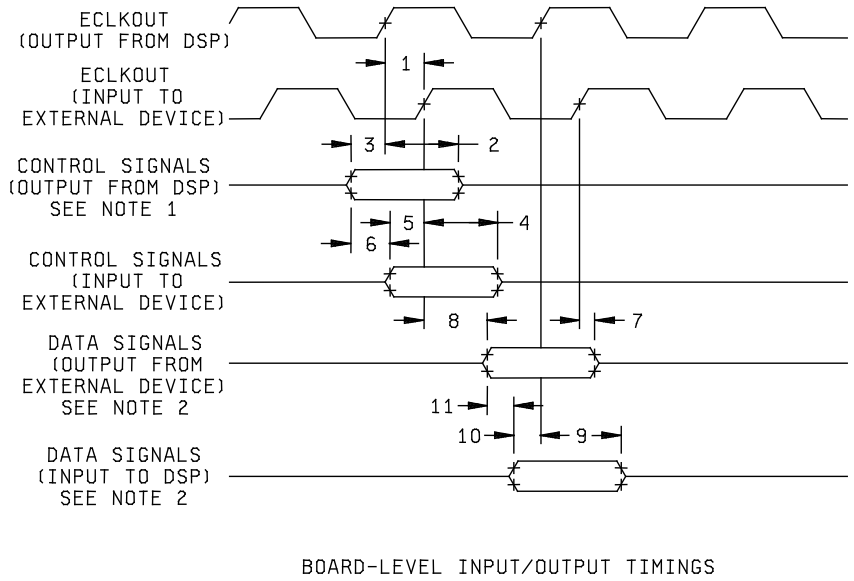
AC timing measurements for device type 02 and 03 only

Note:
The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
Input requirements in this data sheet are tested with an input slew rate of < 4 Volts pre nanosecond (4 V/ns) at the device pin.

FIGURE 4. Test load circuit.

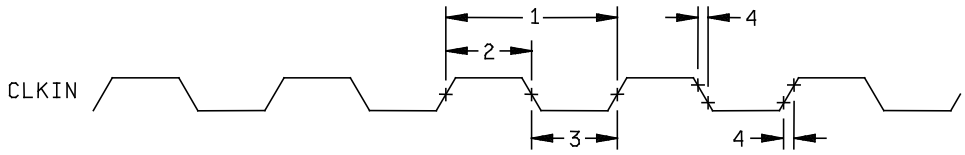
No.	Description
1	Clock route delay
2	Minimum DSP hold time
3	Minimum DSP setup time
4	External device hold time requirement
5	External device setup time requirement
6	Control signal route delay
7	External device hold time
8	External device access time
9	DSP hold time requirement
10	DSP setup time requirement
11	Data route delay

Board level timings example



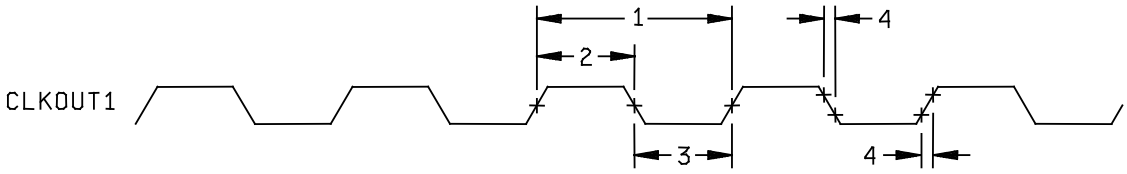
Notes:
1. Control signals include data for Writes.
2. Data signals are generated during Reads from an external device.

FIGURE 5. Board level input/output timings.



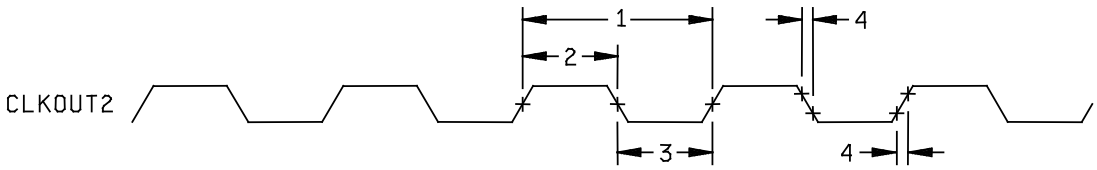
CLKIN TIMING

FIGURE 6 Timing waveforms.



CLKOUT1 TIMINGS [FOR DEVICE TYPES 010 AND 02 ONLY]

FIGURE 7 Timing waveforms.



CLKOUT2 TIMINGS [FOR DEVICE TYPES 01 AND 02]

FIGURE 8 Timing waveforms.

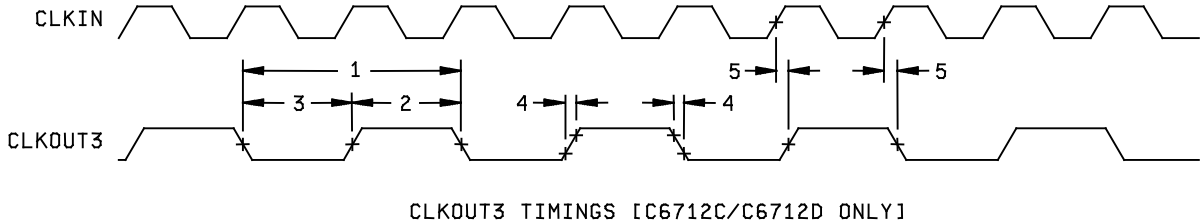


FIGURE 9 Timing waveforms.

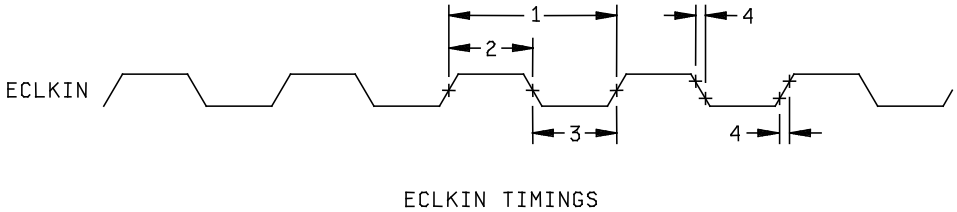


FIGURE 10 Timing waveforms.

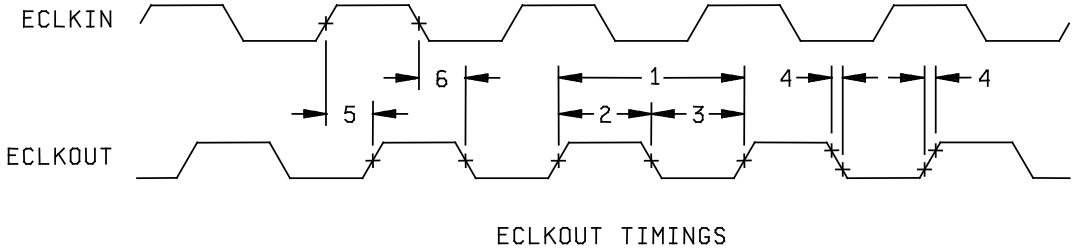
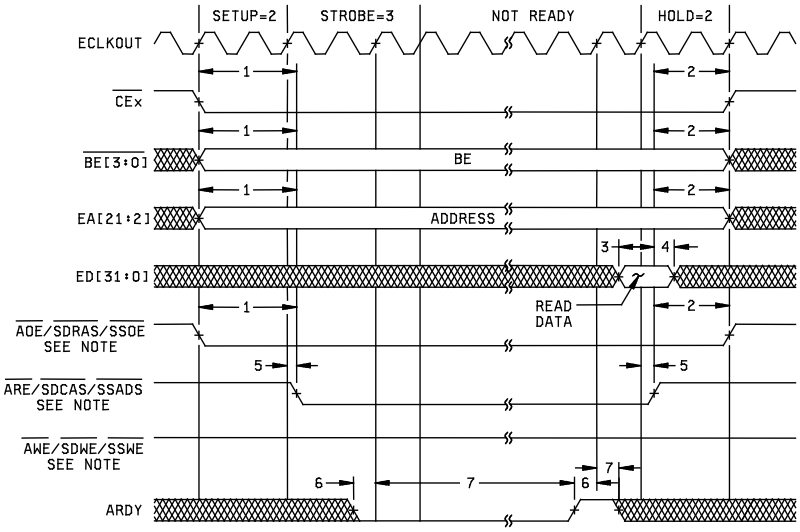
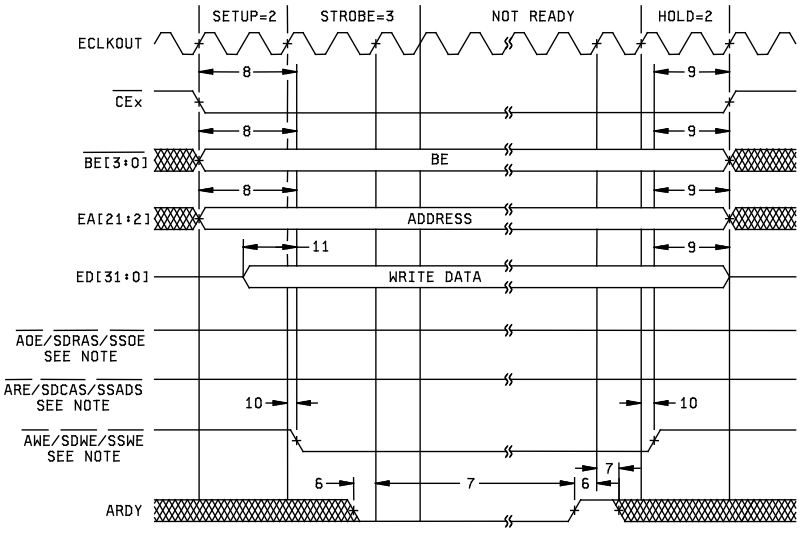


FIGURE 11 Timing waveforms.



ASYNCHRONOUS MEMORY READ TIMING

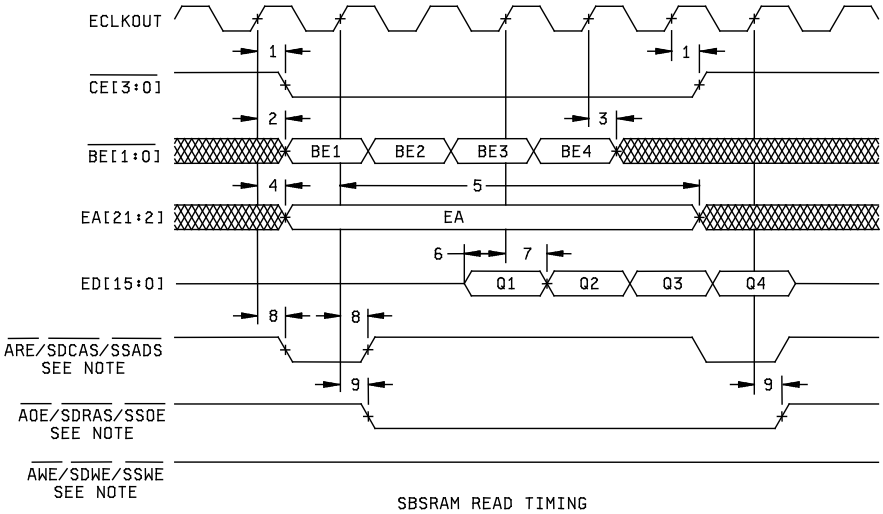


ASYNCHRONOUS MEMORY WRITE TIMING

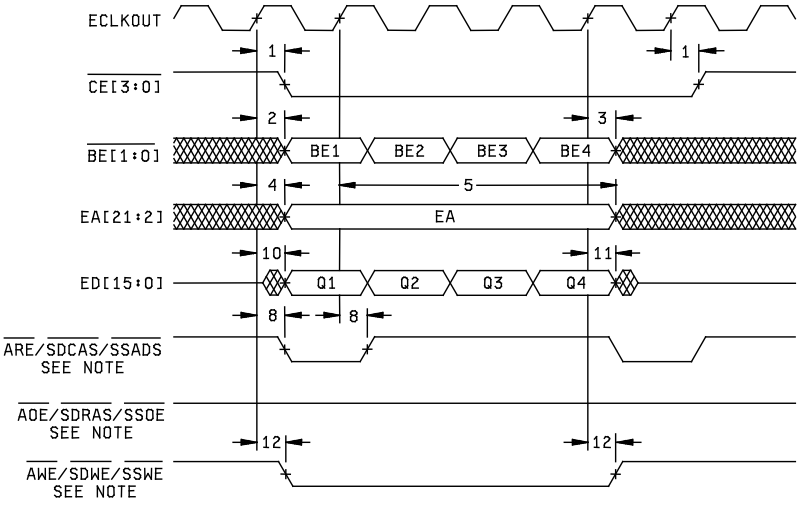
Note:

$\overline{\text{AOE}}$ / $\overline{\text{SDRAS}}$ / $\overline{\text{SSOE}}$, $\overline{\text{ARE}}$ / $\overline{\text{SDCAS}}$ / $\overline{\text{SSADS}}$, and $\overline{\text{AWE}}$ / $\overline{\text{SDWE}}$ / $\overline{\text{SSWE}}$ operate as $\overline{\text{AOE}}$ (identified under select signals), $\overline{\text{ARE}}$, and $\overline{\text{AWE}}$ respectively, during asynchronous memory accesses.

FIGURE 12 Timing waveforms.



SBSRAM READ TIMING

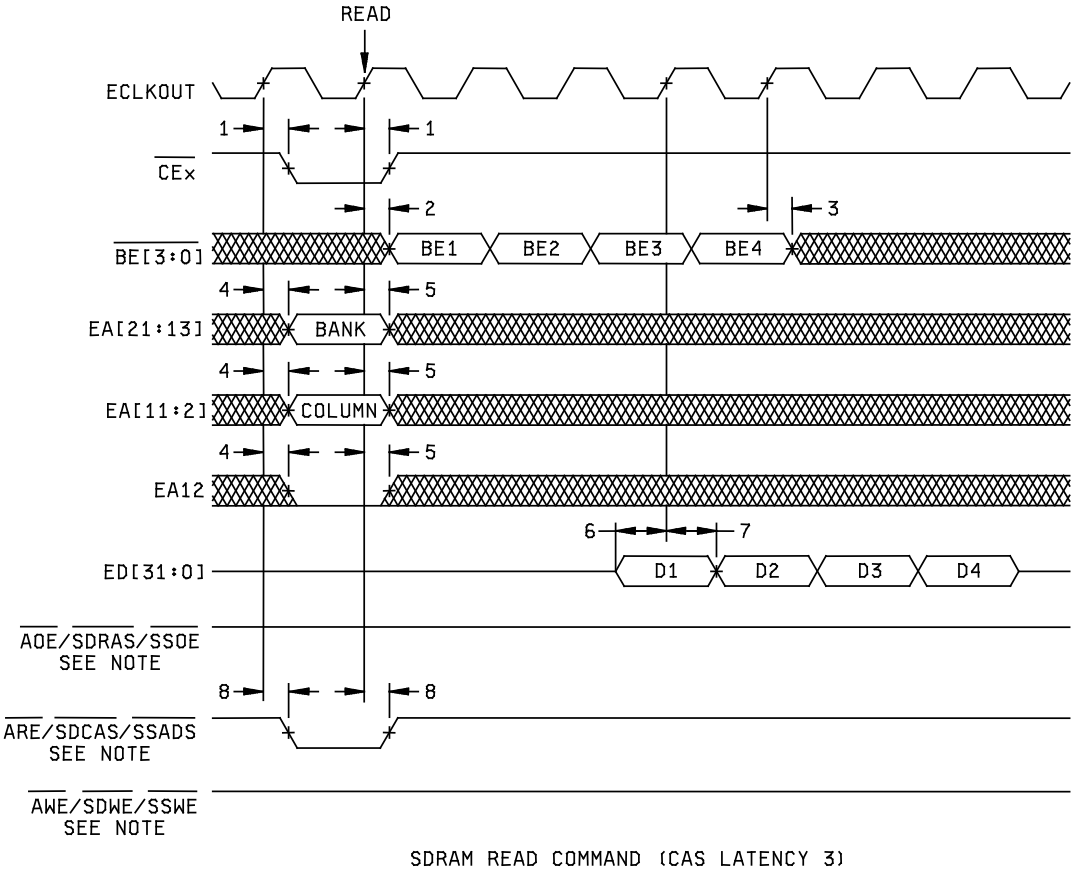


SBSRAM WRITE TIMING

Note:

$\overline{\text{ARE}}$ / $\overline{\text{SDCAS}}$ / $\overline{\text{SSADS}}$, $\overline{\text{AOE}}$ / $\overline{\text{SDRAS}}$ / $\overline{\text{SSOE}}$, and $\overline{\text{AWE}}$ / $\overline{\text{SDWE}}$ / $\overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$ respectively, during SBSRAM accesses.

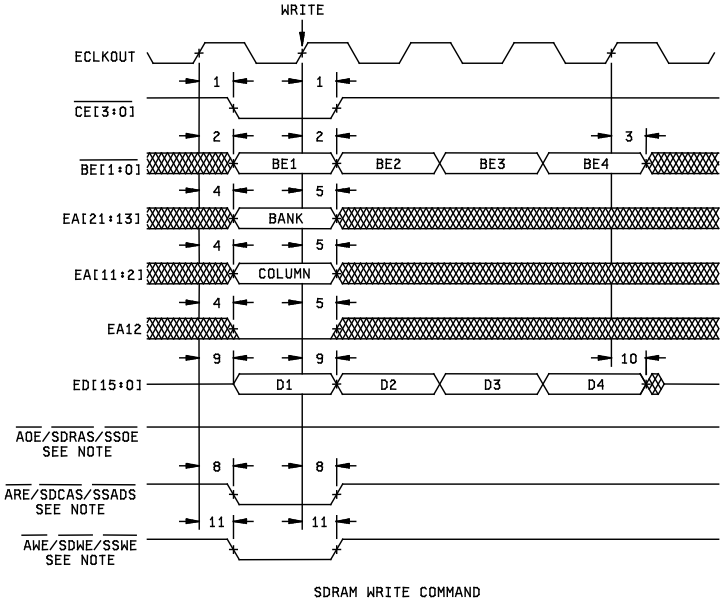
FIGURE 13 Timing waveforms.



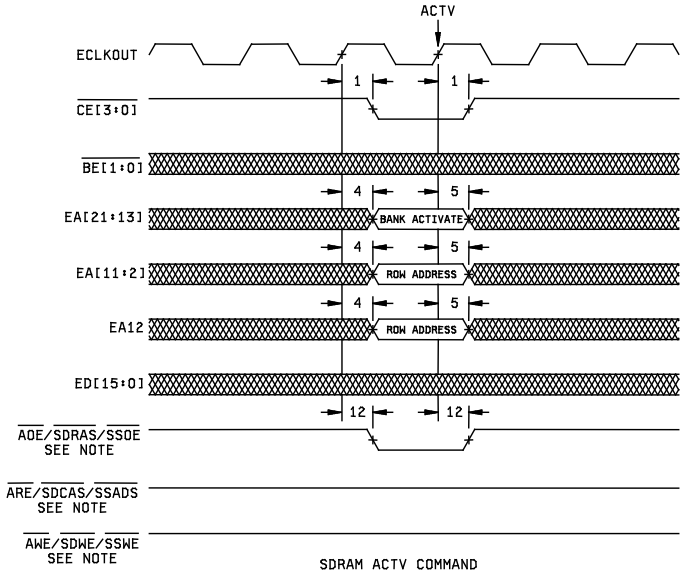
Note:

$\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$, and $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$ operate as $\overline{SDCAS}$, $\overline{SDWE}$, and $\overline{SDRAS}$ respectively, during SDRAM accesses.

FIGURE 14 Timing waveforms.



SDRAM WRITE COMMAND

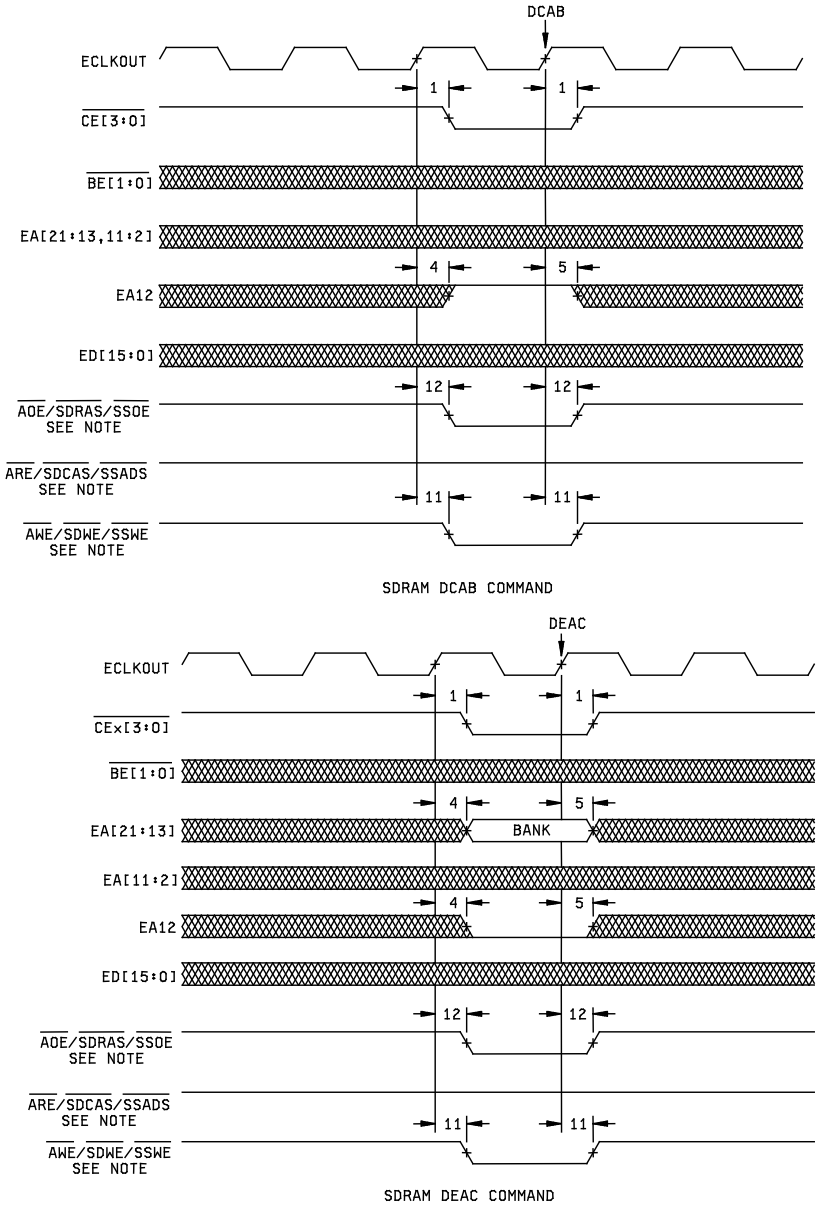


SDRAM ACTV COMMAND

Note:

$\overline{\text{ARE}}$ / $\overline{\text{SDCAS}}$ / $\overline{\text{SSADS}}$, $\overline{\text{AWE}}$ / $\overline{\text{SDWE}}$ / $\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$ / $\overline{\text{SDRAS}}$ / $\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$ respectively, during SDRAM accesses.

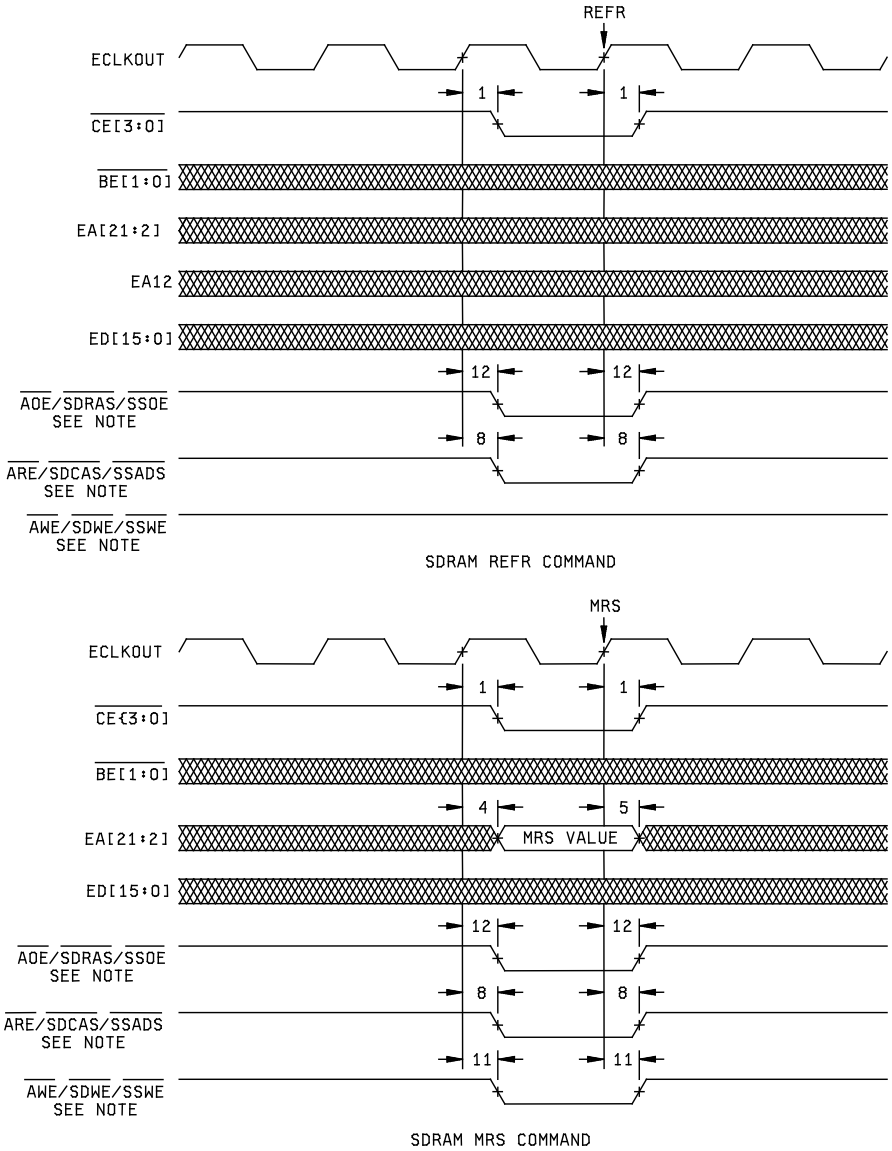
FIGURE 15 Timing waveforms.



Note:

$\overline{\text{ARE}}$ / $\overline{\text{SDCAS}}$ / $\overline{\text{SSADS}}$, $\overline{\text{AWE}}$ / $\overline{\text{SDWE}}$ / $\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$ / $\overline{\text{SDRAS}}$ / $\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$ respectively, during SDRAM accesses.

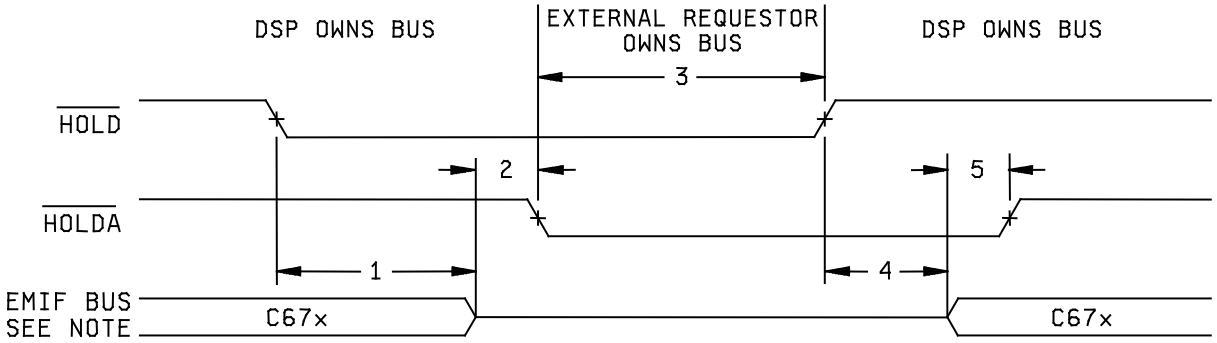
FIGURE 16 Timing waveforms.



Note:

$\overline{\text{ARE}}$ / $\overline{\text{SDCAS}}$ / $\overline{\text{SSADS}}$, $\overline{\text{AWE}}$ / $\overline{\text{SDWE}}$ / $\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$ / $\overline{\text{SDRAS}}$ / $\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$ respectively, during SDRAM accesses.

FIGURE 17 Timing waveforms.

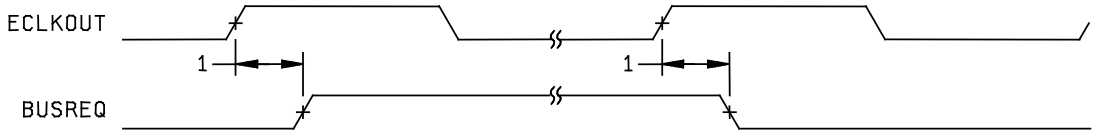


HOLD/HOLDA TIMING

Note:

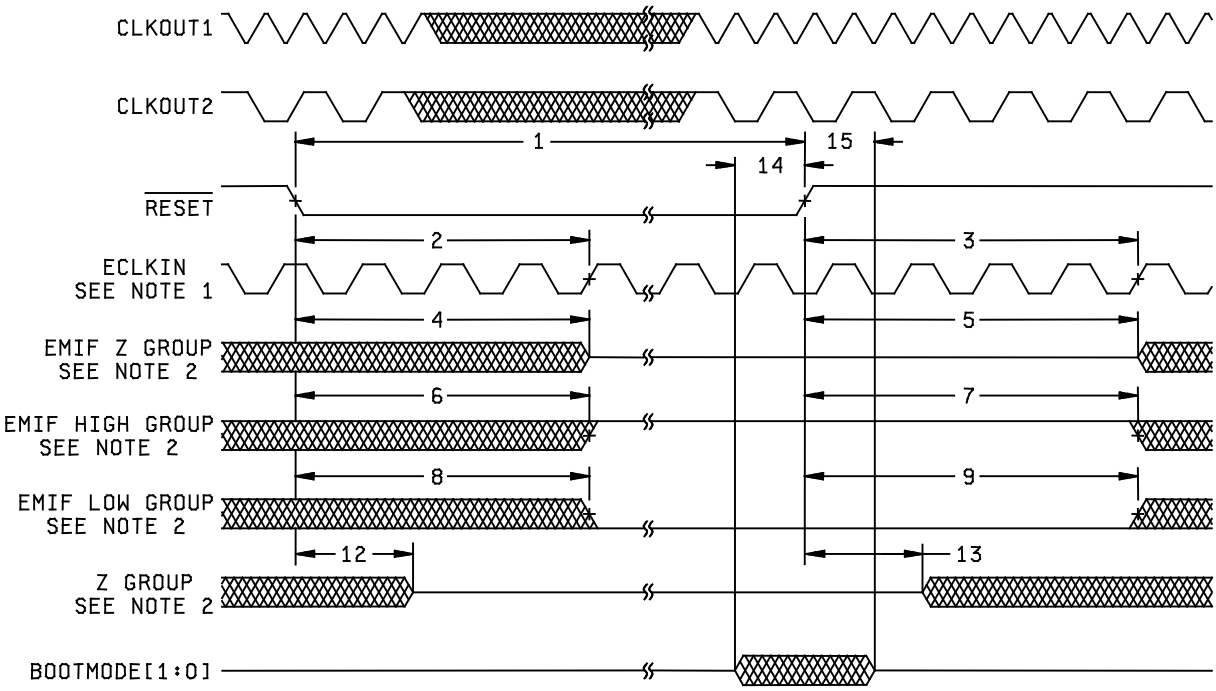
EMIF bus consists of $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, ED[31:0], EA[21:2], $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$, and $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$.

FIGURE 18 Timing waveforms.



BUSREQ TIMING

FIGURE 19 Timing waveforms.



RESET TIMING[C6712]

Notes:

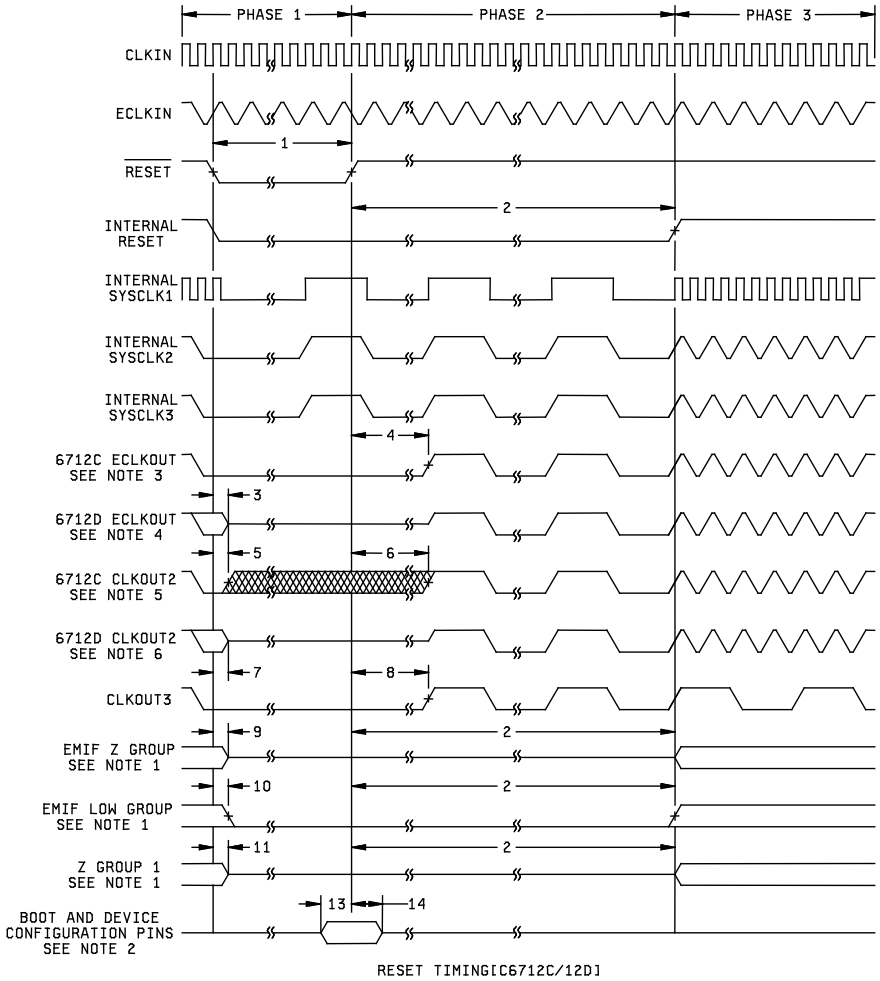
1. ECLKIN should be provided during reset in order to drive EMIF signals to the correct reset values. ECKLOUT continues to clock as long as ECLKIN is provided
2. EMIF Z group consists of: EA[21:2], ED[15:0], $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$, and $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$

   EMIF high group consists of: $\overline{HOLDA}$

   EMIF low group consists of: BUSREQ

   Z group consists of: HD[15:0], CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, TOUT0, and TOUT1.

FIGURE 20 Timing waveforms.



RESET TIMING[C6712C/12D]

Notes:

1. EMIF Z group consists of: EA[21:2], ED[31:0], $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, $\overline{ARE}$ / $\overline{SDCAS}$ / $\overline{SSADS}$, $\overline{AWE}$ / $\overline{SDWE}$ / $\overline{SSWE}$, $\overline{AOE}$ / $\overline{SDRAS}$ / $\overline{SSOE}$, and $\overline{HOLDA}$

   EMIF low group consists of: BUSREQ

   High group consists of: $\overline{HRDY}$ and $\overline{HINT}$

   Z group consists of: CLKR0, CLKR1, CLKX0, CLKX1, FSR0, FSR1, FSX0, FSX1, DX0, DX1, TOUT0, and TOUT1.
2. Boot and device configurations consist of: BOOTMODE[1:0] and LENDIAN.

FIGURE 21 Timing waveforms.

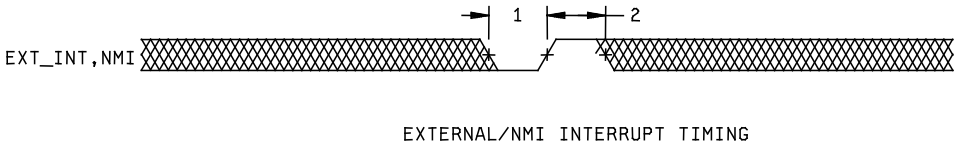


FIGURE 22 Timing waveforms.

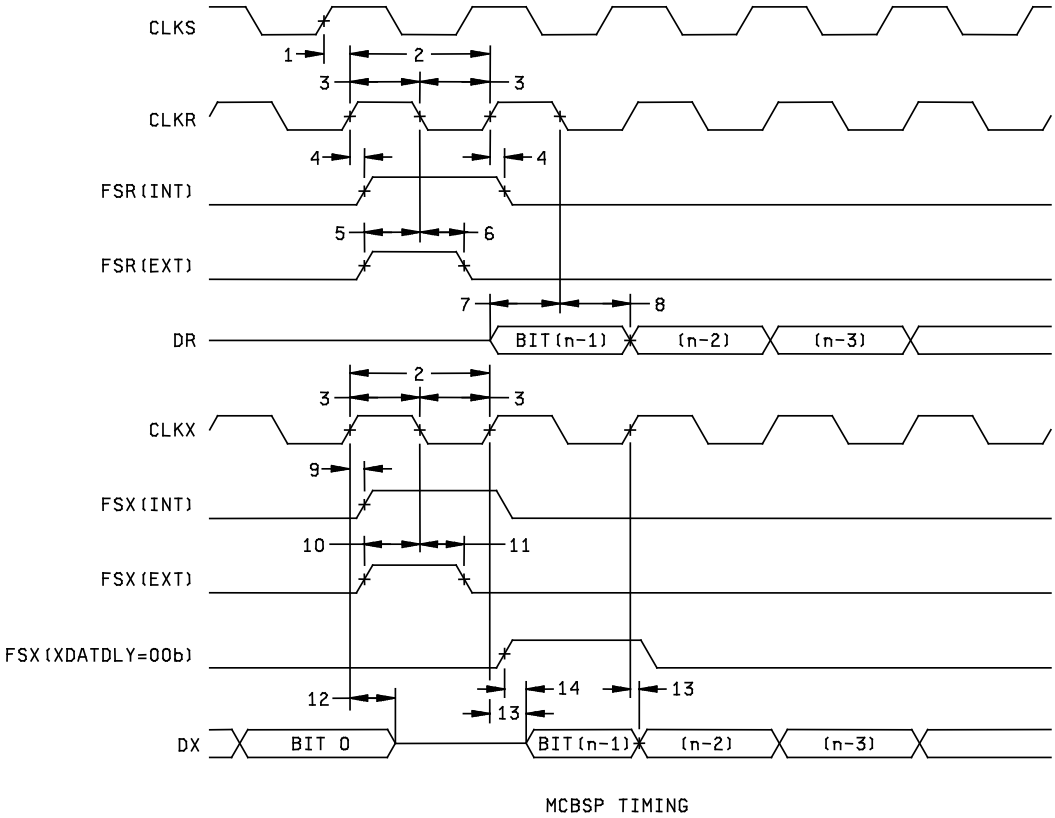


FIGURE 23 Timing waveforms.

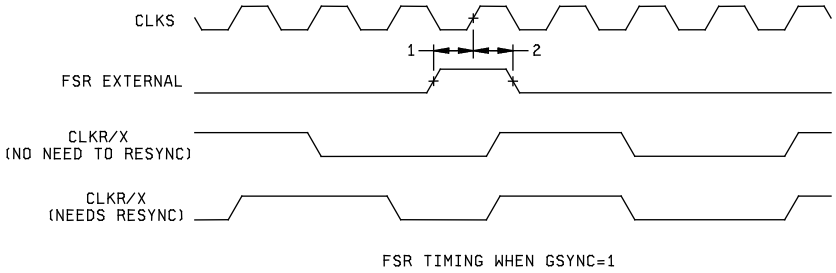


FIGURE 24 Timing waveforms.

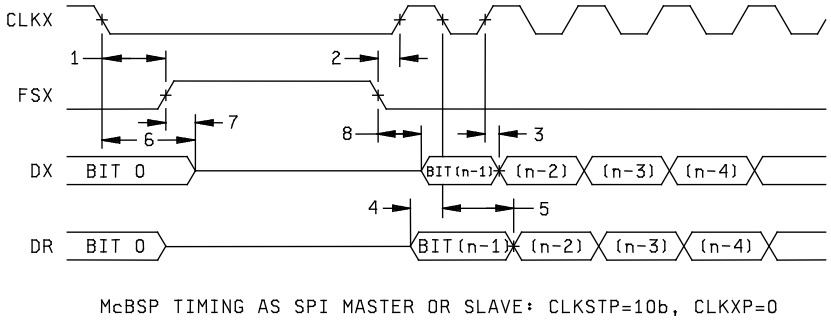


FIGURE 25. Timing waveforms.

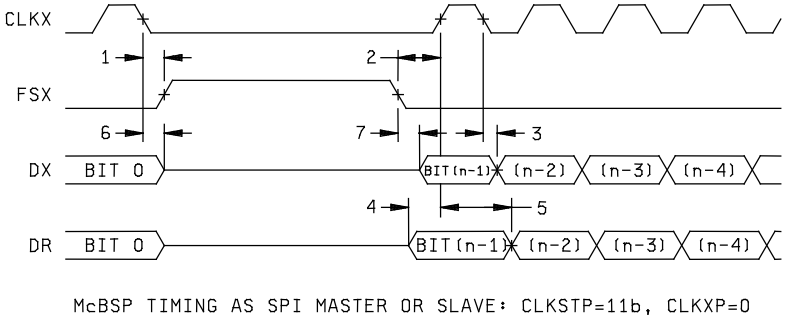
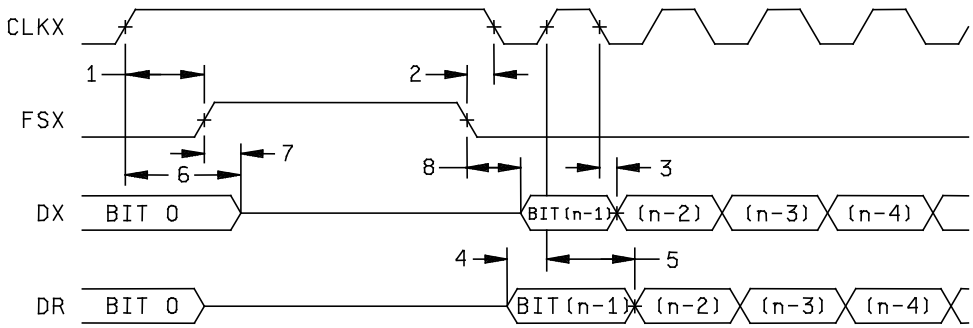
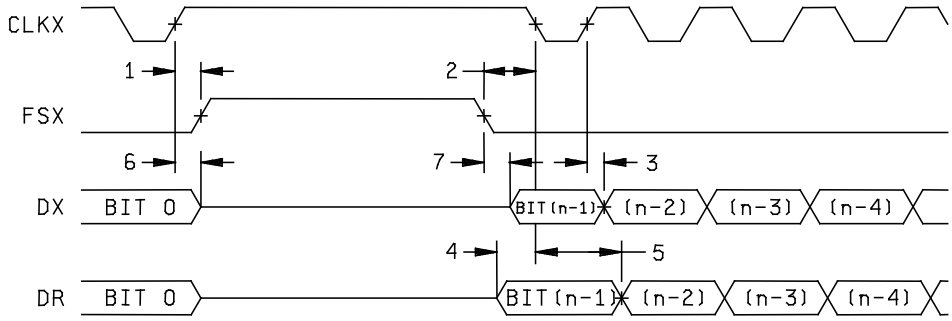


FIGURE 26. Timing waveforms.



McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=10b, CLKXP=1

FIGURE 27. Timing waveforms.



McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=11b, CLKXP=1

FIGURE 28. Timing waveforms.

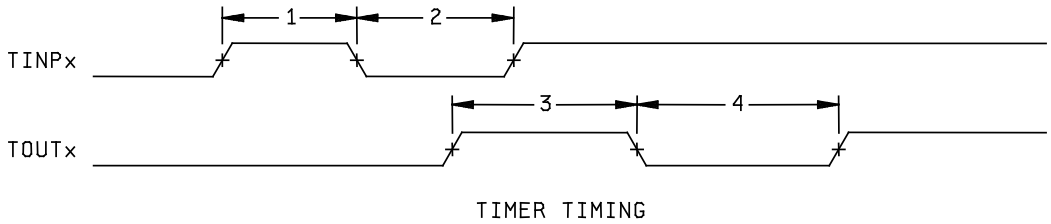


FIGURE 29. Timing waveforms.

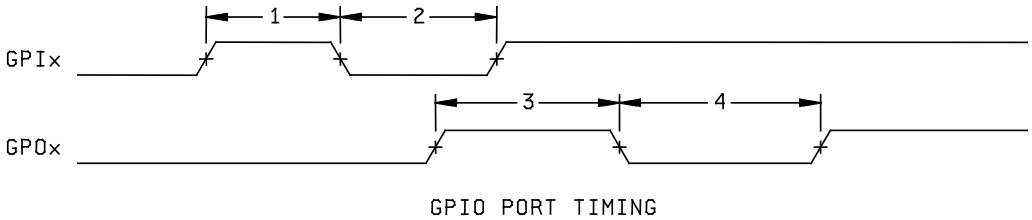


FIGURE 30. Timing waveforms.

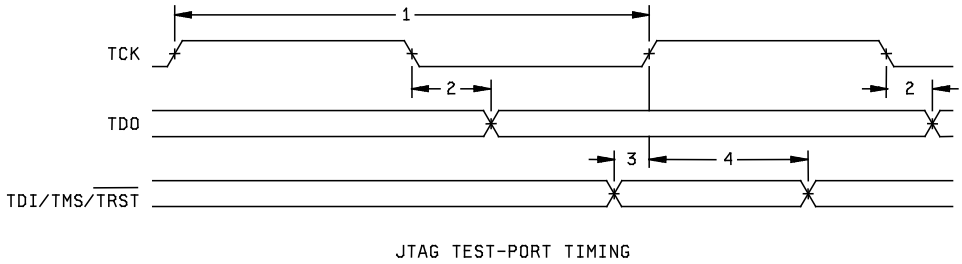


FIGURE 31. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/04754-01XE	01295	2/
V62/04754-02YE	01295	2/
V62/04754-03YA	01295	SM320C6712DGPA16EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not yet available from a source of supplied.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493