

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct lead finish for device 04. Update boilerplate. - CFS	05-12-02	Thomas M. Hess
B	Add device types 05-20. Editorial chances throughout. - PHN	06-01-11	Thomas M. Hess
C	Update boilerplate paragraphs to current requirements. - PHN	13-09-12	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

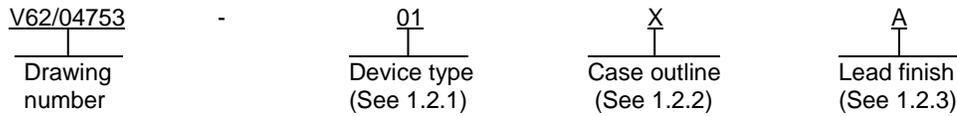
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PMIC N/A		PREPARED BY Phu H. Nguyen					DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990											
Original date of drawing YY MM DD 04-12-08		CHECKED BY Phu H. Nguyen					TITLE MICROCIRCUIT, DIGITAL, FLOATING POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON											
		APPROVED BY Thomas M. Hess																
		SIZE A	CODE IDENT. NO. 16236					DWG NO. V62/04753										
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Floating-Point Digital Signal Processor microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SM320C6711-16EP	Floating Point Digital Signal Processor
02	SM320C6711B-16EP	Floating Point Digital Signal Processor
03	SM320C6711C-16EP	Floating Point Digital Signal Processor
04	SM320C6711D-16EP	Floating Point Digital Signal Processor
05	SM320C6711-10EP	Floating Point Digital Signal Processor
06	SM320C6711B-10EP	Floating Point Digital Signal Processor
07	SM320C6711C-10EP	Floating Point Digital Signal Processor
08	SM320C6711D-10EP	Floating Point Digital Signal Processor
09	SM320C6711-15EP	Floating Point Digital Signal Processor
10	SM320C6711B-15EP	Floating Point Digital Signal Processor
11	SM320C6711C-15EP	Floating Point Digital Signal Processor
12	SM320C6711D-15EP	Floating Point Digital Signal Processor
13	SM320C6711-20EP	Floating Point Digital Signal Processor
14	SM320C6711B-20EP	Floating Point Digital Signal Processor
15	SM320C6711C-20EP	Floating Point Digital Signal Processor
16	SM320C6711D-20EP	Floating Point Digital Signal Processor
17	SM320C6711-25EP	Floating Point Digital Signal Processor
18	SM320C6711B-25EP	Floating Point Digital Signal Processor
19	SM320C6711C-25EP	Floating Point Digital Signal Processor
20	SM320C6711D-25EP	Floating Point Digital Signal Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>Package style</u>
X	256	Plastic ball grid array
Y	272	Plastic ball grid array

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

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1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 2/

Supply voltage ranges, (CV _{DD}): 3/	
Device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20 only	-0.3 V to +1.8 V
Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18	-0.3 V to +2.3 V
Supply voltage ranges, (DV _{DD})	-0.3 V to +4.0 V 3/
Input voltage ranges: (V _I):	
Device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20 only	-0.3 V to DV _{DD} + 0.5 V
Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18	-0.3 V to +4.0 V
Output voltage ranges: (V _O)	
Device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20 only	-0.3 V to DV _{DD} + 0.5 V
Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18	-0.3 V to +4.0 V
Operating case temperature ranges, (T _C):	
(default)	0°C to +90°C
(A version): Case outline X, device type 02, 06, 10, 14, and 18	-40°C to +105°C
Case outline Y, device type 03, 07, 11, 15, and 19	-40°C to +105°C
Storage temperature range, (T _{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 4/

		Min	Max	Unit
Supply voltage, Core (CV _{DD})	Device type 20 only	1.33	1.47	V
	Device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20 only	1.14 5/	1.32	
	Device type 02, 05, 06, 10, 14, and 18	1.71	1.89	
	Device type 09 only	1.80	2.00	
Supply voltage, I/O (DV _{DD})	Device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20	3.13	3.47	V
	Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18	3.14	3.46	

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/ All voltage values are with respect to V_{SS}.

4/ For device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O supply. For device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20, the core supply should be powered up prior to (and powered down after), the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.

5/ These values are compatible with existing 1.26 V designs.

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1.4 Recommended operating conditions - Continued.

			Min	Max	Unit
Supply ground, (V _{SS})			0	0	V
High level input voltage, (V _{IH})	Device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20 only	All signals except CLKS1, DR1, $\overline{\text{RESET}}$	2		V
		CLKS1, DR1, $\overline{\text{RESET}}$	2		
	Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18		2		
Low level input voltage, (V _{IL})	Device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20 only	All signals except CLKS1, DR1, $\overline{\text{RESET}}$		0.8	V
		CLKS1, DR1, $\overline{\text{RESET}}$		0.3*DV _{DD}	
	Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18			0.8	
High level output current, (I _{OH})	Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18	All signals except CLKOUT1, CLKOUT2, and ECLKOUT		-4	mA
		CLKOUT1, CLKOUT2, and ECLKOUT		-8	
	Device type 03, 07, 11, 15, 19 <u>6/</u>	All signals except ECKLOUT, CLKOUT2, CLKOUT3, CLKS1, and DR1		-8	mA
		ECKLOUT, CLKOUT2, and CLKOUT3		-16	
	Device type 04, 08, 12, 16, 20 <u>5/</u>	All signals except ECKLOUT, CLKOUT2, CLKS1, and DR1		-8	mA
		ECKLOUT, and CLKOUT2		-16	
Low level output current, (I _{OL})	Device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18	All signals except CLKOUT1, CLKOUT2, and ECLKOUT		4	mA
		CLKOUT1, CLKOUT2, and ECLKOUT		8	
	Device type 03, 07, 11, 15, 19 <u>5/</u>	All signals except ECKLOUT, CLKOUT2, CLKOUT3, CLKS1, and DR1		8	mA
		ECKLOUT, CLKOUT2, CLKOUT3		16	
		CLKS1 and DR1		3	
	Device type 04, 08, 12, 16, 20 <u>5/</u>	All signals except ECKLOUT, CLKOUT2, CLKS1, and DR1		8	mA
		ECKLOUT and CLKOUT2		16	
		CLKS1 and DR1		3	
	Operating temperature, (T _C)	Default		0	90
A version—Case outline X and Y		-40	105		
I version		-40	80		

6/ Refers to DC (or steady state) currents only, actual switching currents are higher. For more details, see manufacturer data device specific IBIS models.

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1.4 Recommended operating conditions - Continued.

Thermal resistance characteristics for case X (device type 01, 02, 05, 06, 09, 10, 13, 14, 17 and 18 only)

	Air Flow (m/s) <u>z</u> /	°C/W
Junction to case, (R _{θJC})	N/A	6.4
Junction to free air, (R _{θJA})	0.0	25.5
Junction to free air, (R _{θJA})	0.5	23.1
Junction to free air, (R _{θJA})	1.0	22.3
Junction to free air, (R _{θJA})	2.0	21.2

Thermal resistance characteristics for case Y (device type 03, 04, 07, 08, 11, 12, 15, 16, 19 and 20 only)

	Air Flow (m/s) <u>z</u> /	°C/W
Junction to case, (R _{θJC})	N/A	9.7
Junction to package top (P _{siJT})	0.0	1.5
Junction to board, (R _{θJB})	N/A	19
Junction to free air, (R _{θJA})	0.0	22
Junction to free air, (R _{θJA})	0.5	21
Junction to free air, (R _{θJA})	1.0	20
Junction to free air, (R _{θJA})	2.0	19
Junction to free air, (R _{θJA})	4.0	18
Junction to board, (P _{siJB})	0.0	16

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

z/ m/s = meters per second.

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3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 Test load circuits. The test load circuits shall be as specified in figure 4.

3.5.5 Board level input/output timings. The board level input/output timings shall be as specified in figure 5.

3.5.6 Timing waveforms. The timing waveforms shall be as shown in figure 6-36.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test condition 2/		Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	All signals	DV _{DD} = min, I _{OH} = max	3/ 4/	2.4		V
		All signals except CLKS1 and DR1		5/ 6/	2.4		
Low level output voltage	V _{OL}	All signals	DV _{DD} = min, I _{OL} = max	3/ 4/		0.4	V
		All signals except CLKS1 and DR1		5/ 6/		0.4	
		CLKS1 and DR1		5/ 6/		0.4	
Input current	I _i	All signals	V _i = V _{SS} to DV _{DD}	3/ 4/		±150	μA
		All signals except CLKS1 and DR1		5/ 6/		±170	
		CLKS1 and DR1		5/ 6/		±10	
Off state output current	I _{oz}	All signals	V _o = DV _{DD} or 0 V	3/ 4/		±10	μA
		All signals except CLKS1 and DR1		5/ 6/		±170	
		CLKS1 and DR1		5/ 6/		±10	
Core supply current 7/	I _{DD2V}	CV _{DD} = 1.40 V, CPU clock = 250 MHz		6/	810 Typ		mA
		CV _{DD} = 1.26 V, CPU clock = 200 MHz		5/	560 Typ		
		CV _{DD} = 1.26 V, CPU clock = 200 MHz		6/	560 Typ		
		CV _{DD} = 1.26 V, CPU clock = 167 MHz		5/	475 Typ		
		CV _{DD} = 1.26 V, CPU clock = 167 MHz		6/	475 Typ		
I/O supply current 7/	I _{DD3V}	DV _{DD} = 3.3 V, EMIF speed = 100 MHz		5/ 6/	75 Typ		mA
Supply current, CPU + CPU memory access 8/	I _{DD2V}	CV _{DD} = NOM, CPU clock = 150 MHz		3/	433 Typ		mA
				4/	410 Typ		
Supply current, peripherals 8/	I _{DD2V}			3/	232 Typ		
				4/	220 Typ		
Supply current, I/O pins 8/	I _{DD3V}	DV _{DD} = NOM, CPU clock = 150 MHz		3/	60 Typ		mA
				4/	60 Typ		
Input capacitance	C _i			All		7	pF
Output capacitance	C _o			All		7	pF

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Limits		Limits		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
INPUT AND OUTPUT CLOCKS												
Timing requirements for CLKIN 10/ 11/				Device type 05, 06				Device type 09, 10				
				CLKMODE = x4		CLKMODE = x1		CLKMODE = x4		CLKMODE = x1		
1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	40		10		26.7		6.7		ns
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.45C		0.4C		0.45C		
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.45C		0.4C		0.45C		
4	Transaction time, CLKIN	$t_t(CLKIN)$			5		1		5		1	
Timing requirements for CLKIN 10/ 11/ 12/				Device type (03, 04)K ₂ 9/				Device type 15, 16				
				PLL MODE (PLEN = 1)		BYPASS MODE (PLEN = 0)		PLL MODE (PLEN = 1)		BYPASS MODE (PLEN = 0)		
1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6	6	83.3	6		5	83.3	5		ns
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$		0.4C		0.4C		0.4C		0.4C		
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$		0.4C		0.4C		0.4C		0.4C		
4	Transaction time, CLKIN	$t_t(CLKIN)$			5		5		5		5	
Timing requirements for CLKIN 10/ 11/ 12/								Device type 20				
								PLL MODE (PLEN = 1)		BYPASS MODE (PLEN = 0)		
1	Cycle time, CLKIN	$t_{c(CLKIN)}$	See figure 6					4	83.3	4		ns
2	Pulse duration, CLKIN high	$t_{w(CLKINH)}$						0.4C		0.4C		
3	Pulse duration, CLKIN low	$t_{w(CLKINL)}$						0.4C		0.4C		
4	Transaction time, CLKIN	$t_t(CLKIN)$							5		5	

See notes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit
				Min	Max	Min	Max	
INPUT AND OUTPUT CLOCKS (Continued)								
Switching characteristics for CLKOUT1 <u>13/ 14/ 15/</u>				Device type 05, 06, 09, 10				
				CLKMODE = x4		CLKMODE = x4		
1	Cycle time, CLKOUT1	$t_{c(CKO1)}$	See figure 7	P-0.7	P+0.7	P-0.7	P+0.7	ns
2	Pulse duration, CLKOUT1 high	$t_{w(CKO1H)}$		(P/2)-0.7	(P/2)+0.7	PH-0.7	PH+0.7	
3	Pulse duration, CLKOUT1 low	$t_{w(CKO1L)}$		(P/2)-0.7	(P/2)+0.7	PH-0.7	PH+0.7	
4	Transition time, CLKOUT1	$t_{t(CKO1)}$			2		2	
Switching characteristics for CLKOUT2 <u>13/ 14/</u>						Device type 05, 06, 09, 10		
1	Cycle time, CLKOUT2	$t_{c(CKO2)}$	See figure 8	2P-0.7	2P+0.7			ns
2	Pulse duration, CLKOUT2 high	$t_{w(CKO2H)}$		P-0.7	P+0.7			
3	Pulse duration, CLKOUT2 low	$t_{w(CKO2L)}$		P-0.7	P+0.7			
4	Transition time, CLKOUT2	$t_{t(CKO2)}$			2			
Switching characteristics for CLKOUT2 <u>13/ 16/</u>						Device type (03, 04)K ₂ , 15, 16 and 20 <u>9/</u>		
1	Cycle time, CLKOUT2	$t_{c(CKO2)}$	See figure 9	C2-0.8	C2+0.8			ns
2	Pulse duration, CLKOUT2 high	$t_{w(CKO2H)}$		(C2/2)-0.8	(C2/2)+0.8			
3	Pulse duration, CLKOUT2 low	$t_{w(CKO2L)}$		(C2/2)-0.8	(C2/2)+0.8			
4	Transition time, CLKOUT2	$t_{t(CKO2)}$			2			
Switching characteristics for CLKOUT3 <u>13/ 17/</u>				Device type (03)K ₂ , and 15 <u>9/</u>		Device type (04)K ₂ , 16, and 20 <u>9/</u>		
1	Cycle time, CLKOUT3	$t_{c(CKO3)}$		C3-0.6	C3+0.6	C3-0.9	C3+0.9	ns
2	Pulse duration, CLKOUT3 high	$t_{w(CKO3H)}$		(C3/2)-0.6	(C3/2)+0.6	(C3/2)-0.9	(C3/2)+0.9	
3	Pulse duration, CLKOUT3 low	$t_{w(CKO3L)}$		(C3/2)-0.6	(C3/2)+0.6	(C3/2)-0.9	(C3/2)+0.9	
4	Transition time, CLKOUT3	$t_{t(CKO3)}$			2		3	
5	Delay time, CLKIN high to CLKOUT3 valid	$t_{d(CKINH-CKO3V)}$		1.5	6.5	1.5	7.5	

See notes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Limits		Unit
				Min	Max	Min	Max	Min	Max	

INPUT AND OUTPUT CLOCKS (Continued)

Timing requirements for ECLKIN 10/				Device type 05-08		Device type 09-12		Device type (01-04)K ₂ , 13-16, and 20 9/		ns
1	Cycle time, ECLKIN	t _c (EKL)	See figure 11	15		10		10		
2	Pulse duration, ECLKIN high	t _w (ECLKIH)		6.8		4.5		4.5		
3	Pulse duration, ECLKIN low	t _w (ECLKIL)		6.8		4.5		4.5		
4	Transaction time, ECLKIN	t _t (EKL)			2.2		2.2		3.0	

Switching characteristics for ECLKOUT 13/ 18/ 19/				Device type 05-12		Device type (01-04)K ₂ , 13-16, and 20 9/		ns
1	Cycle time, CLKOUT	t _c (EKO)	See figure 12	E-0.7	E+0.7	E-0.9	E+0.9	
2	Pulse duration, ECLKOUT high	t _w (ECKOH)		EH-0.7	EH+0.7	EH-0.9	EH+0.9	
3	Pulse duration, ECLKOUT low	t _w (ECKOL)		EL-0.7	EL+0.7	EL-0.9	EL+0.9	
4	Transition time, ECLKOUT	t _t (EKO)			2		2	
5	Delay time, ECLKIN high to ECLKOUT high	t _d (EKIH-EKOH)		1	7	1	6.5	
6	Delay time, ECLKIN low to ECLKOUT low	t _d (EKIL-EKOL)		1	7	1	6.5	

ASYNCHRONOUS MEMORY TIMING

Timing requirements for asynchronous memory cycles 20/ 21/ 22/				Device type 05		Device type 09		ns
3	Setup time, EDx valid before ARE high	t _{su} (EDV-AREH)	See figure 13	13		9		
4	Hold time, EDx valid after ARE high	t _h (AREH-EDV)		1		1		
6	Setup time, ARDY valid before ECLKOUT high	t _{su} (ARDY-EKOH)		6		3		
7	Hold time, ARDY valid after ECLKOUT high	t _h (EKOH-ARDY)		1.7		1.7		

Timing requirements for asynchronous memory cycles 20/ 21/ 22/				Device type 06, (06)K ₁ 9/		Device type 10		ns
3	Setup time, EDx valid before ARE high	t _{su} (EDV-AREH)	See figure 13	13		9		
4	Hold time, EDx valid after ARE high	t _h (AREH-EDV)		1		1		
6	Setup time, ARDY valid before ECLKOUT high	t _{su} (ARDY-EKOH)		6		3		
7	Hold time, ARDY valid after ECLKOUT high	t _h (EKOH-ARDY)		2.5		2.5		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit	
				Min	Max	Min	Max		
ASYNCHRONOUS MEMORY TIMING - Continued									
Timing requirements for asynchronous memory cycles 20/ 21/ 22/							Device type (03,04)K ₂ 15, 16, and 20 9/		
3	Setup time, EDx valid before $\overline{\text{ARE}}$ high	$t_{su}(\text{EDV-AREH})$	See figure 13			6.5		ns	
4	Hold time, EDx valid after $\overline{\text{ARE}}$ high	$t_h(\text{AREH-EDV})$				1			
6	Setup time, ARDY valid before ECLKOUT high	$t_{su}(\text{ARDY-EKOH})$				3			
7	Hold time, ARDY valid after ECLKOUT high	$t_h(\text{EKOH-ARDY})$				2.3			
Switching characteristics for asynchronous memory cycles 21/ 22/ 23/				Device type 05		Device type 09			
1	Output setup time, select signals valid to $\overline{\text{ARE}}$ low	$t_{osu}(\text{SELV-AREL})$	See figure 13	RS*E-3		RS*E-3		ns	
2	Output hold time, $\overline{\text{ARE}}$ high to select signals invalid	$t_{oh}(\text{AREH-SELIV})$		RH*E-3		RH*E-3			
5	Delay time, ECKLOUT high to $\overline{\text{ARE}}$ valid	$t_d(\text{EKOH-AREV})$		1.5	11	1.5	8		
8	Output setup time, select signals valid to $\overline{\text{AWE}}$ low	$t_{osu}(\text{SELV-AWEL})$		WS*E-3		WS*E-3			
9	Output hold time, $\overline{\text{AWE}}$ high to select signals invalid	$t_{oh}(\text{AWEH-SELIV})$		WH*E-3		WH*E-3			
10	Delay time, ECLKOUT high to $\overline{\text{AWE}}$ valid	$t_d(\text{EKOH-AWEV})$		1.5	11	1.5	8		
Switching characteristics for asynchronous memory cycles 21/ 22/ 23/				Device type 06		Device type 10			
1	Output setup time, select signals valid to $\overline{\text{ARE}}$ low	$t_{osu}(\text{SELV-AREL})$	See figure 13	RS*E-3		RS*E-3		ns	
2	Output hold time, $\overline{\text{ARE}}$ high to select signals invalid	$t_{oh}(\text{AREH-SELIV})$		RH*E-3		RH*E-3			
5	Delay time, ECKLOUT high to $\overline{\text{ARE}}$ valid	$t_d(\text{EKOH-AREV})$		1	11	1	8		
8	Output setup time, select signals valid to $\overline{\text{AWE}}$ low	$t_{osu}(\text{SELV-AWEL})$		WS*E-3		WS*E-3			
9	Output hold time, $\overline{\text{AWE}}$ high to select signals invalid	$t_{oh}(\text{AWEH-SELIV})$		WH*E-3		WH*E-3			
10	Delay time, ECLKOUT high to $\overline{\text{AWE}}$ valid	$t_d(\text{EKOH-AWEV})$		1	11	1	8		
Switching characteristics for asynchronous memory cycles 21/ 22/ 23/							Device type (03,04)K ₂ 15, 16, and 20 9/		
1	Output setup time, select signals valid to $\overline{\text{ARE}}$ low	$t_{osu}(\text{SELV-AREL})$	See figure 13			RS*E-1.7		ns	
2	Output hold time, $\overline{\text{ARE}}$ high to select signals invalid	$t_{oh}(\text{AREH-SELIV})$				RH*E-1.7			
5	Delay time, ECKLOUT high to $\overline{\text{ARE}}$ valid	$t_d(\text{EKOH-AREV})$				1.5	7		
8	Output setup time, select signals valid to $\overline{\text{AWE}}$ low	$t_{osu}(\text{SELV-AWEL})$				WS*E-1.7			
9	Output hold time, $\overline{\text{AWE}}$ high to select signals invalid	$t_{oh}(\text{AWEH-SELIV})$				WH*E-1.7			
10	Delay time, ECLKOUT high to $\overline{\text{AWE}}$ valid	$t_d(\text{EKOH-AWEV})$				1.5	7		
11	Output setup time, ED valid to $\overline{\text{AWE}}$ low	$t_{osu}(\text{EDV-AWEL})$			(WS-1)*E-1.7				

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit
				Min	Max	Min	Max	
SYNCHRONOUS BURST MEMORY TIMING								
Timing requirements for synchronous burst SRAM cycles <u>24/</u>				Device type 05		Device type 09		
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 14	6		2.5		ns
7	Hold time, read EDx valid after ECLKOUT high <u>24/</u>	$t_{h(EKOH-EDV)}$		2.1		2.1		
Timing requirements for synchronous burst SRAM cycles <u>24/</u>				Device type 06		Device type (06)K ₁ , 10 <u>9/</u>		
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 14	6		2.5		ns
7	Hold time, read EDx valid after ECLKOUT high	$t_{h(EKOH-EDV)}$		2.5		2.5		
Timing requirements for synchronous burst SRAM cycles <u>24/</u>								
Device type (03, 04)K ₂ , 15,16, and 20 <u>9/</u>								
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 14			1.5		ns
7	Hold time, read EDx valid after ECLKOUT high	$t_{h(EKOH-EDV)}$				2.5		
Switching characteristics for synchronous burst SRAM cycles <u>24/</u> <u>25/</u>				-Device type 05		Device type 09		
1	Delay time, ECKLOUT high to \overline{CEx} valid	$t_{d(EKOH-CEV)}$		1.5	11	1.5	6.9 <u>25/</u>	ns
2	Delay time, ECKLOUT high to \overline{BEx} valid	$t_{d(EKOH-BEV)}$			11		6.9 <u>25/</u>	
3	Delay time, ECKLOUT high to \overline{BEx} invalid	$t_{d(EKOH-BEIV)}$		1.5		1.5		
4	Delay time, ECKLOUT high to EAx valid	$t_{d(EKOH-EAV)}$			11		6.9 <u>25/</u>	
5	Delay time, ECKLOUT high to EAx invalid	$t_{d(EKOH-EAIV)}$		1.5		1.5		
8	Delay time, ECKLOUT high to \overline{ARE} / \overline{SDCAS} / \overline{SSADS} valid	$t_{d(EKOH-ADSV)}$		1.5	11	1.5	6.9 <u>25/</u>	
9	Delay time, ECKLOUT high to \overline{AOE} / \overline{SDRAS} / \overline{SSOE} valid	$t_{d(EKOH-OEV)}$		1.5	11	1.5	6.9 <u>25/</u>	
10	Delay time, ECKLOUT high to \overline{EDx} valid	$t_{d(EKOH-EDV)}$			11		7.1 <u>25/</u>	
11	Delay time, ECKLOUT high to \overline{EDx} invalid	$t_{d(EKOH-EDIV)}$		1.5		1.5		
12	Delay time, ECKLOUT high to \overline{AWE} / \overline{SDWE} / \overline{SSWE} valid	$t_{d(EKOH-WEV)}$		1.5	11	1.5	6.9 <u>25/</u>	

See notes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Limits		Unit
				Min	Max	Min	Max	Min	Max	

SYNCHRONOUS BURST MEMORY TIMING – Continued

Switching characteristics for synchronous burst SRAM cycles 24/ 25/				Device type 06		Device type (06)K ₁ 9/		Device type 10		
1	Delay time, ECKLOUT high to \overline{CEx} valid	$t_{d(EKOH-CEV)}$	See figure 14 and 15	1	11	1	8.5	1	7.5	ns
2	Delay time, ECKLOUT high to \overline{BEx} valid	$t_{d(EKOH-BEV)}$			11		8.5		7.5	
3	Delay time, ECKLOUT high to \overline{BEx} invalid	$t_{d(EKOH-BEIV)}$		1		1		1		
4	Delay time, ECKLOUT high to EAx valid	$t_{d(EKOH-EAV)}$			11		8.5		7.5	
5	Delay time, ECKLOUT high to EAx invalid	$t_{d(EKOH-EAIV)}$		1		1		1		
8	Delay time, ECKLOUT high to \overline{ARE} / \overline{SDCAS} / \overline{SSADS} valid	$t_{d(EKOH-ADSV)}$		1	11	1	8.5	1	7.5	
9	Delay time, ECKLOUT high to \overline{AOE} / \overline{SDRAS} / \overline{SSOE} valid	$t_{d(EKOH-OEV)}$		1	11	1	8.5	1	7.5	
10	Delay time, ECKLOUT high to \overline{EDx} valid	$t_{d(EKOH-EDV)}$			11		8.5		7.5	
11	Delay time, ECKLOUT high to \overline{EDx} invalid	$t_{d(EKOH-EDIV)}$		1		1		1		
12	Delay time, ECKLOUT high to \overline{AWE} / \overline{SDWE} / \overline{SSWE} valid	$t_{d(EKOH-WEV)}$		1	11	1	8.5	1	7.5	

Switching characteristics for synchronous burst SRAM cycles 24/ 25/										
Device type (03, 04)K ₂ , 15, 16, and 20 9/										
1	Delay time, ECKLOUT high to \overline{CEx} valid	$t_{d(EKOH-CEV)}$	See figure 14 and 15			1.2	7			ns
2	Delay time, ECKLOUT high to \overline{BEx} valid	$t_{d(EKOH-BEV)}$					7			
3	Delay time, ECKLOUT high to \overline{BEx} invalid	$t_{d(EKOH-BEIV)}$				1.2				
4	Delay time, ECKLOUT high to EAx valid	$t_{d(EKOH-EAV)}$					7			
5	Delay time, ECKLOUT high to EAx invalid	$t_{d(EKOH-EAIV)}$				1.2				
8	Delay time, ECKLOUT high to \overline{ARE} / \overline{SDCAS} / \overline{SSADS} valid	$t_{d(EKOH-ADSV)}$				1.2	7			
9	Delay time, ECKLOUT high to \overline{AOE} / \overline{SDRAS} / \overline{SSOE} valid	$t_{d(EKOH-OEV)}$				1.2	7			
10	Delay time, ECKLOUT high to \overline{EDx} valid	$t_{d(EKOH-EDV)}$					7			
11	Delay time, ECKLOUT high to \overline{EDx} invalid	$t_{d(EKOH-EDIV)}$				1.2				
12	Delay time, ECKLOUT high to \overline{AWE} / \overline{SDWE} / \overline{SSWE} valid	$t_{d(EKOH-WEV)}$				1.2	7			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit	
				Min	Max	Min	Max		
SYNCHRONOUS DRAM TIMING									
Timing requirements for synchronous DRAM cycles 24/				Device type 05		Device type 09			
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 16	6		2.5		ns	
7	Hold time, read EDx valid after ECLKOUT high	$t_h(EKOH-EDV)$		2.1		2.1			
Timing requirements for synchronous DRAM cycles 24/				Device type 06		Device type (06)K ₁ , 10 9/			
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 16	6		2.5		ns	
7	Hold time, read EDx valid after ECLKOUT high	$t_h(EKOH-EDV)$		2.5		2.5			
Timing requirements for synchronous DRAM cycles 24/ Device type (03, 04)K ₂ , 15,16, and 20 9/									
6	Setup time, read EDx valid before ECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 16			1.5		ns	
7	Hold time, read EDx valid after ECLKOUT high	$t_h(EKOH-EDV)$				2.5			
Switching characteristics for synchronous DRAM cycles 24/ 27/				Device type 05		Device type 09			
1	Delay time, ECKLOUT high to \overline{CEx} valid	$t_d(EKOH-CEV)$	See figure 16-20	1.5	11	1.5	6.9	ns	
2	Delay time, ECKLOUT high to \overline{BEx} valid	$t_d(EKOH-BEV)$			11		6.9		
3	Delay time, ECKLOUT high to \overline{BEx} invalid	$t_d(EKOH-BEIV)$			1.5		1.5		
4	Delay time, ECKLOUT high to EAx valid	$t_d(EKOH-EAV)$				11			6.9
5	Delay time, ECKLOUT high to EAx invalid	$t_d(EKOH-EAIV)$			1.5		1.5		
8	Delay time, ECKLOUT high to \overline{ARE} / \overline{SDCAS} / \overline{SSADS} valid	$t_d(EKOH-CASV)$			1.5	11	1.5		6.9
9	Delay time, ECKLOUT high to \overline{EDx} valid	$t_d(EKOH-EDV)$				11			7.1
10	Delay time, ECKLOUT high to \overline{EDx} invalid	$t_d(EKOH-EDIV)$			1.5		1.5		
11	Delay time, ECKLOUT high to \overline{AWE} / \overline{SDWE} / \overline{SSWE} valid	$t_d(EKOH-WEV)$			1.5	11	1.5		6.9
12	Delay time, ECKLOUT high to \overline{AOE} / \overline{SDRAS} / \overline{SSOE} valid	$t_d(EKOH-RAS)$			1.5	11	1.5		6.9

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
SYNCHRONOUS DRAM TIMING - Continued								
Switching characteristics for synchronous DRAM cycles 24/ 27/				Device type 06		Device type (06)K1, 10 9/		
1	Delay time, ECKLOUT high to \overline{CEx} valid	$t_{d(EKOH-CEV)}$	See figure 16-20	1	11	1	8	ns
2	Delay time, ECKLOUT high to \overline{BEx} valid	$t_{d(EKOH-BEV)}$			11		8	
3	Delay time, ECKLOUT high to \overline{BEx} invalid	$t_{d(EKOH-BEIV)}$		1		1		
4	Delay time, ECKLOUT high to EAx valid	$t_{d(EKOH-EAV)}$			11		8	
5	Delay time, ECKLOUT high to EAx invalid	$t_{d(EKOH-EAIV)}$		1		1		
8	Delay time, ECKLOUT high to \overline{ARE} / \overline{SDCAS} / \overline{SSADS} valid	$t_{d(EKOH-CASV)}$		1	11	1	8	
9	Delay time, ECKLOUT high to \overline{EDx} valid	$t_{d(EKOH-EDV)}$			11		8	
10	Delay time, ECKLOUT high to \overline{EDx} invalid	$t_{d(EKOH-EDIV)}$		1		1		
11	Delay time, ECKLOUT high to \overline{AWE} / \overline{SDWE} / \overline{SSWE} valid	$t_{d(EKOH-WEV)}$		1	11	1	8	
12	Delay time, ECKLOUT high to \overline{AOE} / \overline{SDRAS} / \overline{SSOE} valid	$t_{d(EKOH-RAS)}$		1	11	1	8	

Switching characteristics for synchronous DRAM cycles 24/ 27/								
Device type (03, 04)K2, 15, 16, and 20 9/								
1	Delay time, ECKLOUT high to \overline{CEx} valid	$t_{d(EKOH-CEV)}$	See figure 16-20			1.5	7	ns
2	Delay time, ECKLOUT high to \overline{BEx} valid	$t_{d(EKOH-BEV)}$					7	
3	Delay time, ECKLOUT high to \overline{BEx} invalid	$t_{d(EKOH-BEIV)}$				1.5		
4	Delay time, ECKLOUT high to EAx valid	$t_{d(EKOH-EAV)}$					7	
5	Delay time, ECKLOUT high to EAx invalid	$t_{d(EKOH-EAIV)}$				1.5		
8	Delay time, ECKLOUT high to \overline{ARE} / \overline{SDCAS} / \overline{SSADS} valid	$t_{d(EKOH-CASV)}$				1.5	7	
9	Delay time, ECKLOUT high to \overline{EDx} valid	$t_{d(EKOH-EDV)}$					7	
10	Delay time, ECKLOUT high to \overline{EDx} invalid	$t_{d(EKOH-EDIV)}$				1.5		
11	Delay time, ECKLOUT high to \overline{AWE} / \overline{SDWE} / \overline{SSWE} valid	$t_{d(EKOH-WEV)}$				1.5	7	
12	Delay time, ECKLOUT high to \overline{AOE} / \overline{SDRAS} / \overline{SSOE} valid	$t_{d(EKOH-RAS)}$				1.5	7	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
HOLD/HOLDA TIMING								
Timing requirements for the $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ cycles 28/				Device type 05-08, 09-12		Device type 9/ (01-04)K ₂ , 13-16, and 20		
3	Hold time $\overline{\text{HOLD}}$ low after $\overline{\text{HOLDA}}$ low	$t_{h(\text{HOLDAL-HOLDL})}$	See figure 21	E		E		ns
Switching characteristics for the $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ cycles 28/ 29/						Device type 05, 06, 09, 10		
1	Delay time, $\overline{\text{HOLD}}$ low to EMIF bus high impedance	$t_{d(\text{HOLDL-EMHZ})}$	See figure 21			2E	25/	ns
2	Delay time, EMIF bus high impedance to $\overline{\text{HOLDA}}$ low	$t_{d(\text{EMHZ-HOLDAL})}$				0	2E	
4	Delay time, $\overline{\text{HOLD}}$ high to EMIF bus low impedance	$t_{d(\text{HOLDH-EMLZ})}$				2E	7E	
5	Delay time, EMIF bus low impedance to $\overline{\text{HOLDA}}$ high	$t_{d(\text{EMLZ-HOLDAH})}$				0	2E	
Switching characteristics for the $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ cycles 28/ 29/				Device type (03)K ₂ , 15 9/		Device type (04)K ₂ , 16, 20 9/		
1	Delay time, $\overline{\text{HOLD}}$ low to EMIF bus high impedance	$t_{d(\text{HOLDL-EMHZ})}$	See figure 21	2E	25/	2E	25/	ns
2	Delay time, EMIF bus high impedance to $\overline{\text{HOLDA}}$ low	$t_{d(\text{EMHZ-HOLDAL})}$		-0.1	2E	0	2E	
4	Delay time, $\overline{\text{HOLD}}$ high to EMIF bus low impedance	$t_{d(\text{HOLDH-EMLZ})}$		2E	7E	2E	7E	
5	Delay time, EMIF bus low impedance to $\overline{\text{HOLDA}}$ high	$t_{d(\text{EMLZ-HOLDAH})}$		-1.5	2E	0	2E	
BUSREQ TIMING								
Switching characteristics for the BUSREQ cycles				Device type 05, 06		Device type 09, 10		
1	Delay time, ECKLOUT high to BUSREQ valid	$t_{d(\text{EKOH-BUSRV})}$	See figure 22	2	11	1.5	11	ns
Switching characteristics for the BUSREQ cycles						Device type (03, 04)K ₂ , 15, 16, 20 9/		
1	Delay time, ECKLOUT high to BUSREQ valid	$t_{d(\text{EKOH-BUSRV})}$	See figure 22			1.5	7.2	ns

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Unit
				Min	Max	
RESET TIMING						
Timing requirements for reset <u>31/</u>		Device type 05, 06, 09, 10				
1	Width of the $\overline{\text{RESET}}$ pulse (PLL stable) <u>32/</u>	$t_{w(\text{RST})}$	See figure 23	10P		ns
	Width of the $\overline{\text{RESET}}$ pulse (PLL needs to sync up) <u>33/</u>			250		
14	Setup time, HD boot configuration bits valid before $\overline{\text{RESET}}$ high	$t_{su(\text{HD})}$		2P		
15	Hold time, HD boot configuration bits valid after $\overline{\text{RESET}}$ high	$t_{su(\text{HD})}$		2P		
Switching characteristics during reset <u>31/ 35/ 36/</u>		Device type 05, 06, 09, 10, 20				
2	Delay time, $\overline{\text{RESET}}$ low to ECLKIN synchronized internally	$t_{d(\text{RSTL-ECKL})}$	See figure 23	2P+3E	3P+4E	ns
3	Delay time, $\overline{\text{RESET}}$ high to ECLKIN synchronized internally	$t_{d(\text{RSTH-ECKI})}$		2P+3E	3P+4E	
4	Delay time, $\overline{\text{RESET}}$ low to EMIF Z group high impedance	$t_{d(\text{RSTL-ENIFZH})}$		2P+3E		
5	Delay time, $\overline{\text{RESET}}$ high to EMIF Z group valid	$t_{d(\text{RSTH-EMIFZV})}$			3P+4E	
6	Delay time, $\overline{\text{RESET}}$ low to EMIF high group invalid	$t_{d(\text{RSTL-EMIFHIV})}$		2P+3E		
7	Delay time, $\overline{\text{RESET}}$ high to EMIF high group valid	$t_{d(\text{RSTH-EMIFHV})}$			3P+4E	
8	Delay time, $\overline{\text{RESET}}$ low to EMIF low group invalid	$t_{d(\text{RSTL-EMIFLIV})}$		2P+3E		
9	Delay time, $\overline{\text{RESET}}$ high to EMIF low group valid	$t_{d(\text{RSTH-EMIFLV})}$			3P+4E	
10	Delay time, $\overline{\text{RESET}}$ low to high group invalid	$t_{d(\text{RSTL-HIGHIV})}$		2P		
11	Delay time, $\overline{\text{RESET}}$ high to high group valid	$t_{d(\text{RSTH-HIGHV})}$			4P	
12	Delay time, $\overline{\text{RESET}}$ low to Z group high impedance	$t_{d(\text{RSTL-ZHZ})}$		2P		
13	Delay time, $\overline{\text{RESET}}$ high to Z group valid	$t_{d(\text{RSTH-ZV})}$		2P		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Unit
				Min	Max	
RESET TIMING (Continuous)						
Timing requirements for reset <u>31/ 37/</u>		Device type (03, 04)K ₂ , 15, 16, 20 <u>9/</u>				
1	Pulse duration, $\overline{\text{RESET}}$	$t_{w(\text{RST})}$	See figure 24	100		ns
13	Setup time, HD boot configuration bits valid before $\overline{\text{RESET}}$ high <u>34/</u>	$t_{su(\text{HD})}$		2P		
14	Hold time, HD boot configuration bits valid after $\overline{\text{RESET}}$ high <u>34/</u>	$t_{su(\text{HD})}$		2P		
Switching characteristics during reset <u>39/</u>		Device type (03, 04)K ₂ , 15, 16, 20 <u>9/</u>				
2	Delay time, external $\overline{\text{RESET}}$ high to internal reset high and all signal group valid <u>40/ 41/</u>	CLKMODE0 = 1 $t_{d(\text{RSTH-ZV})}$	See figure 24		<u>38/</u>	ns
3a	Delay time, $\overline{\text{RESET}}$ low to ECLKOUT low (device type 11, 15)	$t_{d(\text{RSTL-ECKOL})}$		0		
3b	Delay time, $\overline{\text{RESET}}$ low to ECLKOUT high impedance (device type 12, 16, 20)	$t_{d(\text{RSTL-ECKOL})}$		0		
4	Delay time, $\overline{\text{RESET}}$ high to ECLKOUT valid	$t_{d(\text{RSTH-ECKOV})}$			6P	
5a	Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 invalid (device type 11, 15)	$t_{d(\text{RSTL-CKO2IV})}$		0		
5b	Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 high impedance (device type 12, 16, 20)	$t_{d(\text{RSTL-CKO2IV})}$		0		
6	Delay time, $\overline{\text{RESET}}$ high to CLKOUT2 valid	$t_{d(\text{RSTH-CKO2V})}$			6P	
7	Delay time, $\overline{\text{RESET}}$ low to CLKOUT3 low	$t_{d(\text{RSTL-CKO3L})}$		0		
8	Delay time, $\overline{\text{RESET}}$ high to CLKOUT3 valid	$t_{d(\text{RSTH-CKO3V})}$			6P	
9	Delay time, $\overline{\text{RESET}}$ low to EMIF Z group high impedance <u>41/</u>	$t_{d(\text{RSTL-EMIFZH})}$		0		
10	Delay time, $\overline{\text{RESET}}$ low to EMIF low group (BURSEQ) invalid <u>40/</u>	$t_{d(\text{RSTL-EMIFLV})}$		0		
11	Delay time, $\overline{\text{RESET}}$ low to Z group 1 high impedance <u>41/</u>	$t_{d(\text{RSTL-Z1HV})}$		0		
12	Delay time, $\overline{\text{RESET}}$ low to Z group 2 high impedance <u>41/</u>	$t_{d(\text{RSTL-Z2HZ})}$		0		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
EXTERNAL INTERRUPT TIMING								
Timing requirements for external interrupts 31/				Device type 9/ 05-12, (09-12)K ₂		Device type 9/ (01-04)K ₂ , 13-16, 20		
1	Width of the NMI interrupt pulse low	$t_{w(ILOW)}$	See figure 25	2P		2P		ns
	Width of the EXT_INT interrupt pulse low			2P		4P		
2	Width of the NMI interrupt pulse high	$t_{w(IHIGH)}$		2P		2P		
	Width of the EXT_INT interrupt pulse high			2P		4P		
HOST PORT INTERFACE TIMING								
Timing requirements for host port interface cycles 31/ 42/				Device type 05, 09				
1	Setup time, select signals 45/ valid before $\overline{HSTROBE}$ low	$t_{su(SELV-HSTBL)}$	See figure 26 -27			5		ns
2	Hold time, select signals 45/ valid before $\overline{HSTROBE}$ low	$t_h(HSTBL-SELV)$				6 40/		
3	Pulse duration, $\overline{HSTROBE}$ low	$t_w(HSTBL)$				4P		
4	Pulse duration, $\overline{HSTROBE}$ high between consecutive accesses	$t_w(HSTBH)$				4P		
10	Setup time, select signals 45/ valid before \overline{HAS} low	$t_{su(SELV-HASL)}$				5		
11	Hold time, select signals 45/ valid after \overline{HAS} low	$t_h(HASL-SELV)$				3		
12	Setup time, host data valid before $\overline{HSTROBE}$ high	$t_{su(HDV-HSTBH)}$				5		
13	Hold time, host data valid after $\overline{HSTROBE}$ high	$t_h(HSTBH-HDV)$				6 44/		
14	Hold time, $\overline{HSTROBE}$ low after \overline{HRDY} low. $\overline{HSTROBE}$ should not be active until \overline{HRDY} is active (low); otherwise, HPI writes will not complete properly.	$t_h(HRDYL-HSTBL)$				2		
18	Setup time, \overline{HAS} low before $\overline{HSTROBE}$ low	$t_{su(HASL-HSTBL)}$				2		
19	Hold time, \overline{HAS} low after $\overline{HSTROBE}$ low	$t_h(HSTBL-HASL)$				4 44/		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit		
				Min	Max	Min	Max			
HOST PORT INTERFACE TIMING - Continued										
Timing requirements for host port interface cycles <u>31/ 42/</u>				Device type 06		Device type (06)K ₁ , 10 <u>9/</u>				
1	Setup time, select signals <u>45/</u> valid before $\overline{\text{HSTROBE}}$ low	$t_{su(\text{SELV-HSTBL})}$	See figure 26-27	5		5		ns		
2	Hold time, select signals <u>45/</u> valid before $\overline{\text{HSTROBE}}$ low	$t_h(\text{HSTBL-SELV})$		4		4				
3	Pulse duration, $\overline{\text{HSTROBE}}$ low	$t_w(\text{HSTBL})$		4P		4P				
4	Pulse duration, $\overline{\text{HSTROBE}}$ high between consecutive accesses	$t_w(\text{HSTBH})$		4P		4P				
10	Setup time, select signals <u>45/</u> valid before $\overline{\text{HAS}}$ low	$t_{su(\text{SELV-HASL})}$		5		5				
11	Hold time, select signals <u>45/</u> valid after $\overline{\text{HAS}}$ low	$t_h(\text{HASL-SELV})$		3		3				
12	Setup time, host data valid before $\overline{\text{HSTROBE}}$ high	$t_{su(\text{HDV-HSTBH})}$		5		5				
13	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high	$t_h(\text{HSTBH-HDV})$		3		3				
14	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be active until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.	$t_h(\text{HRDYL-HSTBL})$		2		2				
18	Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low	$t_{su(\text{HASL-HSTBL})}$		2		2				
19	Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low	$t_h(\text{HSTBL-HASL})$		2		2				
Timing requirements for host port interface cycles <u>31/ 42/</u>				Device type (03)K ₂ , 15 <u>9/</u>		Device type (04)K ₂ , 16, 20 <u>9/</u>				
1	Setup time, select signals <u>45/</u> valid before $\overline{\text{HSTROBE}}$ low	$t_{su(\text{SELV-HSTBL})}$		See figure 26-27	5		5			ns
2	Hold time, select signals <u>45/</u> valid before $\overline{\text{HSTROBE}}$ low	$t_h(\text{HSTBL-SELV})$			4		4			
3	Pulse duration, $\overline{\text{HSTROBE}}$ low (host read access)	$t_w(\text{HSTBL})$			10P+5.8		4P			
	Pulse duration, $\overline{\text{HSTROBE}}$ low (host write access)				4P		4P			
4	Pulse duration, $\overline{\text{HSTROBE}}$ high between consecutive accesses	$t_w(\text{HSTBH})$			4P		4P			
10	Setup time, select signals <u>45/</u> valid before $\overline{\text{HAS}}$ low	$t_{su(\text{SELV-HASL})}$			5		5			
11	Hold time, select signals <u>45/</u> valid after $\overline{\text{HAS}}$ low	$t_h(\text{HASL-SELV})$			3		3			
12	Setup time, host data valid before $\overline{\text{HSTROBE}}$ high	$t_{su(\text{HDV-HSTBH})}$	5			5				
13	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high	$t_h(\text{HSTBH-HDV})$	3			3				
14	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be active until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.	$t_h(\text{HRDYL-HSTBL})$	2			2				
18	Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low	$t_{su(\text{HASL-HSTBL})}$	2			2				
19	Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low	$t_h(\text{HSTBL-HASL})$	2			2				

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Limits		Unit
				Min	Max	Min	Max	Min	Max	
HOST PORT INTERFACE TIMING - Continued										
Switching Characteristics during host port interface cycles 31/ 43/ 44/ Device type 05, 09										
5	Delay time, \overline{HAS} to \overline{HRDY} 46/	$t_{d(HCS-HRDY)}$	See figure 26-27	1	18					ns
6	Delay time, $\overline{HSTROBE}$ low to \overline{HRDY} high 47/	$t_{d(HSTBL-HRDYH)}$		3	18					
7	Delay time, $\overline{HSTROBE}$ low to HD low impedance for an HPI read	$t_{d(HSTBL-HDLZ)}$		2						
8	Delay time, HD valid to \overline{HRDY} low	$t_{d(HDV-HRDYL)}$		2P-4						
9	Delay time, HD valid after $\overline{HSTROBE}$ high	$t_{d(HSTBH-HDV)}$		3	18					
15	Delay time, $\overline{HSTROBE}$ high to HD impedance	$t_{d(HSTBH-HDHV)}$		3	18					
16	Delay time, $\overline{HSTROBE}$ low to HD valid	$t_{d(HSTBL-HDV)}$		3	18					
17	Delay time, $\overline{HSTROBE}$ high to \overline{HRDY} high 48/	$t_{d(HSTBH-HRDYH)}$		3	18					
Switching Characteristics during host port interface cycles 31/ 43/										
				Device type 06	Device type (06)K ₁ 9/		Device type 10			
5	Delay time, \overline{HAS} to \overline{HRDY} 46/	$t_{d(HCS-HRDY)}$	See figure 26-27	1	15	1	13	1	12	ns
6	Delay time, $\overline{HSTROBE}$ low to \overline{HRDY} high 47/	$t_{d(HSTBL-HRDYH)}$		3	15	3	13	3	12	
7	Delay time, $\overline{HSTROBE}$ low to HD low impedance for an HPI read	$t_{d(HSTBL-HDLZ)}$		2		2		2		
8	Delay time, HD valid to \overline{HRDY} low	$t_{d(HDV-HRDYL)}$		2P-4		2P-4		2P-4		
9	Delay time, HD valid after $\overline{HSTROBE}$ high	$t_{d(HSTBH-HDV)}$		3	15	3	13	3	12	
15	Delay time, $\overline{HSTROBE}$ high to HD impedance	$t_{d(HSTBH-HDHV)}$		3	15	3	13	3	12	
16	Delay time, $\overline{HSTROBE}$ low to HD valid	$t_{d(HSTBL-HDV)}$		3	15	3	13	3	12	
17	Delay time, $\overline{HSTROBE}$ high to \overline{HRDY} high 48/	$t_{d(HSTBH-HRDYH)}$		3	15	3	13	3	12	
Switching Characteristics during host port interface cycles 31/ 43/										
				Device type (03)K ₂ , 15 9/	Device type (04)K ₂ , 16, 20 9/					
5	Delay time, \overline{HAS} to \overline{HRDY} 46/	$t_{d(HCS-HRDY)}$	See figure 26-27	1	15	1	12			ns
6	Delay time, $\overline{HSTROBE}$ low to \overline{HRDY} high 47/	$t_{d(HSTBL-HRDYH)}$		3	15	3	12			
7	Delay time, $\overline{HSTROBE}$ low to HD low impedance for an HPI read	$t_{d(HSTBL-HDLZ)}$		2		2				
8	Delay time, HD valid to \overline{HRDY} low	$t_{d(HDV-HRDYL)}$		2P-4		2P-4				
9	Delay time, HD valid after $\overline{HSTROBE}$ high	$t_{d(HSTBH-HDV)}$		3	12	3	12			
15	Delay time, $\overline{HSTROBE}$ high to HD impedance	$t_{d(HSTBH-HDHV)}$		2	12	2	12			
16	Delay time, $\overline{HSTROBE}$ low to HD valid	$t_{d(HSTBL-HDV)}$		3	10P+5.8	3	12.5			
17	Delay time, $\overline{HSTROBE}$ high to \overline{HRDY} high 48/	$t_{d(HSTBH-HRDYH)}$		3	15	3	12			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING								
Timing requirements for McBSP 31/ 49/				Device type 05, 09				
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 28	CLKR/X ext	2P 49/			ns
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext	50/			
5	Setup, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int	20			
				CLKR ext	1			
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int	6			
				CLKR ext	3			
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int	22			
				CLKR ext	3			
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR int	3			
				CLKR ext	4			
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKX int	23			
			CLKX ext	1				
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-RXH)}$	CLKX int	6				
			CLKX ext	3				
Timing requirements for McBSP 31/ 49/				Device type 06, (06)K1, 10 9/				
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 28	CLKR/X ext	2P 50/			ns
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext	51/			
5	Setup, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int	20			
				CLKR ext	1			
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int	6			
				CLKR ext	5			
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int	22			
				CLKR ext	3			
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR int	3			
				CLKR ext	5			
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKX int	23			
			CLKX ext	1				
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-RXH)}$	CLKX int	6				
			CLKX ext	3				

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Unit
				Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued						
Timing requirements for McBSP <u>31/ 49/</u>			Device type (03, 04)K ₂ , 15, 16, 20 <u>9/</u>			
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 28	CLKR/X ext	2P <u>48/</u>	ns
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext	<u>47/ 49/</u>	
5	Setup, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int	9	
				CLKR ext	1	
6	Hold time, external FSR high after CLKR low	$t_h(CKRL-FRH)$		CLKR int	6	
				CLKR ext	3	
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int	8	
				CLKR ext	0	
8	Hold time, DR valid after CLKR low	$t_h(CKRL-DRV)$		CLKR int	3	
				CLKR ext	4	
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKX int	9	
			CLKX ext	1		
11	Hold time, external FSX high after CLKX low	$t_h(CKXL-RXH)$	CLKX int	6		
			CLKX ext	3		

Switching characteristics for McBSP <u>49/ 54/</u>			Device type 05, 09				
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	$t_{d(CKSH-CKRSH)}$	See figure 28		4	26	ns
2	Cycle time, CLKR/X <u>31/ 49/</u>	$t_{c(CKRX)}$		CLKR/X int	2P		
3	Pulse duration, CLKR/X high or CLKR/X low <u>55/</u>	$t_{w(CKRX)}$		CLKR/X int	C-1	C+1	
4	Delay time, CLKR high to internal FSR valid	$t_{d(CKRH-FRV)}$		CLKR int	-11	3	
9	Delay time, CLKX high to internal FSX valid	$t_{d(CKXH-FXV)}$		CLKX int	-11	3	
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		CLKX ext	3	9	
				CLKX int	-9	4	
13	Delay time, CLKX high to DX valid <u>56/</u>	$t_{d(CKXH-DXV)}$		CLKX ext	3	9	
				CLKX int	-9+D1	7+D2	
14	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	$t_{d(FXH-DXV)}$		CLKX ext	3+D1	19+D2	
				FSX int	-1	3	
				FSX ext	3	9	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Unit		
				Min	Max			
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Switching characteristics for McBSP <u>49/ 54/</u>			Device type 06, 10, (06)K ₁ <u>9/</u>					
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	$t_{d(CKSH-CKRSH)}$	See figure 28		4	26	ns	
2	Cycle time, CLKR/X <u>31/ 50/</u>	$t_{c(CKRX)}$			CLKR/X int	2P		
3	Pulse duration, CLKR/X high or CLKR/X low <u>55/</u>	$t_{w(CKRX)}$			CLKR/X int	C-1		C+1
4	Delay time, CLKR high to internal FSR valid	$t_{d(CKRH-FRV)}$			CLKR int	-11		3
9	Delay time, CLKX high to internal FSX valid	$t_{d(CKXH-FXV)}$			CLKX int	-10		3.5
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$			CLKX ext	3		16
					CLKX int	-9		4
13	Delay time, CLKX high to DX valid <u>56/</u>	$t_{d(CKXH-DXV)}$			CLKX int	-9+D1		8+D2
					CLKX ext	3+D1		26+D2
14	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	$t_{d(FXH-DXV)}$			FSX int	-1		3
					FSX ext	3		9

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Switching characteristics for McBSP <u>49/</u> <u>54/</u>			Device type (03, 04)K ₂ , 15, 16, 20 <u>9/</u>					
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	t _d (CKSH-CKRSH)	See figure 28	1.8	10	1.8	10	ns
2	Cycle time, CLKR/X <u>27/</u> <u>46/</u>	t _c (CKRX)		CLKR/X int	2P		2P	
3	Pulse duration, CLKR/X high or CLKR/X low <u>51/</u>	t _w (CKRX)		CLKR/X int	C-1	C+1	C-1	C+1
4	Delay time, CLKR high to internal FSR valid	t _d (CKRH-FRV)		CLKR int	-2	3	-2	3
9	Delay time, CLKX high to internal FSX valid	t _d (CKXH-FXV)		CLKX int	-2	3	-2	3
12	Disable time, DX high impedance following last data bit from CLKX high	t _{dis} (CKXH-DXHZ)		CLKX ext	2	9	2	9
				CLKX int	-1	4	-1	4
13	Delay time, CLKX high to DX valid <u>51/</u>	t _d (CKXH-DXV)		CLKX ext	1.5	10	1.5	10
				CLKX int	-3.2+D1	4+D2	-3.2+D1	4+D2
14	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	t _d (FXH-DXV)		FSX int	0.5+D1	10+D2	0.5+D1	10+D2
				FSX ext	-1.5	4.5	-1	7.5
			FSX ext	2	9	2	11.5	

Timing requirements for FSR when GSYNC = 1				Device type 05-12		Device type (01-04)K ₂ , 13-16, 20 <u>9/</u>		
1	Setup time, FSR high before CLKS high	t _{su} (FRH-SKSH)	See figure 29	4		4		ns
2	Hold time, FSR high after CLKS high	t _h (CKSH-FRH)		4		4		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit		
				Min	Max	Min	Max			
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued										
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 31/ 57/				Device type 05, 09						
				Master		Slave				
4	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 30	26		2-6P		ns		
5	Hold time, DR valid after CLKX low	$t_h(CKXL-DRV)$		4		6+12P				
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 31/ 57/				Device type 06, 10, (06)K ₁ 9/						
				Master		Slave				
4	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 30	26		2-6P		ns		
5	Hold time, DR valid after CLKX low	$t_h(CKXL-DRV)$		4		14+12P				
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 31/ 57/				Device type (03, 04)K ₂ , 15, 16, 20 9/						
				Master		Slave				
4	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 30	12		2-6P		ns		
5	Hold time, DR valid after CLKX low	$t_h(CKXL-DRV)$		4		5+12P				
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 31/ 57/				Device type 05, 09						
				Master		Slave				
1	Hold time, FSX low after CLKX low 58/	$t_h(CKXL-FXL)$	See figure 30	T-9	T+9			ns		
2	Delay time, FSX low to CLKX high 59/	$t_d(FXL-CKXH)$		L-9	L+9					
3	Delay time, CLKX high to DX valid	$t_d(CKXH-DXV)$		-9	9	6P+4	10P+20			
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis}(CKXL-DXH_Z)$		L-9	L+9					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis}(FXH-DXH_Z)$				2P+3	6P+20			
8	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$				4P+2	8P+20			
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0 31/ 57/				Device type 06, 10, (06)K ₁ 9/						
				Master		Slave				
1	Hold time, FSX low after CLKX low 58/	$t_h(CKXL-FXL)$	See figure 30	T-10	T+10			ns		
2	Delay time, FSX low to CLKX high 59/	$t_d(FXL-CKXH)$		L-10	L+10					
3	Delay time, CLKX high to DX valid	$t_d(CKXH-DXV)$		-10	10	6P+4	-10P+25			
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis}(CKXL-DXH_Z)$		L-10	L+10					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis}(FXH-DXH_Z)$				2P+3	6P+25			
8	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$				4P+2	8P+25			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit		
				Min	Max	Min	Max			
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued										
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0				<u>31/ 57/</u>		Device type (03)K ₂ , 15 <u>9/</u>				
				Master		Slave				
1	Hold time, FSX low after CLKX low <u>58/</u>	$t_{h(CKXL-FXL)}$	See figure 30	T-2	T+3			ns		
2	Delay time, FSX low to CLKX high <u>59/</u>	$t_{d(FXL-CKXH)}$		L-2	L+3					
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+7			
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		L-4	L+3					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+1.5	6P+17			
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17			
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0				<u>31 57</u>		Device type (04)K ₂ , 16, 20 <u>9/</u>				
				Master		Slave				
1	Hold time, FSX low after CLKX low <u>58/</u>	$t_{h(CKXL-FXL)}$	See figure 30	T-2	T+3			ns		
2	Delay time, FSX low to CLKX high <u>59</u>	$t_{d(FXL-CKXH)}$		L-2	L+3					
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+17			
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		L-2	L+3					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+3	6P+17			
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 <u>31/ 57/</u>				Device type 05, 09				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 31	26		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		6+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 <u>31/ 57/</u>				Device type 06, 10, (06)K ₁ <u>9/</u>				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 31	26		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		14+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 <u>31/ 57/</u>				Device type (03, 04)K ₂ , 15, 16, 20 <u>9/</u>				
				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 31	12		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		5+12P		
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 <u>31/ 57/</u>				Device type 05, 09				
				Master		Slave		
1	Hold time, FSX low after CLKX low <u>58/</u>	$t_h(CKXL-FXL)$	See figure 31	L-9	L+9			ns
2	Delay time, FSX low to CLKX high <u>59/</u>	$t_d(FXL-CKXH)$		T-9	T+9			
3	Delay time, CLKX low to DX valid	$t_d(CKXL-DXV)$		-9	9	6P+4	10P+20	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis}(CKXL-DXHZ)$		-9	9	6P+3	10P+20	
7	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$		H-9	H+9	4P+2	8P+20	
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0 <u>31/ 57/</u>				Device type 06, 10, (06)K ₁ <u>9/</u>				
				Master		Slave		
1	Hold time, FSX low after CLKX low <u>58/</u>	$t_h(CKXL-FXL)$	See figure 31	L-10	L+10			ns
2	Delay time, FSX low to CLKX high <u>59/</u>	$t_d(FXL-CKXH)$		T-10	T+10			
3	Delay time, CLKX low to DX valid	$t_d(CKXL-DXV)$		-10	10	6P+4	10P+25	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis}(CKXL-DXHZ)$		-10	10	6P+4	10P+25	
7	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$		H-10	H+10	4P+2	8P+25	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0				<u>31/ 57/</u>		Device type (03)K ₂ , 15 <u>9/</u>		
				Master		Slave		
1	Hold time, FSX low after CLKX low <u>58/</u>	$t_{h(CKXL-FXL)}$	See figure 31	L-2	L+3			ns
2	Delay time, FSX low to CLKX high <u>59/</u>	$t_{d(FXL-CKXH)}$		T-2	T+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-4	4	6P+1.5	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H-2	H+4	4P+2	8P+17	

Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0				<u>31/ 57/</u>		Device type (04)K ₂ , 16, 20 <u>9/</u>		
				Master		Slave		
1	Hold time, FSX low after CLKX low <u>58/</u>	$t_{h(CKXL-FXL)}$	See figure 31	L-2	L+3			ns
2	Delay time, FSX low to CLKX high <u>59/</u>	$t_{d(FXL-CKXH)}$		T-2	T+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-2	4	6P+3	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H-2	H+6.5	4P+2	8P+17	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit		
				Min	Max	Min	Max			
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued										
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1				Device type 05, 09						
31/ 57/				Master		Slave				
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 32	26		2-6P		ns		
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		6+12P				
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1				Device type 06, 10, (06)K ₁ 9/						
31/ 57/				Master		Slave				
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 32	26		2-6P		ns		
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		14+12P				
Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1				Device type (03, 04)K ₂ , 15, 16, 20 9/						
31/ 57/				Master		Slave				
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 32	12		2-6P		ns		
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		5+12P				
Switching characteristics for McBSP as SPI master or slave:				Device type 05, 09						
CLKSTP = 10b, CLKXP = 1				31/ 57/		Master		Slave		
1	Hold time, FSX low after CLKX high 58/	$t_h(CKXH-FXL)$	See figure 32	T-9	T+9			ns		
2	Delay time, FSX low to CLKX low 59/	$t_d(FXL-CKXL)$		H-9	H+9					
3	Delay time, CLKX low to DX valid	$t_d(CKXL-DXV)$		-9	9	6P+4	10P+20			
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis}(CKXH-DXHZ)$		H-9	H+9					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis}(FXH-DXHZ)$				2P+3	6P+20			
8	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$				4P+2	8P+20			
Switching characteristics for McBSP as SPI master or slave:				Device type 06, 10, (06)K ₁ 9/						
CLKSTP = 10b, CLKXP = 1				31/ 57/		Master			Slave	
1	Hold time, FSX low after CLKX high 58/	$t_h(CKXH-FXL)$	See figure 32	T-10	T+10			ns		
2	Delay time, FSX low to CLKX low 59/	$t_d(FXL-CKXL)$		H-10	H+10					
3	Delay time, CLKX low to DX valid	$t_d(CKXL-DXV)$		-10	10	6P+4	10P+25			
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis}(CKXH-DXHZ)$		H-10	H+10					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis}(FXH-DXHZ)$				2P+3	6P+25			
8	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$				4P+2	8P+25			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit		
				Min	Max	Min	Max			
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued										
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1				<u>31/ 57/</u>		Device type (03)K ₂ , 15 <u>9/</u>				
				Master		Slave				
1	Hold time, FSX low after CLKX high <u>58/</u>	$t_{h(CKXH-FXL)}$	See figure 32	T-2	T+3			ns		
2	Delay time, FSX low to CLKX low <u>59/</u>	$t_{d(FXL-CKXL)}$		H-2	H+3					
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17			
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		H-3.6	H+3					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+1.5	6P+17			
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17			
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1				<u>31/ 57/</u>		Device type (04)K ₂ , 16, 20 <u>9/</u>				
				Master		Slave				
1	Hold time, FSX low after CLKX high <u>58/</u>	$t_{h(CKXH-FXL)}$	See figure 32	T-2	T+3			ns		
2	Delay time, FSX low to CLKX low <u>59/</u>	$t_{d(FXL-CKXL)}$		H-2	H+3					
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-3	4	6P+2	10P+17			
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		H-2	H+3					
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				2P+3	6P+17			
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				4P+2	8P+17			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions 2/	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1				Device type 05, 09				
31/ 57/				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 33	26		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		6+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1				Device type 06, 10, (06)K ₁ 9/				
31/ 57/				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 33	26		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		14+12P		
Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1				Device type (03, 04)K ₂ , 15, 16, 20 9/				
31/ 57/				Master		Slave		
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 33	12		2-6P		ns
5	Hold time, DR valid after CLKX high	$t_h(CKXH-DRV)$		4		5+12P		
Switching characteristics for McBSP as SPI master or slave:				Device type 05, 09				
CLKSTP = 11b, CLKXP = 1				31/ 57/				
1	Hold time, FSX low after CLKX high 58/	$t_h(CKXH-FXL)$	See figure 33	H-9	H+9			ns
2	Delay time, FSX low to CLKX low 59/	$t_d(FXL-CKXL)$		T-9	T+9			
3	Delay time, CLKX high to DX valid	$t_d(CKXH-DXV)$		-9	9	6P+4	10P+20	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis}(CKXH-DXHZ)$		-9	9	6P+3	10P+20	
7	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$		L-9	L+9	4P+2	8P+20	
Switching characteristics for McBSP as SPI master or slave:				Device type 06, 10, (06)K ₁ 9/				
CLKSTP = 11b, CLKXP = 1				31/ 57/				
1	Hold time, FSX low after CLKX high 58/	$t_h(CKXH-FXL)$	See figure 33	H-10	H+10			ns
2	Delay time, FSX low to CLKX low 59/	$t_d(FXL-CKXL)$		T-10	T+10			
3	Delay time, CLKX high to DX valid	$t_d(CKXH-DXV)$		-10	10	6P+4	10P+25	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis}(CKXH-DXHZ)$		-10	10	6P+3	10P+25	
7	Delay time, FSX low to DX valid	$t_d(FXL-DXV)$		L-10	L+10	4P+2	8P+25	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT TIMING - Continued								
Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0				<u>31/ 57/</u>		Device type (03)K ₂ , 15 <u>9/</u>		
				Master		Slave		
1	Hold time, FSX low after CLKX high <u>58/</u>	$t_{h(CKXH-FXL)}$	See figure 33	H-2	H+3			ns
2	Delay time, FSX low to CLKX low <u>59/</u>	$t_{d(FXL-CKXL)}$		T-2	T+3			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		-3.6	4	6P+1.5	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L-2	L+4	4P+2	8P+17	

Switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0				<u>31/ 57/</u>		Device type (04)K ₂ , 16, 20 <u>9/</u>		
				Master		Slave		
1	Hold time, FSX low after CLKX high <u>58/</u>	$t_{h(CKXH-FXL)}$	See figure 33	H-2	H+3			ns
2	Delay time, FSX low to CLKX low <u>59/</u>	$t_{d(FXL-CKXL)}$		T-2	T+3			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-3	4	6P+2	10P+17	
6	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		-2	4	6P+3	10P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L-2	L+6.5	4P+2	8P+17	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test conditions <u>2/</u>	Limits		Limits		Unit
				Min	Max	Min	Max	
TIMER TIMING								
Timing requirements for timer inputs <u>31/</u>				Device type 05-12		Device type (01-04)K ₂ , 13-16, 20 <u>9/</u>		
1	Pulse duration, TNP high	$t_{w(TINPH)}$	See figure 34	2P		2P		ns
2	Pulse duration, TNP low	$t_{w(TINPL)}$		2P		2P		
Switching characteristics for time outputs <u>31/</u>				Device type 05-12		Device type (01-04)K ₂ , 13-16, 20 <u>9/</u>		
3	Pulse duration, TOUT high	$t_{w(TOUTH)}$	See figure 34	4P-3		4P-3		ns
4	Pulse duration, TOUT low	$t_{w(TOUTL)}$		4P-3		4P-3		
GENERAL PURPOSE INPUT/OUTPUT (GPIO) PORT TIMING [Device type 03 and 04 only]								
Timing requirements for GPIO inputs <u>31/</u> <u>60/</u>						Device type (01-04)K ₂ , 13-16, 20 <u>9/</u>		
1	Pulse duration, GPIx high	$t_{w(GPIH)}$	See figure 35			4P		ns
2	Pulse duration, GPIx low	$t_{w(GPIL)}$				4P		
Switching characteristics for GPIO outputs <u>31/</u> <u>60/</u>						Device type (01-04)K ₂ , 13-16, 20 <u>9/</u>		
3	Pulse duration, GPOx high	$t_{w(GPOH)}$	See figure 35			12P-3		ns
4	Pulse duration, GPOx low	$t_{w(GPOL)}$				12P-3		
JTAG TEST PORT TIMING								
Timing requirements for JTAG test port				Device type 05-12		Device type (01-04)K ₂ , 13-16, 20 <u>9/</u>		
1	Cycle time, TCK	$t_c(TCK)$	See figure 36	35		35		ns
3	Setup time, TDI/TMS/ \overline{TRST} valid before TCK high	$t_{su}(TDIV-TCKH)$		10		10		
4	Hold time, TDI/TMS/ \overline{TRST} valid after TCK high	$t_h(TCKH-TDIV)$		9		7		
Switching characteristics for JTAG test port				Device type 05-12		Device type (01-04)K ₂ , 13-16, 20 <u>9/</u>		
2	Delay time, TCK low to TDO valid	$t_d(TCKL-TDOV)$	See figure 36	-3	18	0	15	ns

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Test conditions are over recommended ranges of supply voltage and operating case temperature unless otherwise specified.
- 3/ Device types: 01, 05, 09, 13, and 17.
- 4/ Device types: 02, 06, 10, 14, and 18.
- 5/ Device types: 03, 07, 11, 15, and 19.
- 6/ Device types: 04, 08, 12, 16, and 20.
- 7/ For device type 5/ and 6/, these currents were measured with average activity (50% high/50% low power) at 25°C case temperature and 100 MHz EMIF. This model represents a device performing high DSP activity operations 50% of the time, and the remainder performing low DSP activity operations. The high/low DSP activity models are defined as follow
 High DSP activity model:
 CPU: 8 instructions/cycle with 2LDDW instructions [L1 Data Memory: 128 bits/cycle via LDDW instructions; L1 program memory: 256 bits/cycle; L2/EMIF EDMA: 50% writes, 50% reads to/from SDRAM (50% bit switching)]
 McBSP: 2 channels at E1 rate
 Times: 2 times at maximum rate.
 Low DSP activity model:
 CPU: 2 instructions/cycle with 1 LDH instruction [L1 data memory: 16 bits/cycle; L1 program memory: 256 bits per 4 cycles; L2/EMIF EDMA: None]
 McBSP: 2 channels at E1 rate
 Times: 2 times at maximum rate.
- 8/ For device type 3/ and 4/, these currents were measured with average activity (50% high/50% low power).
- 9/ K₁: Case outline X, operate at -40°C to +105°C.
 K₂: Case outline Y, operate at -40°C to +105°C.
- 10/ The reference points for the rise and fall transactions are measured at V_{IL} max and V_{IH} min.
- 11/ C = CLKIN cycle time in nanoseconds (ns). For example, when CLKIN frequency is 40 MHz, use C = 25 ns.
- 12/ See PLL and PLL controller section from manufacturer data.
- 13/ The reference points for the rise and fall transactions are measured at V_{OL} max and V_{OH} min.
- 14/ P = 1/CPU cloc frequency in nanoseconds (ns).
- 15/ PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.
- 16/ C₂ = CLKOUT2 period in ns. CLKOUT2 period is determined by the PLL controller output SYSCLOCK2 period, which must be set to CPU period divide by 2.
- 17/ C₃ = CLKOUT3 period in ns. CLKOUT3 period is a divide down of the CPU clock, configurable via the RATIO field in the PLLDIV3 register.
- 18/ E = ECLKIN period in ns.
- 19/ EH is high period of ECLKIN in ns and EL is the low period of ECLKIN in ns.
- 20/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = 2E) to ensure setup and hold time is met.
- 21/ RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.
- 22/ E = ECLKOUT period in ns.
- 23/ Select signals include: $\overline{\text{CE}}_x$, $\overline{\text{BE}}[3:0]$, EA[21:2], and $\overline{\text{AOE}}$.
- 24/ Device types: 3/, 4/, 5/ and 6/, SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.
- 25/ Make sure the external SBSRAM meets the timing specifications of the C6711 device. Delays or buffers may be needed to compensate for any timing differences. IBIS analysis should be used to correctly model the system interface.
- 26/ $\overline{\text{ARE}}$ / $\overline{\text{SDCAS}}$ / $\overline{\text{SSADS}}$, $\overline{\text{AOE}}$ / $\overline{\text{SDRAS}}$ / $\overline{\text{SSOE}}$, and $\overline{\text{AWE}}$ / $\overline{\text{SDWE}}$ / $\overline{\text{SSWE}}$ operate as $\overline{\text{SSADSS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
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TABLE I. Electrical performance characteristics - Continued.

- 27/ \overline{ARE} / \overline{SDCAS} / \overline{SSADS} , \overline{AWE} / \overline{SDWE} / \overline{SSWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SSOE} operate as \overline{SDCAS} , \overline{SDWE} , and \overline{SDRAS} , respectively, during SDRAM accesses.
- 28/ E = ECLKIN period in ns.
- 29/ EMIF bus consists of \overline{AWE} , \overline{AWE} , ED[31:0], EA[21:2], \overline{ARE} / \overline{SDCAS} / \overline{SSADS} , \overline{AOE} / \overline{SDRAS} / \overline{SSOE} , and \overline{AWE} / \overline{SDWE} / \overline{SSWE} .
- 30/ All pending EMIF transactions are allowed to complete before \overline{HOLDA} is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.
- 31/ P = 1/CPU clock frequency in nanoseconds (ns). For example, when running parts at 250 MHz, use P = 4 ns.
- 32/ This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x4 when CLKIN and PLL are stable.
- 33/ This parameter applies to CLKMODE x4 only (it does not apply to CLKMODE x1). The \overline{RESET} signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 μ s to stabilize following power up or after PLL configuration has been changed. During that time \overline{RESET} must be asserted to ensure proper device operation. See the clock PLL in manufacturer data for PLL clock times.
- 34/ HD[4:3] are the boot configuration pins during device reset.
- 35/ E = ECLKIN period in ns.
- 36/ EMIF Z group consists of: EA[21:2], ED[31:0], \overline{CE} [3:0], \overline{BE} [3:0], \overline{ARE} / \overline{SDCAS} / \overline{SSADS} , \overline{AWE} / \overline{SDWE} / \overline{SSWE} , and \overline{AOE} / \overline{SDRAS} / \overline{SSOE}
- EMIF high group consists of: \overline{HOLDA}
 EMIF low group consists of: \overline{BUSREQ}
 High group consists of: \overline{HRDY} and \overline{HINT}
 Z group consists of: HD[15:0], CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, TOUT0, and TOUT1.
- 37/ For device types 5/ and 6/, the PLL is bypassed immediately after the device comes out of reset. The PLL Controller can be programmed to change the PLL mode in software. See manufacturer for more detail.
- 38/ The boot and device configurations bits are latched asynchronously when RESET is transitioning high. The boot and device configurations bits consist of HD[8,4:3].
- 39/ P = 1/CPU clock frequency in ns. Note that while internal reset is asserted low, the CPU clock (SYSCLK1) period is equal to the input clock (CLKIN) period multiplied by 8. For example, if the CLKIN period is 20 ns, then the CPU clock (SYSCLK1) period is 20 ns x 8 = 160 ns. Therefore, P = SYSCLK1 = 160 ns while internal reset is asserted.
- 40/ The internal reset is stretched exactly 512 x CLKIN cycles if CLKIN is used (CLKMODE0 = 1). If the input clock (CLKIN) is not stable when RESET is deasserted, the actual delay may vary.
- 41/ EMIF Z group consists of: EA[21:2], ED[31:0], \overline{CE} [3:0], \overline{BE} [3:0], \overline{ARE} / \overline{SDCAS} / \overline{SSADS} , \overline{AWE} / \overline{SDWE} / \overline{SSWE} , \overline{AOE} / \overline{SDRAS} / \overline{SSOE} , and \overline{HOLDA}
- EMIF low group consists of: \overline{BUSREQ}
 Z group 1 consists of: CLKR0, CLKR1, CLKX0, CLKX1, FSR0, FSR1, FSX0, FSX1, DX0, DX1, TOUT0, and TOUT1.
 Z group 2 consists of: All other HPI and GPIO signals.
- 42/ 512 x CLKIN period.
- 43/ $\overline{HSTROBE}$ refers to the following logical operation on \overline{HCS} , $\overline{HDS1}$, and $\overline{HDS2}$: [NOT($\overline{HDS1}$ XOR $\overline{HDS2}$)] OR \overline{HCS} .
- 44/ Make sure the external host meets the timing specifications of the device type 01. Delays or buffers may be needed to compensate for any timing differences. IBIS analysis should be used to correctly model the system interface.
- 45/ Select signal include: HCNTL[1:0], \overline{HR} / \overline{W} , and HHWL.
- 46/ \overline{HCS} enables \overline{HRDY} , and \overline{HRDY} is always low when \overline{HCS} is high. The case where \overline{HRDY} goes high when \overline{HCS} falls indicates that HPI is busy completing a previous HPID WRITE or READ with autoincrement.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
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TABLE I. Electrical performance characteristics - Continued.

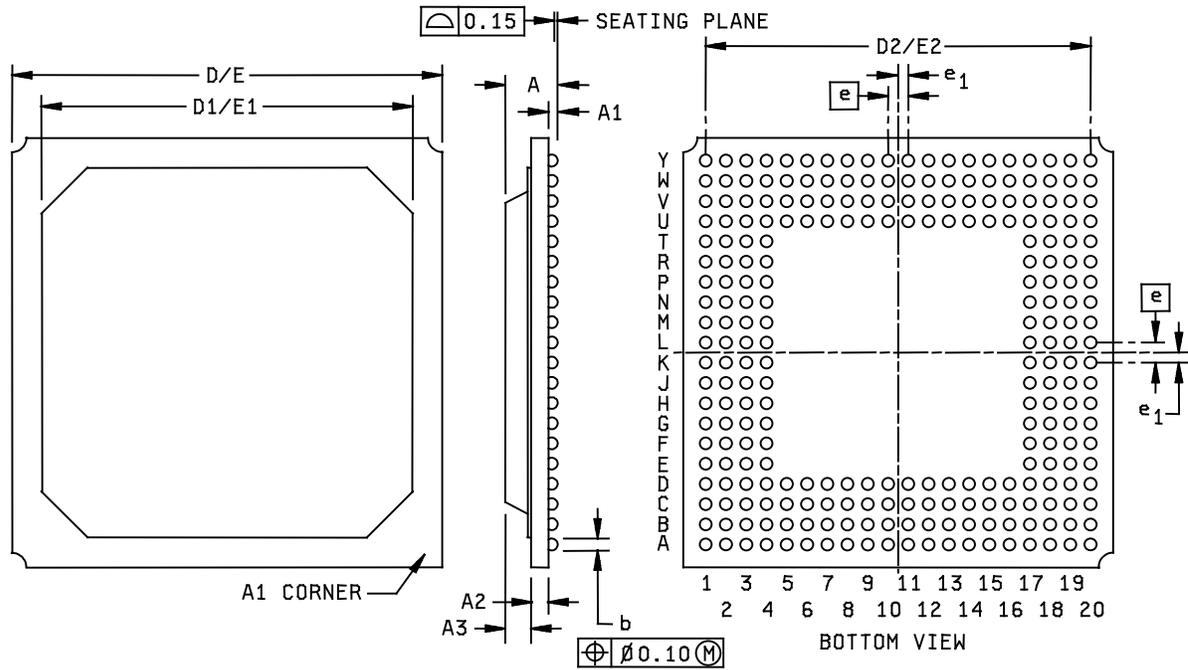
- 47/ This parameter is used during an HPID read. At the beginning of the first half word transfer on the falling edge of $\overline{\text{HSTROBE}}$, the HPI sends the request to the EDMA internal address generation hardware, and $\overline{\text{HRDY}}$ remains high until the EDMA internal address generation hardware loads the requested data into HPID.
- 48/ This parameter is used after the second half word of an HPID write or autoincrement read. $\overline{\text{HRDY}}$ remains low if the access is not an HPID write or or autoincrement read. Reading or writing to HPIC or HPIA does not affect the $\overline{\text{HRDY}}$ signal.
- 49/ $\text{CLKRP} = \text{CLKXP} = \text{FSRP} = \text{FSXP} = 0$. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- 50/ The minimum CLKR/X period is twice the CPU cycle time (2P). This means that the maximum bit rate for communications between the McBSP and other device is 75 Mbps for 150 MHz CPU clock or 50 Mbps for 100 MHz CPU clock; where the McBSP is either the master or slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP to McBSP communication is 33 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 30 ns (33 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 33 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP to McBSP communications applies when the serial port is a Master of the clock and frame syncs (with CLKR connected to CLKX , FSR connected to FSX , $\text{CLKXM} = \text{FSXM} = 1$, and $\text{CLKRM} = \text{FSRM} = 0$) in data delay 1 or 2 mode ($\text{R/XDATDLY} = 01\text{b}$ or 10b) and the other device the McBSP communicates to is a slave.
- 51/ $0.5t_{\text{C}(\text{CKRX})}$
- 52/ The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other device is 75 Mbps for 150 MHz CPU clock or 50 Mbps for 100 MHz CPU clock; where the McBSP is either the master or slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP to McBSP communication is 33 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 30 ns (33 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 33 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP to McBSP communications applies when the serial port is a Master of the clock and frame syncs (with CLKR connected to CLKX , FSR connected to FSX , $\text{CLKXM} = \text{FSXM} = 1$, and $\text{CLKRM} = \text{FSRM} = 0$) in data delay 1 or 2 mode ($\text{R/XDATDLY} = 01\text{b}$ or 10b) and the other device the McBSP communicates to is a slave.
- 53/ This parameter is applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.
- 54/ Minimum delay times also represent minimum output hold times.
- 55/ C = H or L
 S = Sample rate generator input clock = 2P if $\text{CLKSM} = 1$ (P = 1/CPU clock frequency)
 = Sample rate generator input clock = P_clks if $\text{CLKSM} = 0$ (P_clks = CLKS period)
 T = CLKX period = $(1 + \text{CLKGDV}) * S$
 H = CLKX high pulse width = $(\text{CLKGDV}/2 + 1) * S$ if CLKGDV is even
 = $(\text{CLKGDV} + 1)/2 * S$ if CLKGDV is odd or zero
 L = CLKX low pulse width = $(\text{CLKGDV}/2) * S$ if CLKGDV is even
 = $(\text{CLKGDV} + 1)/2 * S$ if CLKGDV is odd or zero
- 56/ Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if $\text{DXENA} = 1$ in SPCR.
 If $\text{DXENA} = 0$, then $\text{D1} = \text{D2} = 0$
 If $\text{DXENA} = 1$, then $\text{D1} = 2\text{P}$, $\text{D2} = 4\text{P}$
- 57/ For all SPI slave modes, CLKG is programmed as $\frac{1}{2}$ of the CPU clock by setting $\text{CLKSM} = \text{CLKGDV} = 1$.
- 58/ $\text{FSRP} = \text{FSXP} = 1$. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
 $\text{CLKXM} = \text{FSXM} = 1$, $\text{CLKRM} = \text{FSRM} = 0$ for master McBSP
 $\text{CLKXM} = \text{CLKRM} = \text{FSXM} = \text{FSRM} = 0$ for slave McBSP

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- 59/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).
- 60/ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the DSP recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to at least 24P to allow the DSP enough time to access the GPIO register through the CFGBUS.
- 61/ The number of CFGBUS cycles between two back-to-back CFGBUS writes to the GPIO register is 12 SYSCLK1 cycles; therefore, the minimum GPOx pulse width is 12P.

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Case X



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-151.

FIGURE 1. Case outlines.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 39</p>

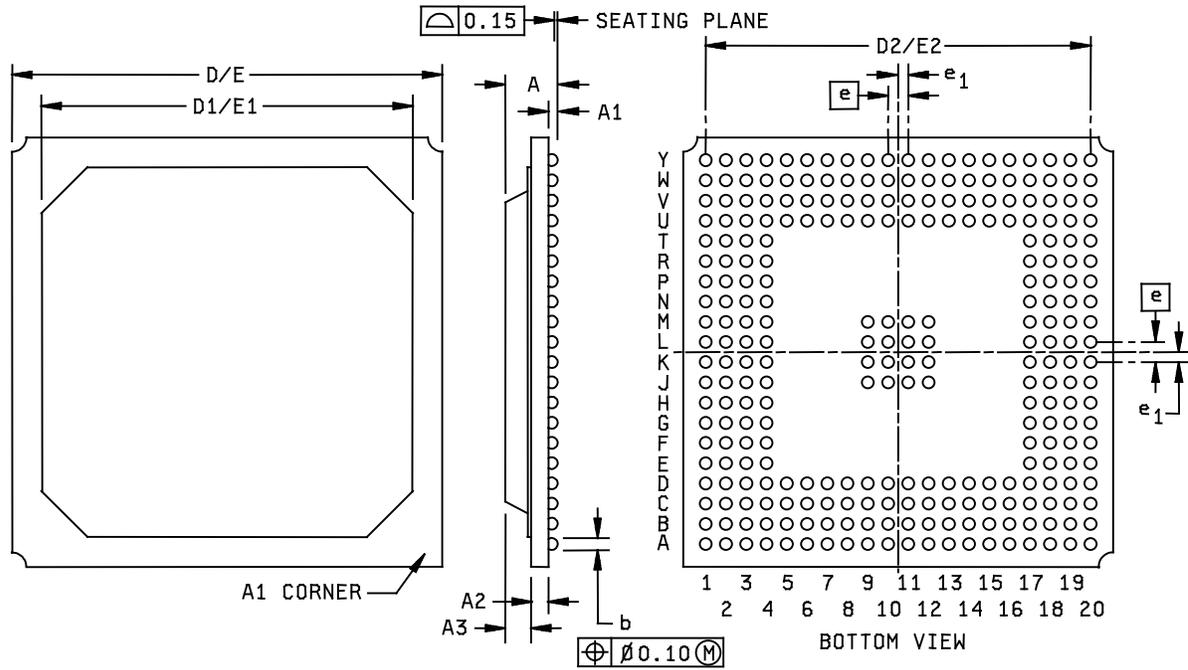
Case X

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A		2.32		0.091
A1	0.50	0.70	0.020	0.028
A2	0.30	0.40	0.012	0.016
A3	1.17 TYP		0.046 TYP	
b	0.60	0.90	0.024	0.035
D/E	26.80	27.20	1.055	1.071
D1/E1	23.80	24.70	0.937	0.965
D2/E2	24.13 TYP		0.950 TYP	
e	1.27 NOM		0.050 NOM	
e1	0.635 NOM		0.025 NOM	

FIGURE 1. Case outline - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
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Case Y



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-151.

FIGURE 1. Case outline - Continued.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 41</p>

Case Y

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A		2.57		0.101
A1	0.50	0.70	0.020	0.028
A2	0.57	0.65	0.022	0.026
A3	1.12	1.22	0.044	0.048
b	0.60	0.90	0.024	0.035
D/E	26.80	27.20	1.055	1.071
D1/E1	23.80	24.20	0.937	0.953
D2/E2	24.13 TYP		0.950 TYP	
e	1.27 NOM		0.050 NOM	
e1	0.635 NOM		0.025 NOM	

FIGURE 1. Case outline - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 42

Case X

[Device type 01, 02, 05, 06, 09, 10, 13, 14, 17, and 18 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
A1	V _{SS}	B1	V _{SS}	C1	GP[5](EXT_INT5)	D1	DV _{DD}
A2	V _{SS}	B2	CV _{DD}	C2	GP[4](EXT_INT4)	D2	GP[6](EXT_INT6)
A3	CLKIN	B3	DV _{DD}	C3	CV _{DD}	D3	RSV
A4	PLLV	B4	V _{SS}	C4	CLKMODE0	D4	V _{SS}
A5	RSV	B5	PLL \overline{F}	C5	DV _{DD}	D5	CV _{DD}
A6	TCK	B6	TR \overline{ST}	C6	PLL \overline{G}	D6	CV _{DD}
A7	TDI	B7	TMS	C7	CV _{DD}	D7	CLKOUT1
A8	TDO	B8	DV _{DD}	C8	V _{SS}	D8	V _{SS}
A9	CV _{DD}	B9	EMU1	C9	V _{SS}	D9	EMU0
A10	CV _{DD}	B10	EMU3	C10	DV _{DD}	D10	EMU2
A11	V _{SS}	B11	V _{SS}	C11	EMU4	D11	CV _{DD}
A12	CV _{DD}	B12	EMU5	C12	RSV	D12	RSV
A13	RE \overline{SET}	B13	DV _{DD}	C13	NMI	D13	V _{SS}
A14	V _{SS}	B14	HD15	C14	HD14	D14	CV _{DD}
A15	HD13	B15	V _{SS}	C15	HD12	D15	CV _{DD}
A16	HD11	B16	HD10	C16	HD9	D16	DV _{DD}
A17	DV _{DD}	B17	HD8	C17	HD6	D17	V _{SS}
A18	HD7	B18	HD5	C18	CV _{DD}	D18	HD2
A19	V _{SS}	B19	CV _{DD}	C19	HD4	D19	DV _{DD}
A20	V _{SS}	B20	V _{SS}	C20	HD3	D20	HD1
E1	CLKS1	F1	TOUT1	G1	TOUT0	H1	FSX0
E2	V _{SS}	F2	TINP1	G2	TINP0	H2	DX0
E3	GP[7](EXT_INT7)	F3	DV _{DD}	G3	CLKX0	H3	CLKR0
E4	V _{SS}	F4	CV _{DD}	G4	V _{SS}	H4	V _{SS}
E17	V _{SS}	F17	CV _{DD}	G17	V _{SS}	H17	V _{SS}
E18	HAS $\overline{}$	F18	HDS $\overline{2}$	G18	HCNTL0	H18	DV _{DD}
E19	HDS1 $\overline{}$	F19	V _{SS}	G19	HCNTL1	H19	HRDY $\overline{}$
E20	HD0	F20	HCS $\overline{}$	G20	HR/W $\overline{}$	H20	HHWIL

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
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Case X

[Device type 01, 02, 05, 06, 09, 10, 13, 14, 17, and 18 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
J1	DR0	K1	CV _{DD}	L1	FSX1	M1	CLKR1
J2	DV _{DD}	K2	V _{SS}	L2	DX1	M2	DR1
J3	FSR0	K3	CLKS0	L3	CLKX1	M3	FSR1
J4	V _{SS}	K4	CV _{DD}	L4	CV _{DD}	M4	V _{SS}
J17	$\overline{\text{HOLD}}$	K17	CV _{DD}	L17	CV _{DD}	M17	V _{SS}
J18	$\overline{\text{HOLDA}}$	K18	ED0	L18	ED2	M18	DV _{DD}
J19	BUSREQ	K19	ED1	L19	ED3	M19	ED4
J20	$\overline{\text{HINT}}$	K20	V _{SS}	L20	CV _{DD}	M20	ED5

FIGURE 2. Terminal connections - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 44

Case X

[Device type 01, 02, 05, 06, 09, 10, 13, 14, 17, and 18 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
N1	DV _{DD}	P1	ED28	R1	DV _{DD}	T1	ED24
N2	RSV	P2	ED29	R2	ED27	T2	ED25
N3	ED31	P3	ED30	R3	ED26	T3	DV _{DD}
N4	V _{SS}	P4	V _{SS}	R4	CV _{DD}	T4	V _{SS}
N17	V _{SS}	P17	V _{SS}	R17	CV _{DD}	T17	V _{SS}
N18	ED6	P18	ED9	R18	DV _{DD}	T18	ED13
N19	ED7	P19	V _{SS}	R19	ED11	T19	ED15
N20	ED8	P20	ED10	R20	ED12	T20	ED14
U1	ED22	V1	ED20	W1	V _{SS}	Y1	V _{SS}
U2	ED21	V2	ED19	W2	CV _{DD}	Y2	V _{SS}
U3	ED23	V3	CV _{DD}	W3	DV _{DD}	Y3	ED18
U4	V _{SS}	V4	ED16	W4	ED17	Y4	$\overline{\text{BE}}_2$
U5	DV _{DD}	V5	$\overline{\text{BE}}_3$	W5	V _{SS}	Y5	ARDY
U6	CV _{DD}	V6	$\overline{\text{CE}}_3$	W6	$\overline{\text{CE}}_2$	Y6	EA2
U7	DV _{DD}	V7	EA3	W7	EA4	Y7	DV _{DD}
U8	V _{SS}	V8	EA5	W8	EA6	Y8	EA7
U9	V _{SS}	V9	EA8	W9	DV _{DD}	Y9	EA9
U10	CV _{DD}	V10	EA10	W10	$\overline{\text{AOE}} / \overline{\text{SDRAS}} / \overline{\text{SSOE}}$	Y10	ECLKOUT
U11	CV _{DD}	V11	$\overline{\text{ARE}} / \overline{\text{SDCAS}} / \overline{\text{SSADS}}$	W11	V _{SS}	Y11	ECLKIN
U12	DV _{DD}	V12	$\overline{\text{AWE}} / \overline{\text{SDWE}} / \overline{\text{SSWE}}$	W12	DV _{DD}	Y12	CLKOUT2/(GP[2])
U13	V _{SS}	V13	DV _{DD}	W13	EA11	Y13	V _{SS}
U14	CV _{DD}	V14	EA12	W14	EA13	Y14	EA14
U15	CV _{DD}	V15	DV _{DD}	W15	EA15	Y15	EA16
U16	DV _{DD}	V16	EA17	W16	V _{SS}	Y16	EA18
U17	V _{SS}	V17	$\overline{\text{CE}}_0$	W17	EA19	Y17	DV _{DD}
U18	EA21	V18	CV _{DD}	W18	$\overline{\text{CE}}_1$	Y18	EA20
U19	$\overline{\text{BE}}_1$	V19	DV _{DD}	W19	CV _{DD}	Y19	V _{SS}
U20	V _{SS}	V20	$\overline{\text{BE}}_0$	W20	V _{SS}	Y20	RSV

FIGURE 2. Terminal connections - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 45

Case Y

[Device type 03, 04, 07, 08, 11, 12, 15, 16, 19, and 20 only]

Pin No	Signal name						
A1	V _{SS}	B1	V _{SS}	C1	GP[5](EXT_INT5)	D1	DV _{DD}
A2	V _{SS}	B2	CV _{DD}	C2	GP[4](EXT_INT4)	D2	GP[6](EXT_INT6)
A3	CLKIN	B3	DV _{DD}	C3	CV _{DD}	D3	EMU2
A4	CV _{DD}	B4	V _{SS}	C4	CLKMODE0	D4	V _{SS}
A5	RSV	B5	RSV	C5	PLLHV	D5	CV _{DD}
A6	TCK	B6	TRST	C6	V _{SS}	D6	CV _{DD}
A7	TDI	B7	TMS	C7	CV _{DD}	D7	RSV
A8	TDO	B8	DV _{DD}	C8	V _{SS}	D8	V _{SS}
A9	CV _{DD}	B9	EMU1	C9	V _{SS}	D9	EMU0
A10	CV _{DD}	B10	EMU3	C10	DV _{DD}	D10	CLKOUT3
A11	V _{SS}	B11	RSV	C11	EMU4	D11	CV _{DD}
A12	RSV	B12	EMU5	C12	RSV	D12	RSV
A13	RESET	B13	DV _{DD}	C13	NMI	D13	V _{SS}
A14	V _{SS}	B14	HD15	C14	HD14	D14	CV _{DD}
A15	HD13	B15	V _{SS}	C15	HD12	D15	CV _{DD}
A16	HD11	B16	HD10	C16	HD9	D16	DV _{DD}
A17	DV _{DD}	B17	HD8	C17	HD6	D17	V _{SS}
A18	HD7	B18	HD5	C18	CV _{DD}	D18	HD2
A19	V _{SS}	B19	CV _{DD}	C19	HD4	D19	DV _{DD}
A20	V _{SS}	B20	V _{SS}	C20	HD3	D20	HD1
E1	CLKS1	F1	TOUT1	G1	TOUT0	H1	FSX0
E2	V _{SS}	F2	TINP1	G2	TINP0	H2	DX0
E3	GP[7](EXT_INT7)	F3	DV _{DD}	G3	CLKX0	H3	CLKR0
E4	V _{SS}	F4	CV _{DD}	G4	V _{SS}	H4	V _{SS}
E17	V _{SS}	F17	CV _{DD}	G17	V _{SS}	H17	V _{SS}
E18	HAS	F18	HDS2	G18	HCNTL0	H18	DV _{DD}
E19	HDS1	F19	V _{SS}	G19	HCNTL1	H19	HRDY
E20	HD0	F20	HCS	G20	HR/W	H20	HHWIL

FIGURE 2. Terminal connections - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 46

Case Y

[Device type 03, 04, 07, 08, 11, 12, 15, 16, 19, and 20 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
J1	DR0	K1	CV _{DD}	L1	FSX1	M1	CLKR1
J2	DV _{DD}	K2	V _{SS}	L2	DX1	M2	DR1
J3	FSR0	K3	CLKS0	L3	CLKX1	M3	FSR1
J4	V _{SS}	K4	CV _{DD}	L4	CV _{DD}	M4	V _{SS}
J9	V _{SS}	K9	V _{SS}	L9	V _{SS}	M9	V _{SS}
J10	V _{SS}	K10	V _{SS}	L10	V _{SS}	M10	V _{SS}
J11	V _{SS}	K11	V _{SS}	L11	V _{SS}	M11	V _{SS}
J12	V _{SS}	K12	V _{SS}	L12	V _{SS}	M12	V _{SS}
J17	$\overline{\text{HOLD}}$	K17	CV _{DD}	L17	CV _{DD}	M17	V _{SS}
J18	$\overline{\text{HOLDA}}$	K18	ED0	L18	ED2	M18	DV _{DD}
J19	BUSREQ	K19	ED1	L19	ED3	M19	ED4
J20	$\overline{\text{HINT}}$	K20	V _{SS}	L20	CV _{DD}	M20	ED5

FIGURE 2. Terminal connections - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 47

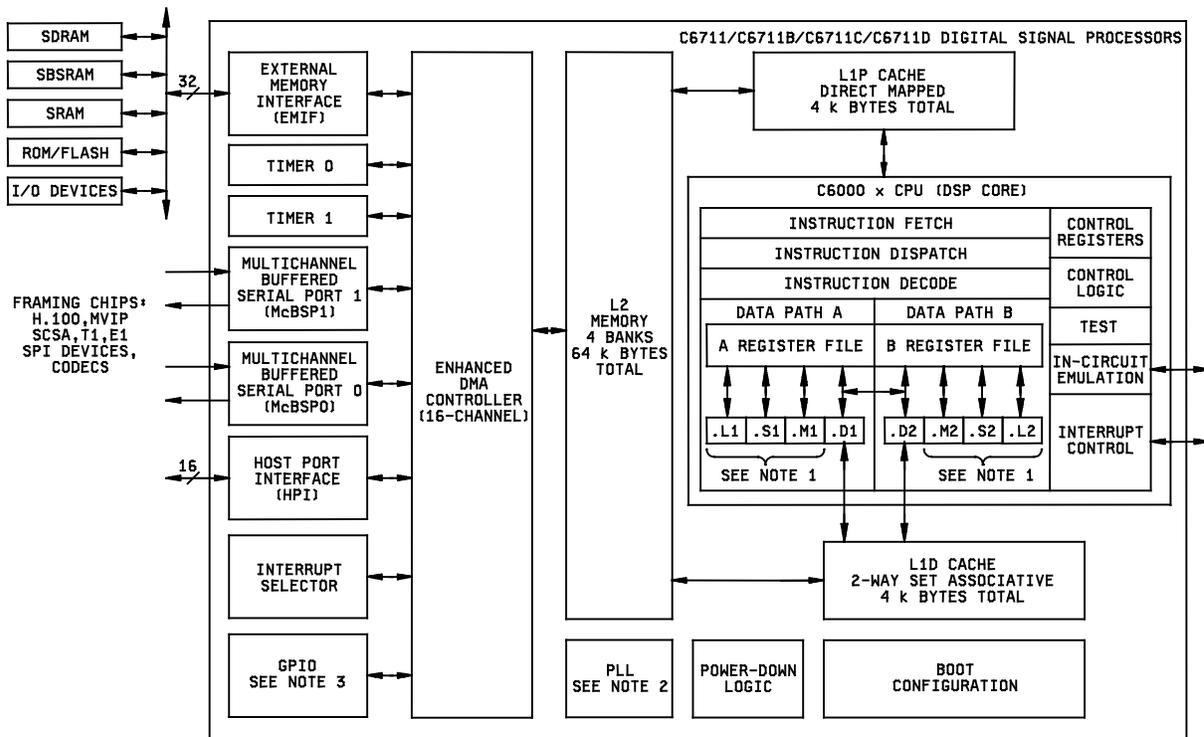
Case Y

[Device type 03, 04, 07, 08, 11, 12, 15, 16, 19, and 20 only]

Pin No	Signal name	Pin No	Signal name	Pin No	Signal name	Pin No	Signal name
N1	RSV	P1	ED28	R1	DV _{DD}	T1	ED24
N2	RSV	P2	ED29	R2	ED27	T2	ED25
N3	ED31	P3	ED30	R3	ED26	T3	DV _{DD}
N4	V _{SS}	P4	V _{SS}	R4	CV _{DD}	T4	V _{SS}
N17	V _{SS}	P17	V _{SS}	R17	CV _{DD}	T17	V _{SS}
N18	ED6	P18	ED9	R18	DV _{DD}	T18	ED13
N19	ED7	P19	V _{SS}	R19	ED11	T19	ED15
N20	ED8	P20	ED10	R20	ED12	T20	ED14
U1	ED22	V1	ED20	W1	V _{SS}	Y1	V _{SS}
U2	ED21	V2	ED19	W2	CV _{DD}	Y2	V _{SS}
U3	ED23	V3	CV _{DD}	W3	DV _{DD}	Y3	ED18
U4	V _{SS}	V4	ED16	W4	ED17	Y4	$\overline{\text{BE}}_2$
U5	DV _{DD}	V5	$\overline{\text{BE}}_3$	W5	V _{SS}	Y5	ARDY
U6	CV _{DD}	V6	$\overline{\text{CE}}_3$	W6	$\overline{\text{CE}}_2$	Y6	EA2
U7	DV _{DD}	V7	EA3	W7	EA4	Y7	DV _{DD}
U8	V _{SS}	V8	EA5	W8	EA6	Y8	EA7
U9	V _{SS}	V9	EA8	W9	DV _{DD}	Y9	EA9
U10	CV _{DD}	V10	EA10	W10	$\overline{\text{AOE}} / \overline{\text{SDRAS}} / \overline{\text{SSOE}}$	Y10	ECLKOUT
U11	CV _{DD}	V11	$\overline{\text{ARE}} / \overline{\text{SDCAS}} / \overline{\text{SSADS}}$	W11	V _{SS}	Y11	ECLKIN
U12	DV _{DD}	V12	$\overline{\text{AWE}} / \overline{\text{SDWE}} / \overline{\text{SSWE}}$	W12	DV _{DD}	Y12	CLKOUT2/(GP[2])
U13	V _{SS}	V13	DV _{DD}	W13	EA11	Y13	V _{SS}
U14	CV _{DD}	V14	EA12	W14	EA13	Y14	EA14
U15	CV _{DD}	V15	DV _{DD}	W15	EA15	Y15	EA16
U16	DV _{DD}	V16	EA17	W16	V _{SS}	Y16	EA18
U17	V _{SS}	V17	$\overline{\text{CE}}_0$	W17	EA19	Y17	DV _{DD}
U18	EA21	V18	CV _{DD}	W18	$\overline{\text{CE}}_1$	Y18	EA20
U19	$\overline{\text{BE}}_1$	V19	DV _{DD}	W19	CV _{DD}	Y19	V _{SS}
U20	V _{SS}	V20	$\overline{\text{BE}}_0$	W20	V _{SS}	Y20	V _{SS}

FIGURE 2. Terminal connections - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 48

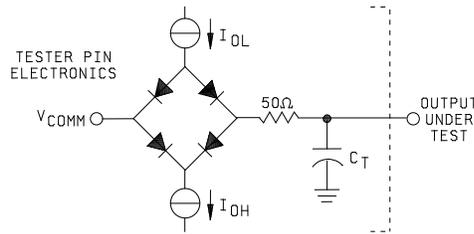


Notes:

1. In addition to fixed point instructions, these functional units execute floating point instructions.
2. Device type 03, 04, 07, 08, 11, 12, 15, 16, 19, and 20 have a software configurable PLL (with x4 through x25 multiplier and /1 through /32 divider) and a PLL controller which is different from the hardware PLL peripheral on the device type 01, 02, 05, 06, 09, 10, 13, 14, 17, and 18.
3. Applicable to the device type 03, 04, 07, 08, 11, 12, 15, 16, 19, and 20 only.

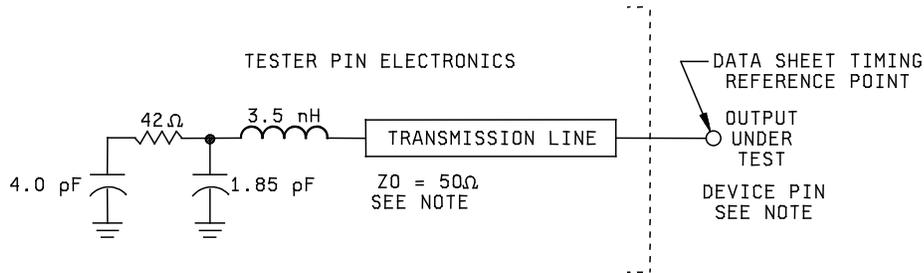
FIGURE 3. Block diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 49



AC timing measurements for device type 01 and 02 only

Where: I_{OL} = 2 mA
 I_{OH} = 2 mA
 V_{comm} = 0.8 V
 C_T = 10-15 pF typical load capacitance



AC timing measurements for device type 03 and 04 only

Note:

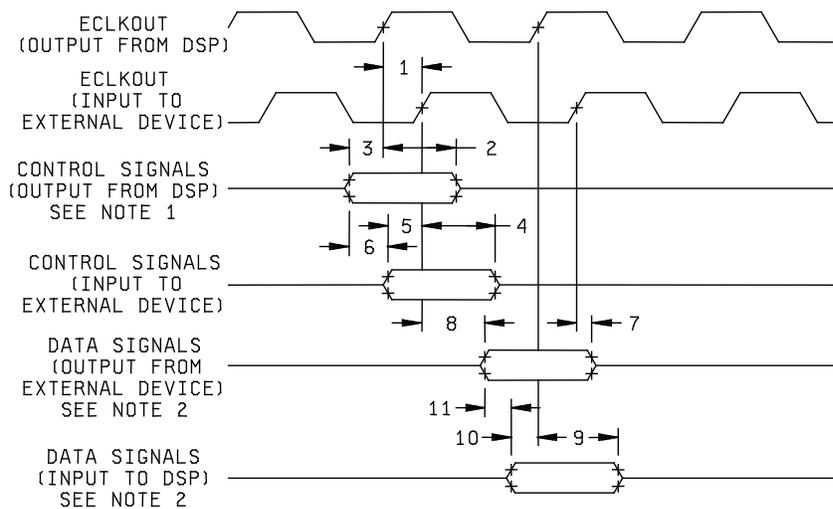
The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts pre nanosecond (4 V/ns) at the device pin.

FIGURE 4. Test load circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 50

No.	Description
1	Clock route delay
2	Minimum DSP hold time
3	Minimum DSP setup time
4	External device hold time requirement
5	External device setup time requirement
6	Control signal route delay
7	External device hold time
8	External device access time
9	DSP hold time requirement
10	DSP setup time requirement
11	Data route delay

Board level timings example



BOARD-LEVEL INPUT/OUTPUT TIMINGS

Notes:

1. Control signals include data for Writes.
2. Data signals are generated during Reads from an external device.

FIGURE 5. Board level input/output timings.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 51

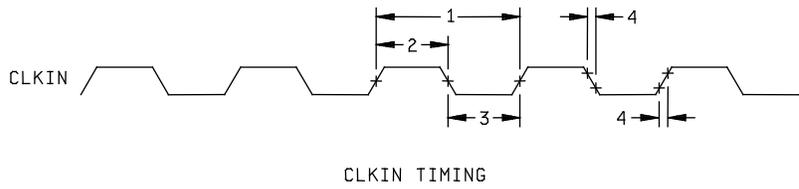


FIGURE 6 Timing waveforms.

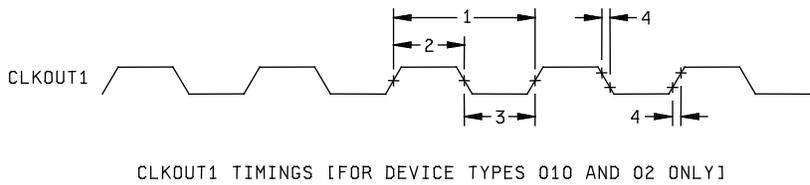


FIGURE 7 Timing waveforms.

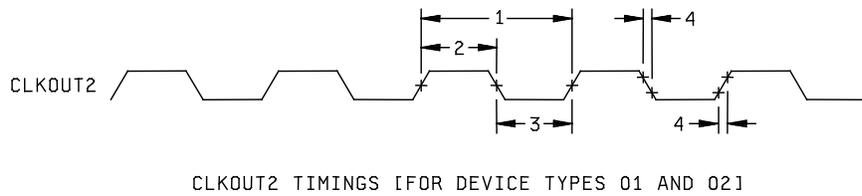


FIGURE 8 Timing waveforms.

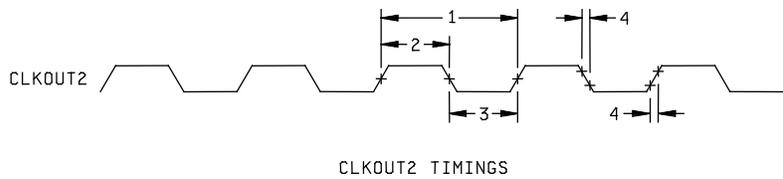


FIGURE 9 Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 52</p>

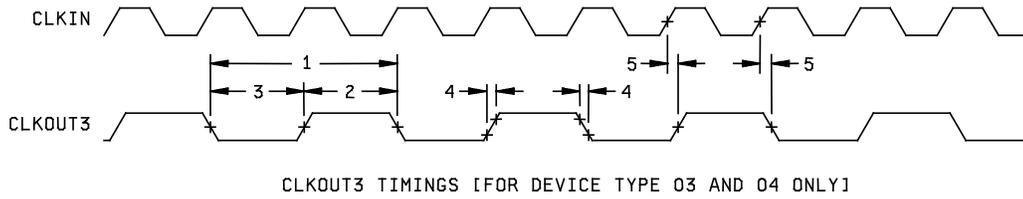


FIGURE 10 Timing waveforms.

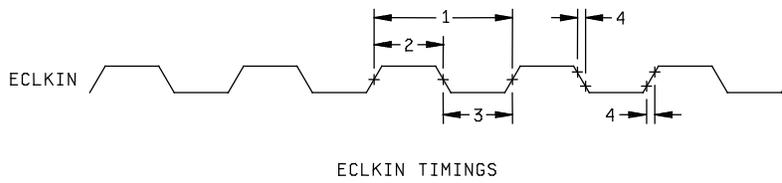


FIGURE 11 Timing waveforms.

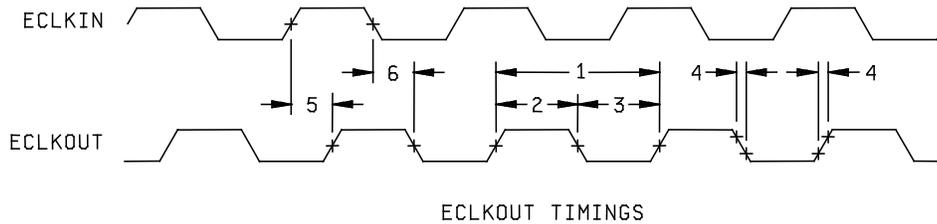
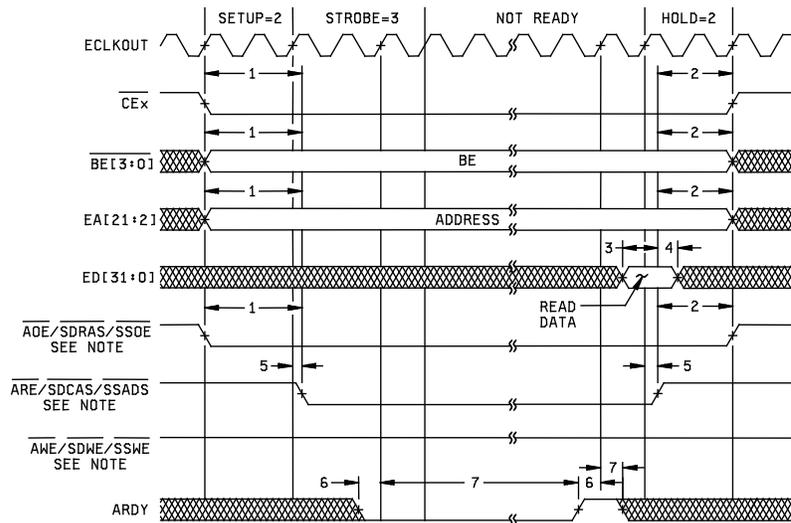
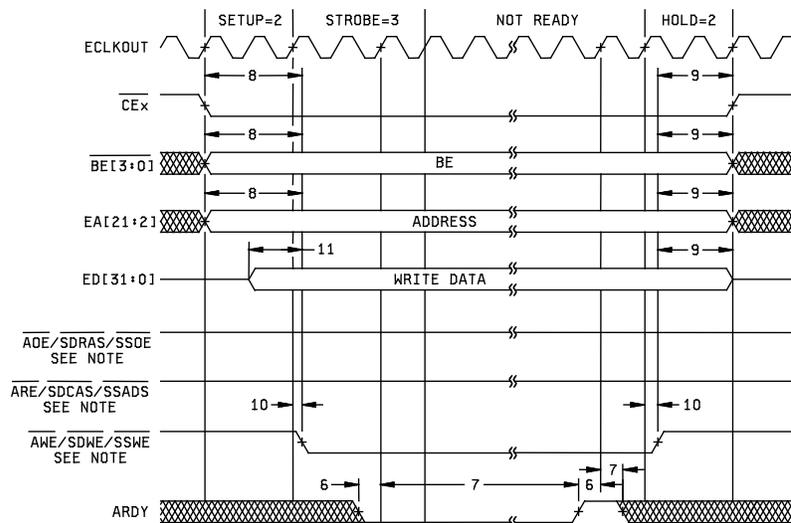


FIGURE 12 Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 53</p>



ASYNCHRONOUS MEMORY READ TIMING



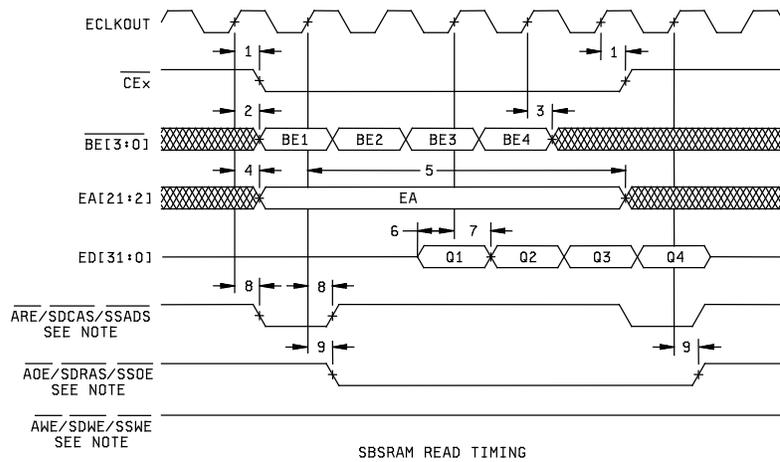
ASYNCHRONOUS MEMORY WRITE TIMING

Note:

\overline{AOE} / \overline{SDRAS} / \overline{SSOE} , \overline{ARE} / \overline{SDCAS} / \overline{SSADS} , and \overline{AWE} / \overline{SDWE} / \overline{SSWE} operate as \overline{AOE} , \overline{ARE} , and \overline{AWE} respectively, during asynchronous memory accesses.

FIGURE 13 Timing waveforms.

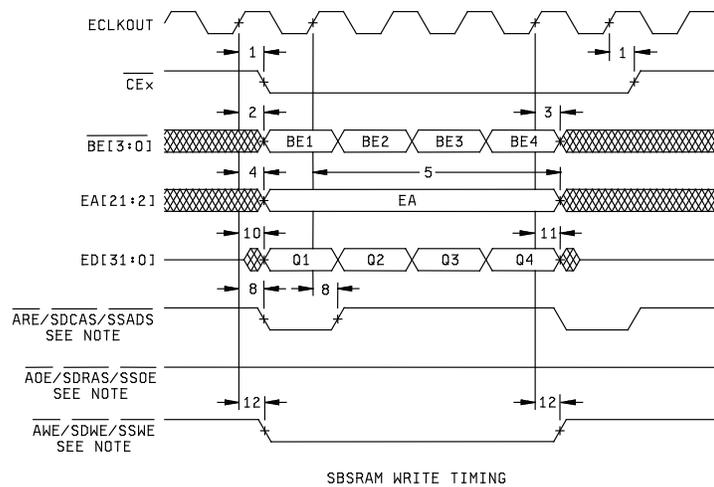
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 54</p>



Note:

$\overline{\text{ARE}} / \overline{\text{SDCAS}} / \overline{\text{SSADS}}$, $\overline{\text{AOE}} / \overline{\text{SDRAS}} / \overline{\text{SSOE}}$, and $\overline{\text{AWE}} / \overline{\text{SDWE}} / \overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$ respectively, during SBSRAM accesses.

FIGURE 14 Timing waveforms.

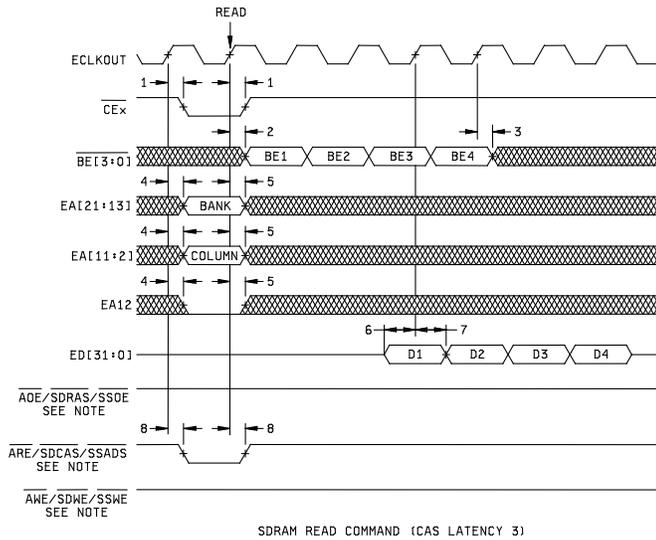


Note:

$\overline{\text{ARE}} / \overline{\text{SDCAS}} / \overline{\text{SSADS}}$, $\overline{\text{AOE}} / \overline{\text{SDRAS}} / \overline{\text{SSOE}}$, and $\overline{\text{AWE}} / \overline{\text{SDWE}} / \overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$ respectively, during SBSRAM accesses.

FIGURE 15 Timing waveforms.

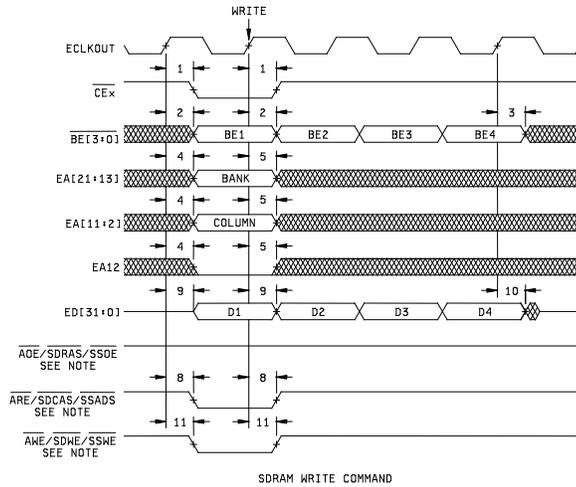
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 55



Note:

$\overline{ARE} / \overline{SDCAS} / \overline{SSADS}$, $\overline{AWE} / \overline{SDWE} / \overline{SSWE}$, and $\overline{AOE} / \overline{SDRAS} / \overline{SSOE}$ operate as \overline{SDCAS} , \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 16 Timing waveforms.

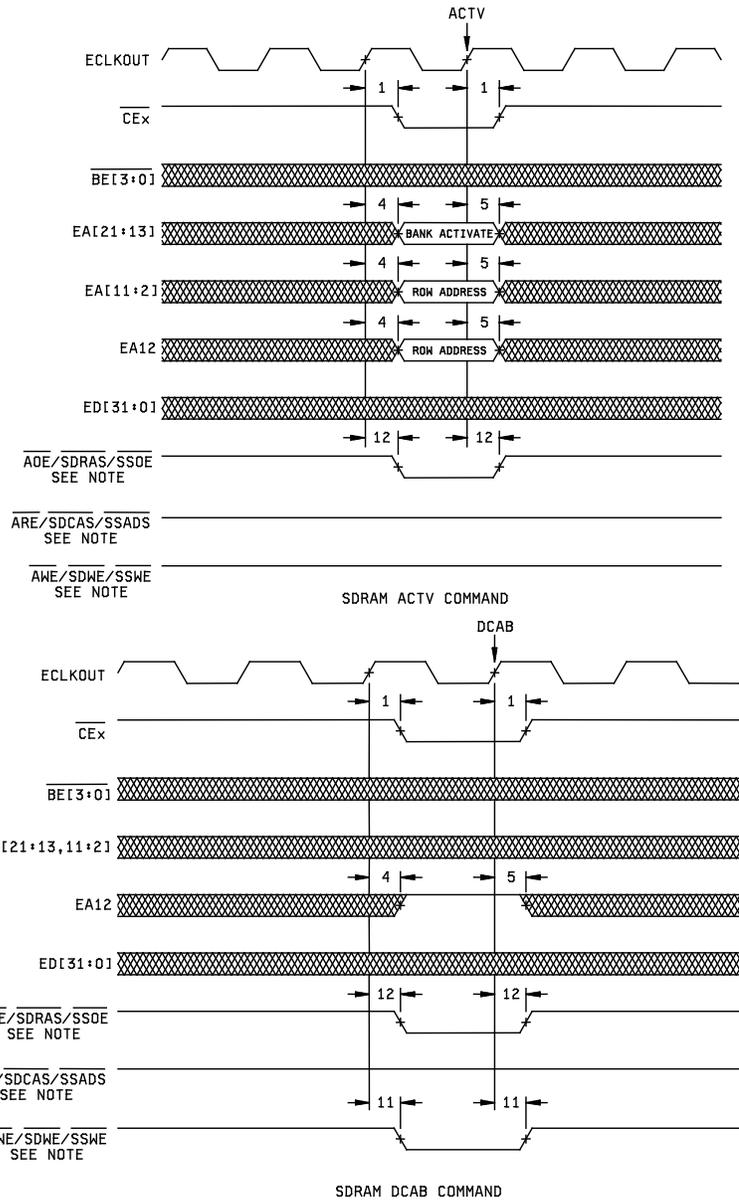


Note:

$\overline{ARE} / \overline{SDCAS} / \overline{SSADS}$, $\overline{AWE} / \overline{SDWE} / \overline{SSWE}$, and $\overline{AOE} / \overline{SDRAS} / \overline{SSOE}$ operate as \overline{SDCAS} , \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 17 Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 56

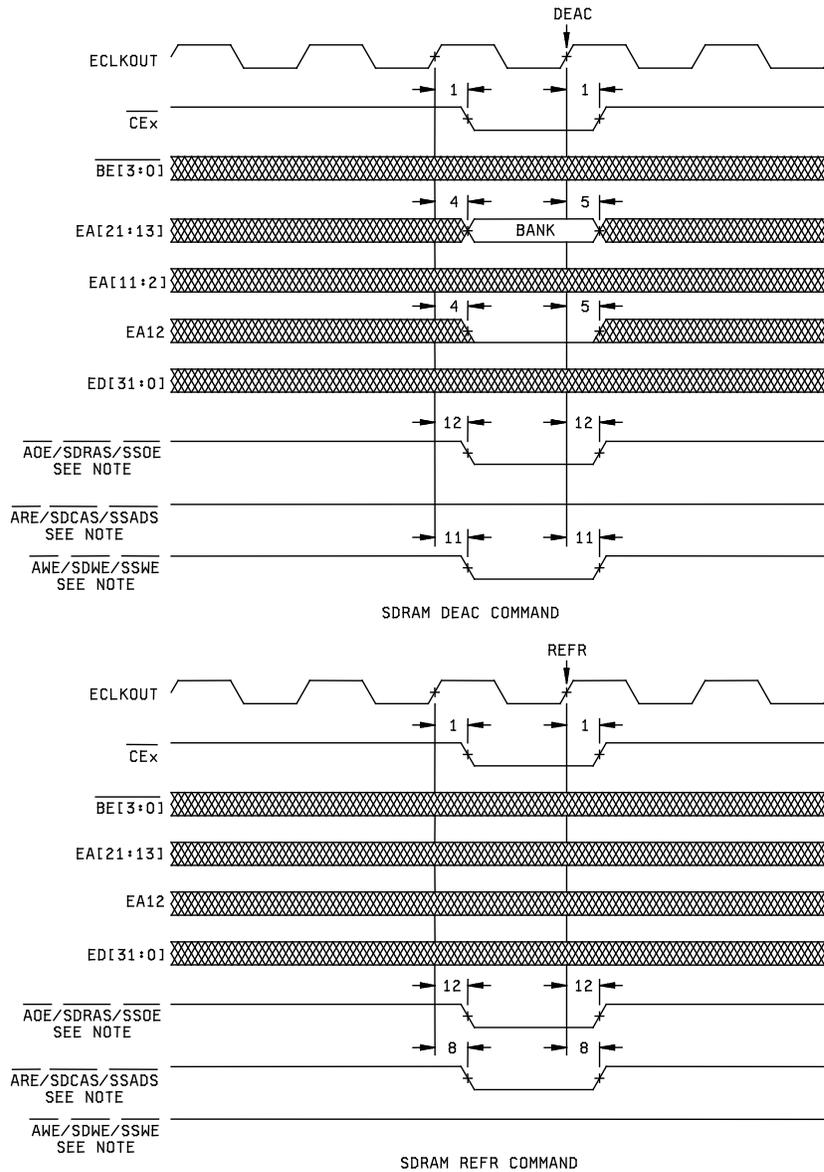


Note:

$\overline{\text{ARE}} / \overline{\text{SDCAS}} / \overline{\text{SSADS}}$, $\overline{\text{AWE}} / \overline{\text{SDWE}} / \overline{\text{SSWE}}$, and $\overline{\text{AOE}} / \overline{\text{SDRAS}} / \overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$ respectively, during SDRAM accesses.

FIGURE 18 Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 57</p>

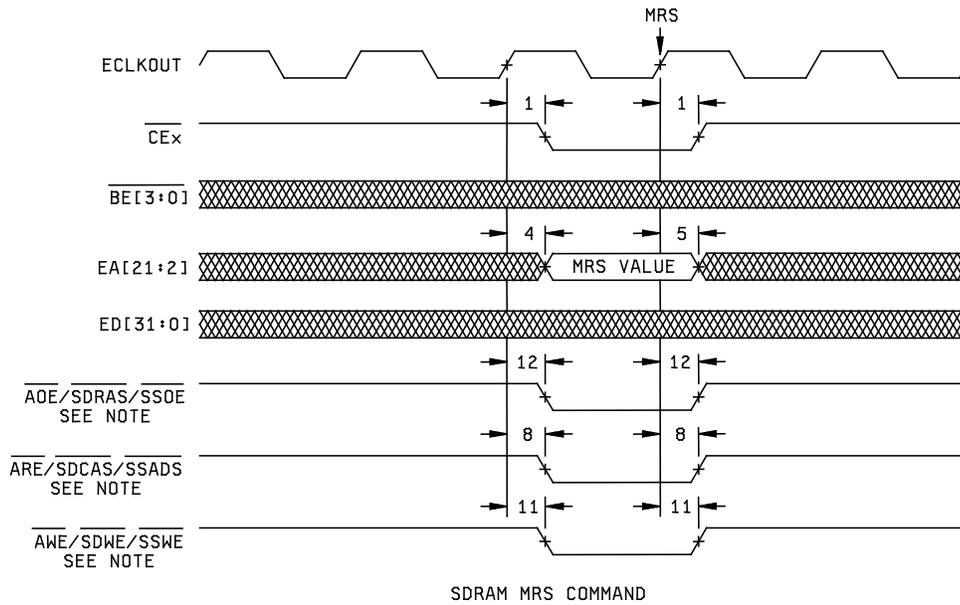


Note:

$\overline{\text{AOE}} / \overline{\text{SDRAS}} / \overline{\text{SSOE}}$, $\overline{\text{ARE}} / \overline{\text{SDCAS}} / \overline{\text{SSADS}}$, $\overline{\text{AWE}} / \overline{\text{SDWE}} / \overline{\text{SSWE}}$, and $\overline{\text{AOE}} / \overline{\text{SDRAS}} / \overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$ respectively, during SDRAM accesses.

FIGURE 19 Timing waveforms.

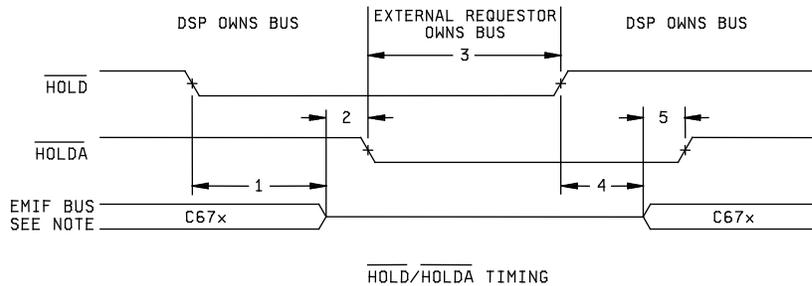
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 58</p>



Note:

$\overline{ARE} / \overline{SDCAS} / \overline{SSADS}$, $\overline{AWE} / \overline{SDWE} / \overline{SSWE}$, and $\overline{AOE} / \overline{SDRAS} / \overline{SSOE}$ operate as \overline{SDCAS} , \overline{SDWE} , and \overline{SDRAS} respectively, during SDRAM accesses.

FIGURE 20 Timing waveforms.



Note:

EMIF bus consists of $\overline{CE}[3:0]$, $\overline{BE}[3:0]$, $\overline{ED}[31:0]$, $\overline{EA}[21:2]$, $\overline{ARE} / \overline{SDCAS} / \overline{SSADS}$, $\overline{AOE} / \overline{SDRAS} / \overline{SSOE}$, and $\overline{AWE} / \overline{SDWE} / \overline{SSWE}$.

FIGURE 21 Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 59

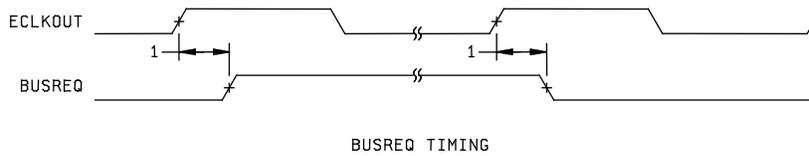
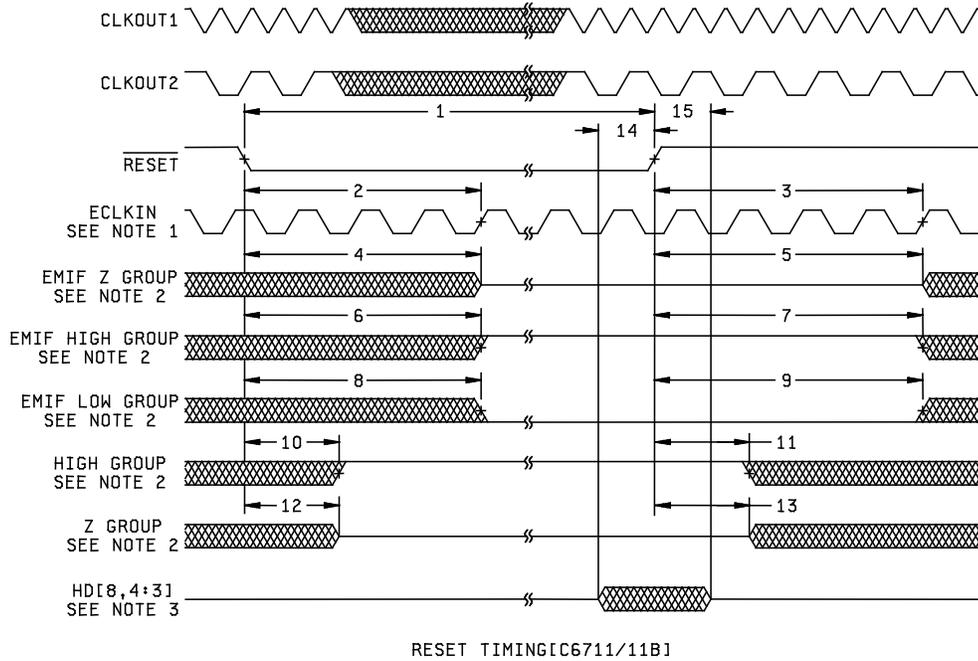


FIGURE 22 Timing waveforms.

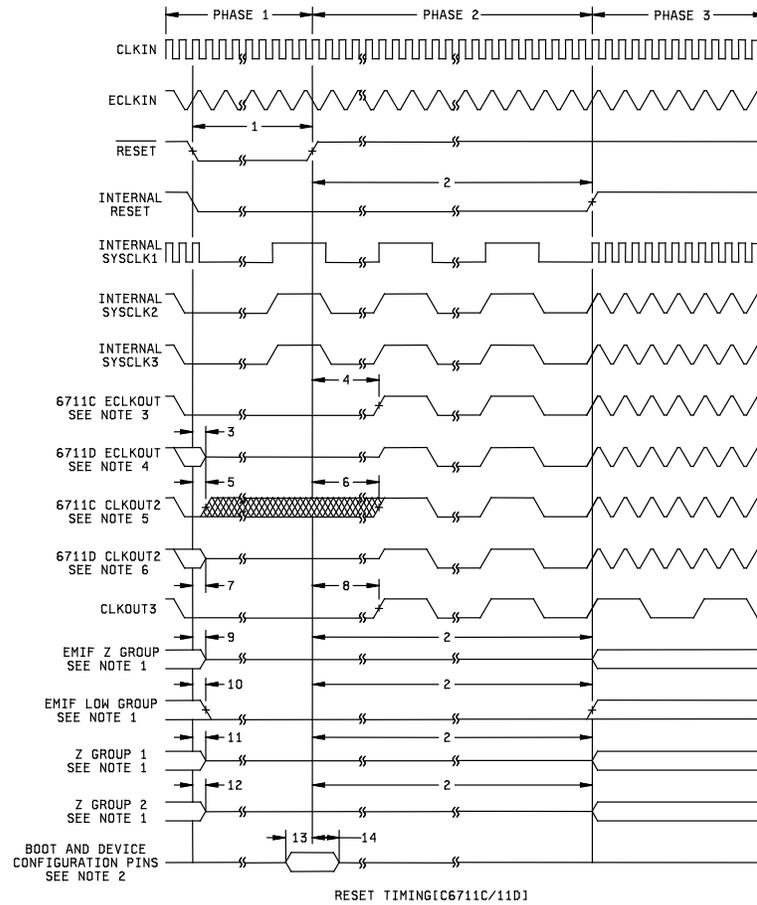


Notes:

1. ECLKIN should be provided during reset in order to drive EMIF signals to the correct reset values. ECKLOUT continues to clock as long as ECLKIN is provided
2. EMIF Z group consists of: $\overline{EA}[21:2]$, $\overline{ED}[31:0]$, $\overline{CE}[3:0]$, $\overline{BE}[3:0]$, $\overline{ARE} / \overline{SDCAS} / \overline{SSADS}$, $\overline{AWE} / \overline{SDWE} / \overline{SSWE}$, and $\overline{AOE} / \overline{SDRAS} / \overline{SSOE}$
 EMIF high group consists of: \overline{HOLDA}
 EMIF low group consists of: \overline{BUSREQ}
 High group consists of: \overline{HRDY} and \overline{HINT}
 Z group consists of: $\overline{HD}[15:0]$, $\overline{CLKX0}$, $\overline{CLKX1}$, $\overline{FSX0}$, $\overline{FSX1}$, $\overline{DX0}$, $\overline{DX1}$, $\overline{CLKR0}$, $\overline{CLKR1}$, $\overline{FSR0}$, $\overline{FSR1}$, $\overline{TOUT0}$, and $\overline{TOUT1}$.
3. $\overline{HD}[8, 4:3]$ are the endianness and boot configuration pins during device reset.

FIGURE 23 Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 60



Notes:

1. EMIF Z group consists of: $\overline{EA}[21:2]$, $\overline{ED}[31:0]$, $\overline{CE}[3:0]$, $\overline{BE}[3:0]$, $\overline{ARE} / \overline{SDCAS} / \overline{SSADS}$, $\overline{AWE} / \overline{SDWE} / \overline{SSWE}$, and $\overline{AOE} / \overline{SDRAS} / \overline{SSOE}$
 EMIF high group consists of: \overline{HOLDA}
 EMIF low group consists of: \overline{BUSREQ}
 High group consists of: \overline{HRDY} and \overline{HINT}
 Z group consists of: $\overline{HD}[15:0]$, $\overline{CLKX0}$, $\overline{CLKX1}$, $\overline{FSX0}$, $\overline{FSX1}$, $\overline{DX0}$, $\overline{DX1}$, $\overline{CLKR0}$, $\overline{CLKR1}$, $\overline{FSR0}$, $\overline{FSR1}$, $\overline{TOUT0}$, and $\overline{TOUT1}$.
2. Boot and device configurations consist of $\overline{HD}[8, 4:3]$.
3. ECLKOUT for device type 03, 07, 11, 15, 19
4. ECLKOUT for device type 04, 08, 12, 16, 20
5. CLKOUT2 for device type 03, 07, 11, 15, 19
6. CLKOUT2 for device type 04, 08, 12, 16, 20

FIGURE 24 Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 61

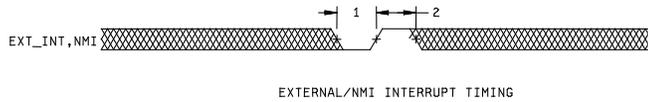
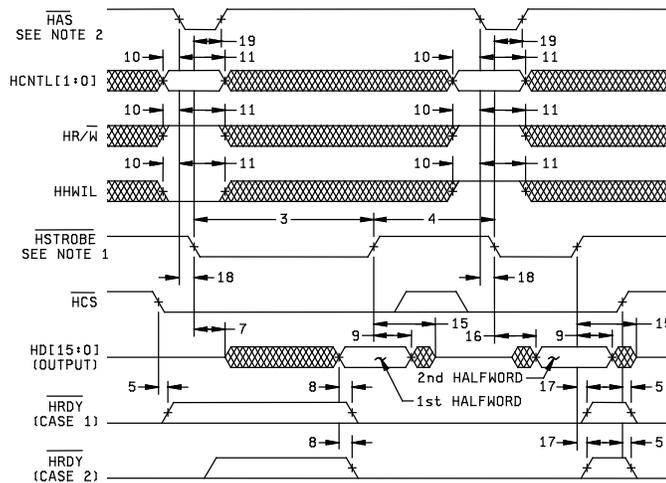
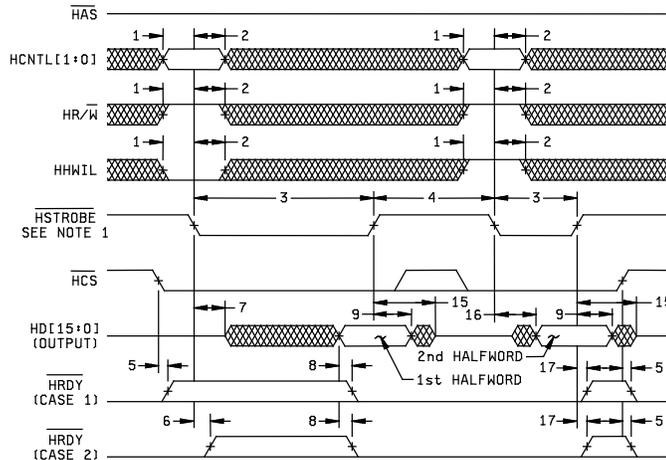


FIGURE 25 Timing waveforms.

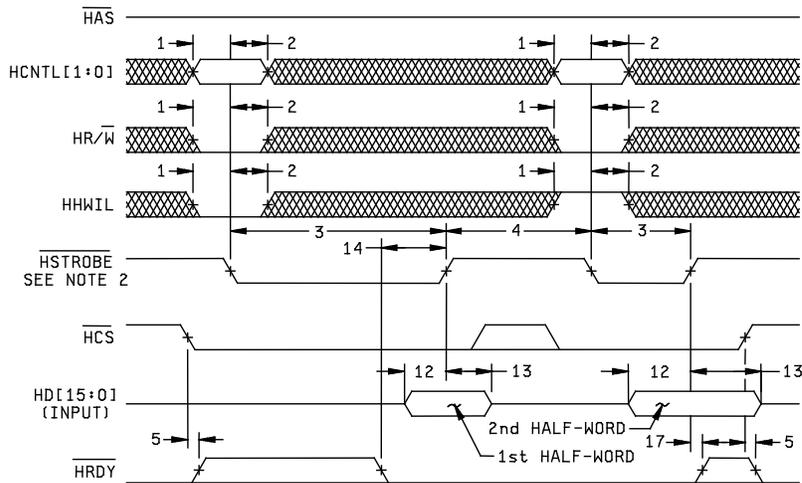


Notes:

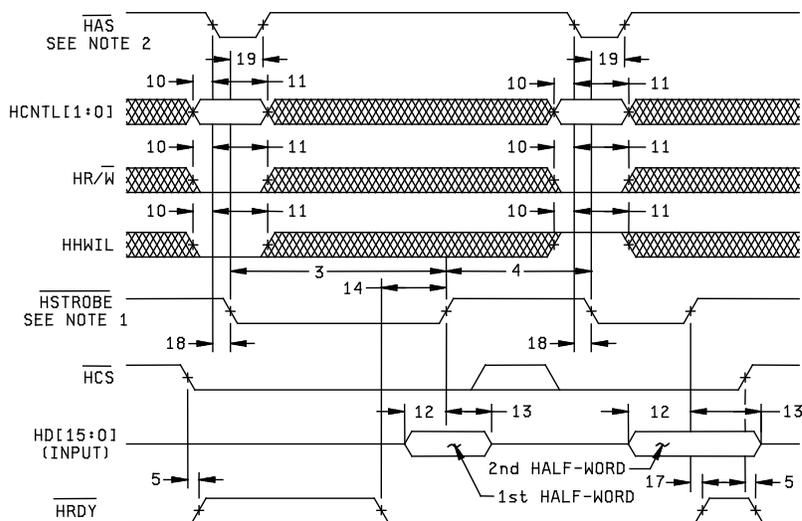
1. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$.
2. For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.

FIGURE 26 Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04753
		REV C	PAGE 62



HPI WRITE TIMING (HAS NOT USED, TIED HIGH)



HPI WRITE TIMING (HAS USED)

Notes:

1. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$.
2. For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.

FIGURE 27 Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 63</p>

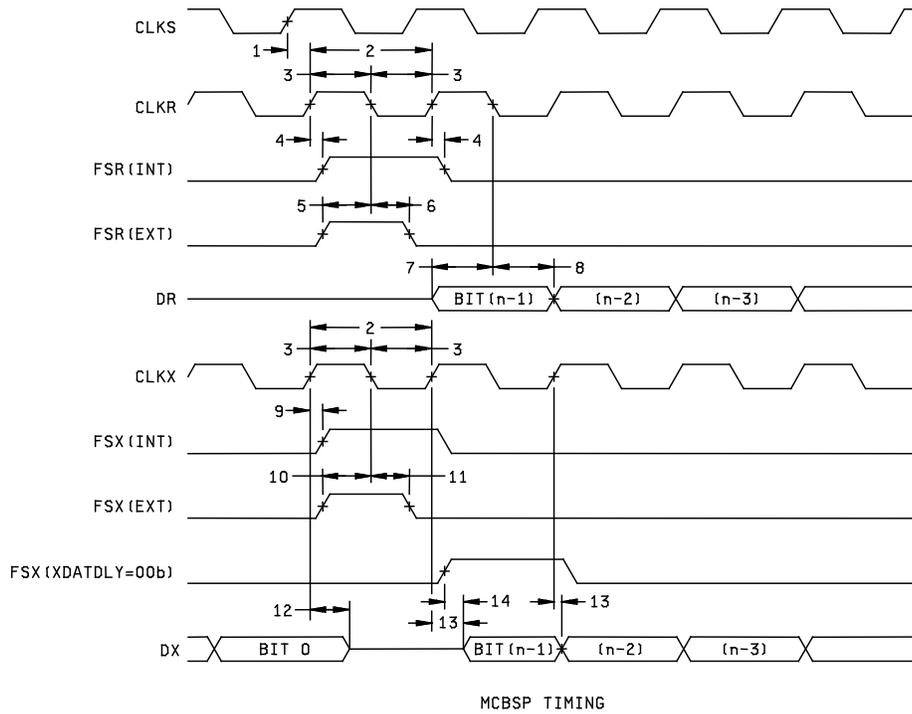


FIGURE 28 Timing waveforms.

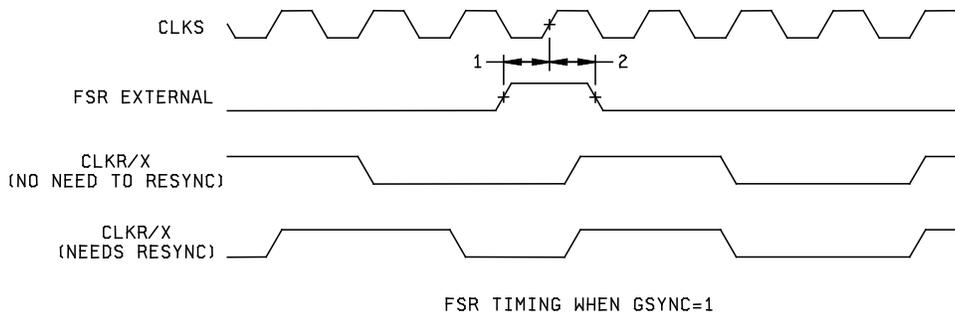


FIGURE 29 Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
		<p>REV C</p>	<p>PAGE 64</p>

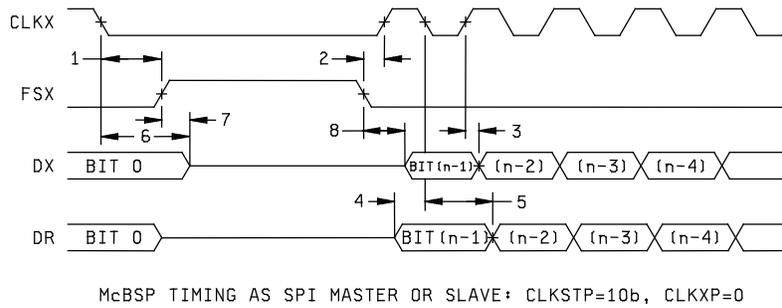


FIGURE 30. Timing waveforms.

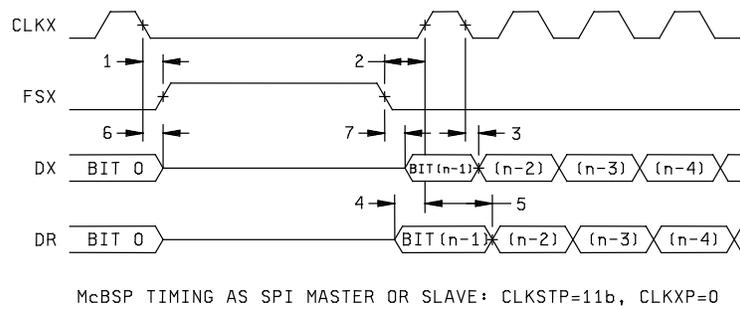


FIGURE 31. Timing waveforms.

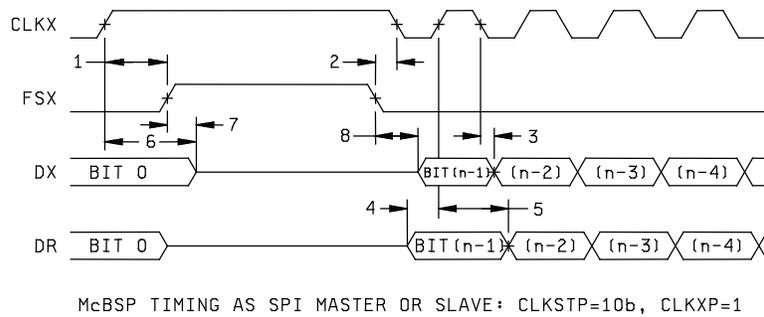


FIGURE 32. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
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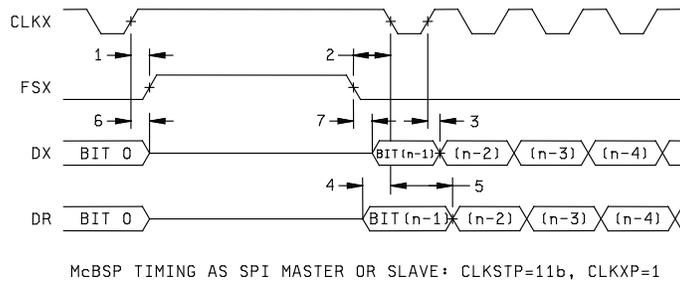


FIGURE 33. Timing waveforms.

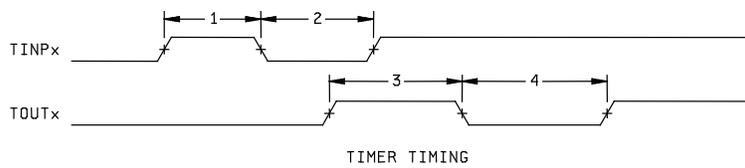


FIGURE 34. Timing waveforms.

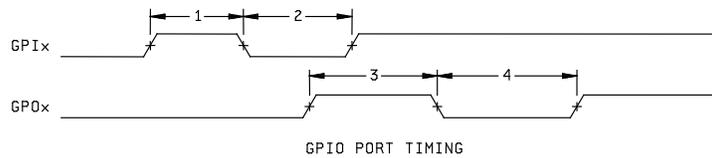


FIGURE 35. Timing waveforms.

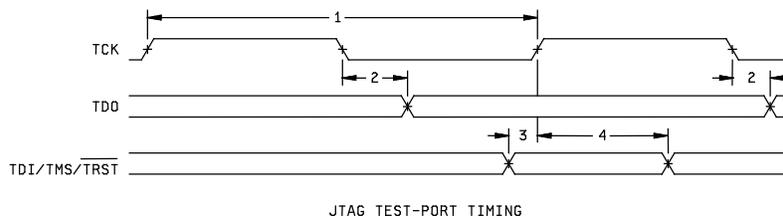


FIGURE 36. Timing waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04753</p>
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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/04753-01XE	<u>2/</u>	SM32C6711GFNA16EP
V62/04753-01YA	<u>2/</u>	SM32C6711GDPA16EP
V62/04753-02XE	<u>2/</u>	SM32C6711BGFNA16EP
V62/04753-02YA	<u>2/</u>	SM32C6711BGDPA16EP
V62/04753-03XE	<u>2/</u>	SM32C6711CGFNA16EP
V62/04753-03YA	<u>2/</u>	SM32C6711CGDPA16EP
V62/04753-04XE	<u>2/</u>	SM32C6711DGFNA16EP
V62/04753-04YA	01295	SM32C6711DGDPA16EP
V62/04753-05XE	<u>2/</u>	SM32C6711GFNA10EP
V62/04753-05YA	<u>2/</u>	SM32C6711GDPA10EP
V62/04753-06XE	<u>2/</u>	SM32C6711BGFNA10EP
V62/04753-06YA	<u>2/</u>	SM32C6711BGDPA10EP
V62/04753-07XE	<u>2/</u>	SM32C6711CGFNA10EP
V62/04753-07YA	<u>2/</u>	SM32C6711CGDPA10EP
V62/04753-08XE	<u>2/</u>	SM32C6711DGFNA10EP
V62/04753-08YA	<u>2/</u>	SM32C6711DGDPA10EP

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Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/04753-09XE	<u>2/</u>	SM32C6711GFNA15EP
V62/04753-09YA	<u>2/</u>	SM32C6711GDPA15EP
V62/04753-10XE	<u>2/</u>	SM32C6711BGFNA15EP
V62/04753-10YA	<u>2/</u>	SM32C6711BGDPA15EP
V62/04753-11XE	<u>2/</u>	SM32C6711CGFNA15EP
V62/04753-11YA	<u>2/</u>	SM32C6711CGDPA15EP
V62/04753-12XE	<u>2/</u>	SM32C6711DGFNA15EP
V62/04753-12YA	<u>2/</u>	SM32C6711DGDPA15EP
V62/04753-13XE	<u>2/</u>	SM32C6711GFNA20EP
V62/04753-13YA	<u>2/</u>	SM32C6711GDPA20EP
V62/04753-14XE	<u>2/</u>	SM32C6711BGFNA20EP
V62/04753-14YA	<u>2/</u>	SM32C6711BGDPA20EP
V62/04753-15XE	<u>2/</u>	SM32C6711CGFNA20EP
V62/04753-15YA	<u>2/</u>	SM32C6711CGDPA20EP
V62/04753-16XE	<u>2/</u>	SM32C6711DGFNA20EP
V62/04753-16YA	01295	SM32C6711DGDPI20EP
V62/04753-17XE	<u>2/</u>	SM32C6711GFNA25EP
V62/04753-17YA	<u>2/</u>	SM32C6711GDPA25EP
V62/04753-18XE	<u>2/</u>	SM32C6711BGFNA25EP
V62/04753-18YA	<u>2/</u>	SM32C6711BGDPA25EP
V62/04753-19XE	<u>2/</u>	SM32C6711CGFNA25EP
V62/04753-19YA	<u>2/</u>	SM32C6711CGDPA25EP
V62/04753-20XE	<u>2/</u>	SM32C6711DGFNA25EP
V62/04753-20YA	<u>2/</u>	SM32C6711DGDPA25EP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ Not yet available from a source of supplied.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243
Point of contact: U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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