REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-09-16	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-10-24	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - DRH	23-05-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																							
REV																							
SHEET																							
REV	C	C	C	C	C	C	C	C	C	C													
SHEET	1	2	3	4	5	6	7	8	9	10													

PMIC N/A

Original date of drawing

YY-MM-DD

04-07-08

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COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS LOGIC OCTAL D-TYPE FLIP FLOP 3-STATE, POSITIVE EDGE TRIGGERED, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04739
REV C		PAGE 1 OF 10

AMSC N/A

5962-V095-23

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high speed CMOS logic octal D-type flip flop 3-state, positive edge triggered microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04739	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	CD74HCT574-EP	High speed CMOS logic octal D-type flip -flop. 3-state, positive edge triggered

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-013	Plastic small outline package
Y	20	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC})	-0.5 V to +7.0 V 2/
Input clamp current, (I_{IK}) (V_I < -0.5 or V_I > V_{CC} + 0.5 V)	±20 mA
Output clamp current, (I_{OK}) (V_O < -0.5 V or V_O > V_{CC} + 0.5 V)	±20 mA
Drain current per output, (I_O) (V_O > -0.5 V or V_O < V_{CC} + 0.5 V)	±35 mA
Output source or sink current per output, (I_O) (V_O > -0.5 V or V_O < V_{CC} + 0.5 V)	±25 mA
Continuous current through V_{CC} or GND, (I_{CC})	±50 mA
Package thermal impedance (θ_{JA}): 3/	
Case X	58°C/W
Case Y	69°C/W
Maximum junction temperature, (T_J)	150°C
Lead temperature (during soldering):	
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max	300°C
Storage temperature range, (T_{STG})	-65°C to +150°C 4/

1.4 Recommended operating conditions. 4/

Supply voltage, (V_{CC})	+4.5 V to +5.5 V
Minimum high level input voltage, (V_{IH}) (V_{CC} = 4.5 V to 5.5 V)	+2.0 V
Maximum low level input voltage, (V_{IL}) (V_{CC} = 4.5 V to 5.5 V)	+0.8 V
Input voltage, (V_I)	0.0 V to V_{CC}
Output voltage, (V_O)	0.0 V to V_{CC}
Input transition (rise and fall) time, (t_t):	
V_{CC} = 2 V	0 ns to 1000 ns
V_{CC} = 4.5 V	0 ns to 500 ns
V_{CC} = 6 V	0 ns to 400 ns
Operating free air temperature, (T_A)	-40°C to +125°C

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage referenced to GND unless otherwise specified.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions unless otherwise specified		I_O (mA)	V_{CC}	Device type	T_A = 25°C		-40°C ≤ T_A ≤ +125°C		Unit
							Min	Max	Min	Max	
High level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	-0.02	4.5 V	All	4.4		4.4		V
			TTL loads	-6	4.5 V		3.98		3.7		
Low level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	4.5 V			0.1		0.1	
			TTL loads	6	4.5 V			0.26		0.4	
Input current	I_I	$V_I = V_{CC}$ or GND		0	5.5 V			±0.1		±1	µA
High impedance state output current	I_{OZ}	$V_I = V_{IH}$ or V_{IL}, $V_O = V_{CC}$ or GND			6 V			±0.5		±10	
Quiescent supply current	I_{CC}	$V_I = V_{CC}$ or GND		0	5.5 V			8		160	
Quiescent supply current delta	ΔI_{CC}	$V_I = V_{CC} - 2.1V$ 2/			4.5 V to 5.5 V			360		490	
Input capacitance	C_{IN}	C_L = 50 pF						10		10	pF
Output capacitance	C_{OUT}	3-state						20		20	
Maximum clock frequency	f_{max}				4.5 V		30		20		MHz
Clock pulse duration	t_w				4.5 V		16		24		ns
Setup time, data before clock↑	t_{su}				4.5 V		12		18		
Hold time, data after clock↑	t_h				4.5 V		5		5		
Propagation delay time from input CP to output Q	t_{pd}	C_L = 50 pF			4.5 V			33		50	
		C_L = 15 pF			5 V			15 TYP			
Disable time from input $\overline{OE}$ to output Q	t_{dis}	C_L = 50 pF			4.5 V			28		42	
		C_L = 15 pF			5 V			11 TYP			
Enable time from input $\overline{OE}$ to output Q	t_{en}	C_L = 50 pF			4.5 V			30		45	
		C_L = 15 pF			5 V			12 TYP			
Transition time to output Q	t_t	C_L = 50 pF			4.5 V			12		18	
Maximum frequency from input CP	f_{max}	C_L = 15 pF			5 V			60 TYP			MHz
Power dissipation capacitance	C_{pd} 3/	Input t_r, t_f = 6 ns			5 V			47 TYP			pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

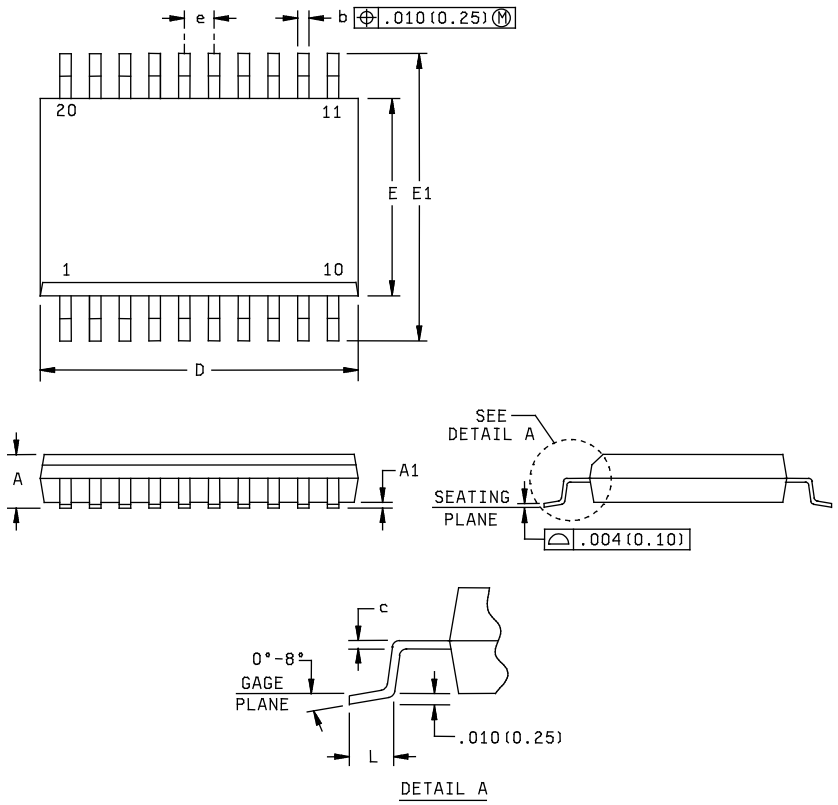
2/ For dual supply systems, theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
HCT input loading

Input	Unit Loads
D0-D7	0.4
CP	0.75
$\overline{OE}$	0.6

Unit loads is ΔI_{CC} limit specified in electrical characteristics table, e.g., 360 µA max at 25°C.

3/ C_{pd} is used to determine the dynamic power consumption (P_D), per package.
$P_D = (C_{PD} \times V_{CC}^2 \times f_I) + \Sigma(C_L \times V_{CC}^2 \times f_O)$ where:
f_I = input frequency f_O = output frequency
C_L = output load capacitance V_{CC} = supply voltage

Case X

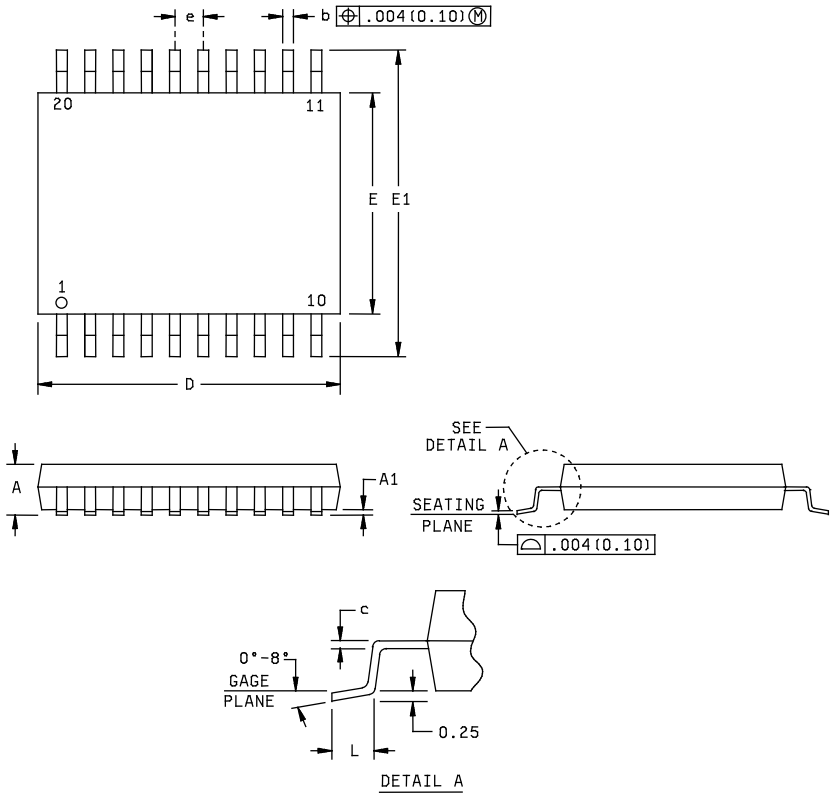


Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.104		2.65	E	.291	.299	7.39	7.59
A1	.004	.012	0.10	0.30	E1	.400	.419	10.15	10.65
b	.014	.020	0.35	0.51	e	.050 BSC		1.27 BSC	
c	.010 NOM		0.25 NOM		L	.016	.050	0.40	1.27
D	.500	.510	12.70	12.95					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
4. Fall within JEDEC MO-013.

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.047		1.20	E	.168	.176	4.30	4.50
A1	.000	.006	0.05	0.15	E1	.242	.258	6.20	6.60
b	.007	.012	0.19	0.30	e	.025 BSC		0.65 BSC	
c	.006 NOM		0.15 NOM		L	.020	.029	0.50	0.75
D	.250	.258	6.40	6.60					

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines – Continued.

Pin No.	Signal name	Pin No.	Signal name
1	$\overline{OE}$	11	CP
2	D0	12	Q7
3	D1	13	Q6
4	D2	14	Q5
5	D3	15	Q4
6	D4	16	Q3
7	D5	17	Q2
8	D6	18	Q1
9	D7	19	Q0
10	GND	20	V_{CC}

FIGURE 2. Terminal connections.

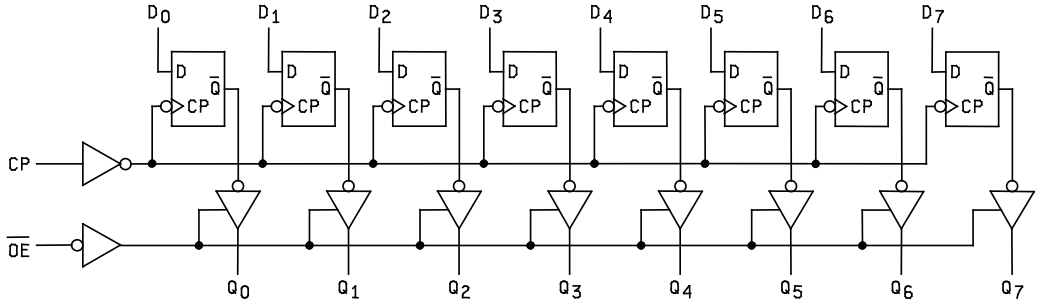
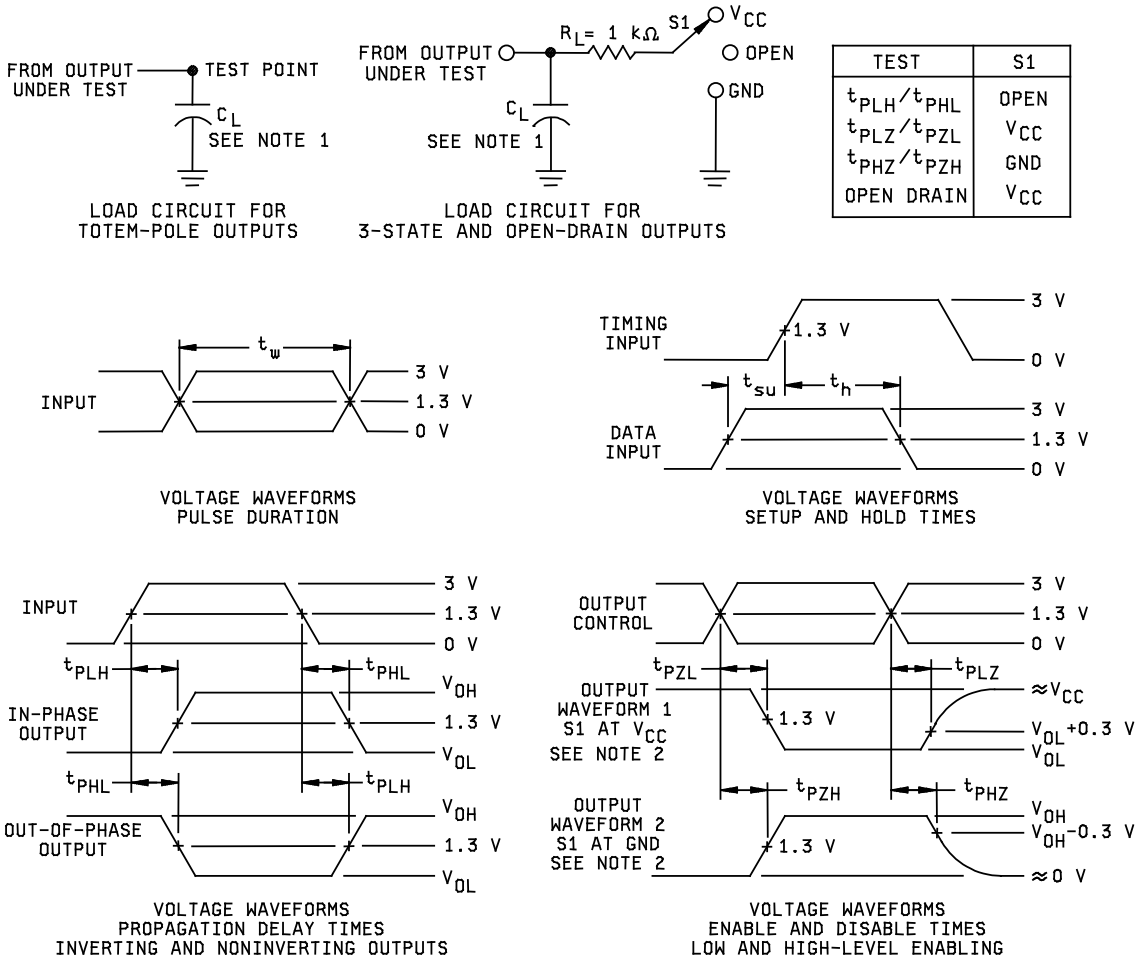


FIGURE 3. Logic diagram.

Inputs			Output
$\overline{OE}$	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High voltage level (steady state)
L = Low voltage level (steady state)
X = Don't care
↑ = Transition from low to high level
Q_0 = Level before indicated steady state conditions were established.
Z = High impedance state

FIGURE 4. Function Table.



NOTES:

1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
4. The outputs are measured one at a time with one transition per measurement.
5. All parameters and waveforms are not applicable to all devices.
6. t_{PLH} and t_{PHL} are the same t_{pd}.
7. t_{PLZ} and t_{PHZ} are the same t_{dis}.
8. t_{PZH} and t_{PZL} are the same t_{en}.

FIGURE 5. Load circuit and voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04739-01XE	01295	CD74HCT574QM96EP	HCT574EP
V62/04739-01YE	01295	CD74HCT574QPWREP	HCT574EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243