REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-09-16	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-10-24	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - DRH	23-05-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C													
SHEET	1	2	3	4	5	6	7	8	9													

PMIC N/A

Original date of drawing

YY-MM-DD

04-07-08

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TITLE
MICROCIRCUIT, DIGITAL, OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04738
REV	C	PAGE 1 OF 9

AMSC N/A

5962-V094-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal bus transceiver with 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04738	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74ABT245B-EP	Octal bus transceiver with 3-state outputs.

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-150	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC}) ..... -0.5 V to +7.0 V
Input voltage range, (V_I) (except I/O ports) ..... -0.5 V to +7.0 V 2/
Voltage range applied to any output in the high impedance or power-off stage, (V_O) ..... -0.5 V to +5.5 V
Current into any output in the low state, (I_O) ..... 96 mA
Input clamp current, (I_{IK}) ($V_I < 0$) ..... -18 mA
Output clamp current, (I_{OK}) ($V_O < 0$) ..... -50 mA
Package thermal impedance, (θ_{JA}) ..... 70°C/W 3/
Storage temperature range, (T_{STG}) ..... -65°C to +150°C 4/

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1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may exceeded if the input and output current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.

1.4 Recommended operating conditions. 5/

Supply voltage, (V_{CC})	+4.5 V to +5.5 V
Minimum high level input voltage, (V_{IH})	+2.0 V
Maximum low level input voltage, (V_{IL})	+0.8 V
Input voltage, (V_I)	0.0 V to V_{CC}
Maximum high level output current, (I_{OH})	-24.0 mA
Maximum low level output current, (I_{OL})	+32.0 mA
Maximum input transition rise or fall rate, ($\Delta t/\Delta v$)	5 ns/V
Operating free air temperature, (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions unless otherwise specified	V_{CC}	Device type	T_A = 25°C		-55°C to +125°C		Unit
					Min	Max	Min	Max	
	V_{IK}	I_I = - 18 mA	4.5 V	All		-1.2		-1.2	V
High level output voltage	V_{OH}	I_{OH} = -3 mA	4.5 V		2.5		2.5		V
		I_{OH} = -3 mA	5.0 V		3		3		
		I_{OH} = -24 mA	4.5 V		2		2		
Low level output voltage	V_{OL}	I_{OL} = 32 mA	4.5 V			0.55		0.55	
Input current, Control inputs	I_I	V_I = V_{CC} or GND	0 V to 5.5 V			±1		±1	µA
Input current, A or B ports			2.1 V to 5.5 V			±20		±100	
High impedance state output current -Power up	I_{OZPU}	V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X	0 V to 2.1 V			±50		±50	
High impedance state output current -Power down	I_{OZPD}	V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X	2.1 V to 0 V			±50		±50	
High impedance state output current	I_{OZH} 2/	V_O = 2.7 V, $\overline{OE} \geq$ 2 V	2.1 V to 5.5 V			10		10	
Low impedance state output current	I_{OZL} 2/	V_O = 0.5 V, $\overline{OE} \geq$ 2 V	2.1 V to 5.5 V			-10		-10	
Input/output power off leakage current	I_{off}	V_I or $V_O \leq$ 4.5 V	0 V			±100			
	I_{CEX}	V_O = 5.5 V, Outputs high	5.5 V			50		50	
Output current	I_O 3/	V_O = 2.5 V	5.5 V		-50	-180	-50	-180	mA
Quiescent supply current	I_{CC}	I_O = 0, V_I = V_{CC} or GND, Outputs high	5.5 V			250		250	µA
		I_O = 0, V_I = V_{CC} or GND, Outputs low	5.5 V			30		30	mA
		I_O = 0, V_I = V_{CC} or GND, Outputs disabled	5.5 V			250		250	µA
Quiescent supply current delta, Data inputs	ΔI_{CC}	One input at 3.4 V, other inputs at V_{CC} or GND, Output enabled	5.5 V			1.5		1.5	mA
		One input at 3.4 V, other inputs at V_{CC} or GND, Outputs disabled	5.5 V			50		50	µA
Quiescent supply current delta, Control inputs		One input at 3.4 V, other inputs at V_{CC} or GND	5.5 V			1.5		1.5	mA
Input capacitance, Control inputs	C_i	V_I = 2.5 V or 0.5 V	5.0 V			4 TYP			pF
Input/output capacitance, A or B ports	C_{iO}	V_O = 2.5 V or 0.5 V	5.0 V			8 TYP			

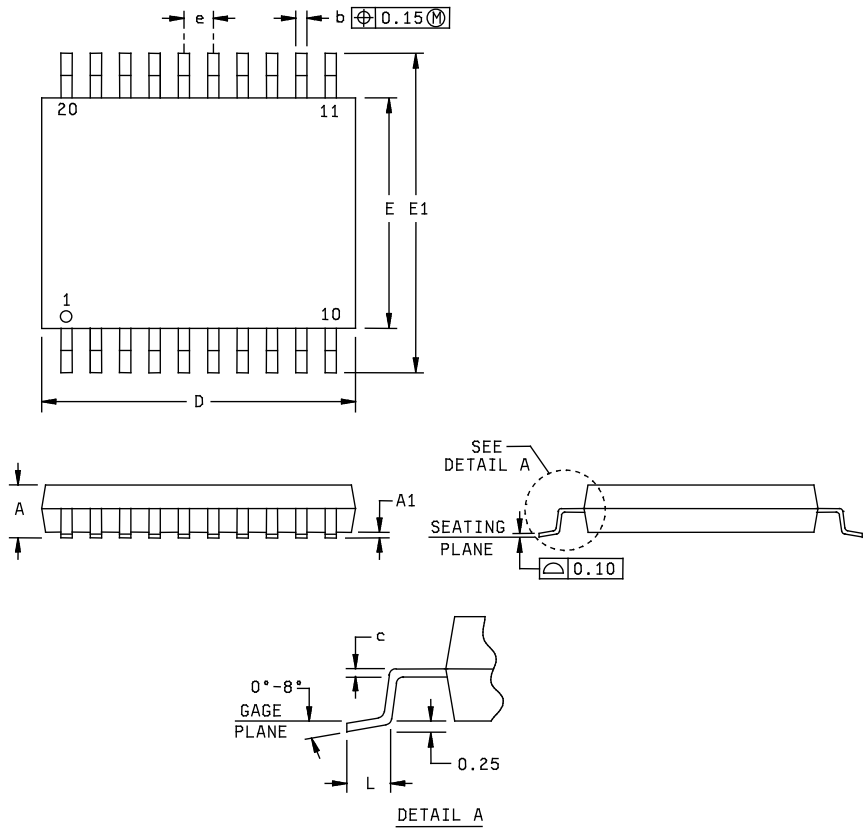
See footnote at end of the table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	V_{CC} = 5.0 V, T_A = 25°C		-55°C to +125°C		Unit
				Min	Max	Min	Max	
Propagation delay time, high to low, from input A or B to output B or A	t_{PLH}	C_L = 50 pF	All	1	3.2	0.8	3.8	ns
Propagation delay time, low to high, from input A or B to output B or A	t_{PHL}			1	3.5	1	4.2	
Enable time to high level from input $\overline{OE}$ to outputs A or B	t_{PZH}			2	4.5	1.2	6.2	
Enable time to low level from input $\overline{OE}$ to outputs A or B	t_{PZL}			1.9	5.3	1.3	6.8	
Disable time from high level, from input $\overline{OE}$ to outputs A or B	t_{PHZ}			2.2	5.4	2.2	6.1	
Disable time from low level, from input $\overline{OE}$ to outputs A or B	t_{PLZ}			1.5	4	1.0	4.9	
Outputs skew time	$t_{sk(o)}$				0.5			

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ The parameters I_{OZH} and I_{OZL} include the input leakage current.
3/ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
4/ This is increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.078		2.0	E	.195	.219	5.00	5.60
A1	.000		0.05		E1	.289	.320	7.40	8.20
b	.009	.015	0.22	0.38	e	.025 BSC		0.65 BSC	
c	.004	.010	0.09	0.25	L	.021	.037	0.55	0.95
D	.270	.293	6.90	7.50					

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Fall within JEDEC MO-150.

FIGURE 1. Case outlines.

Pin No.	Signal name	Pin No.	Signal name
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{OE}$
10	GND	20	V_{CC}

FIGURE 2. Terminal connections.

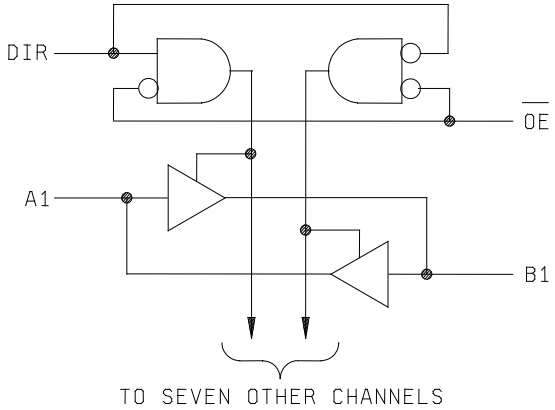
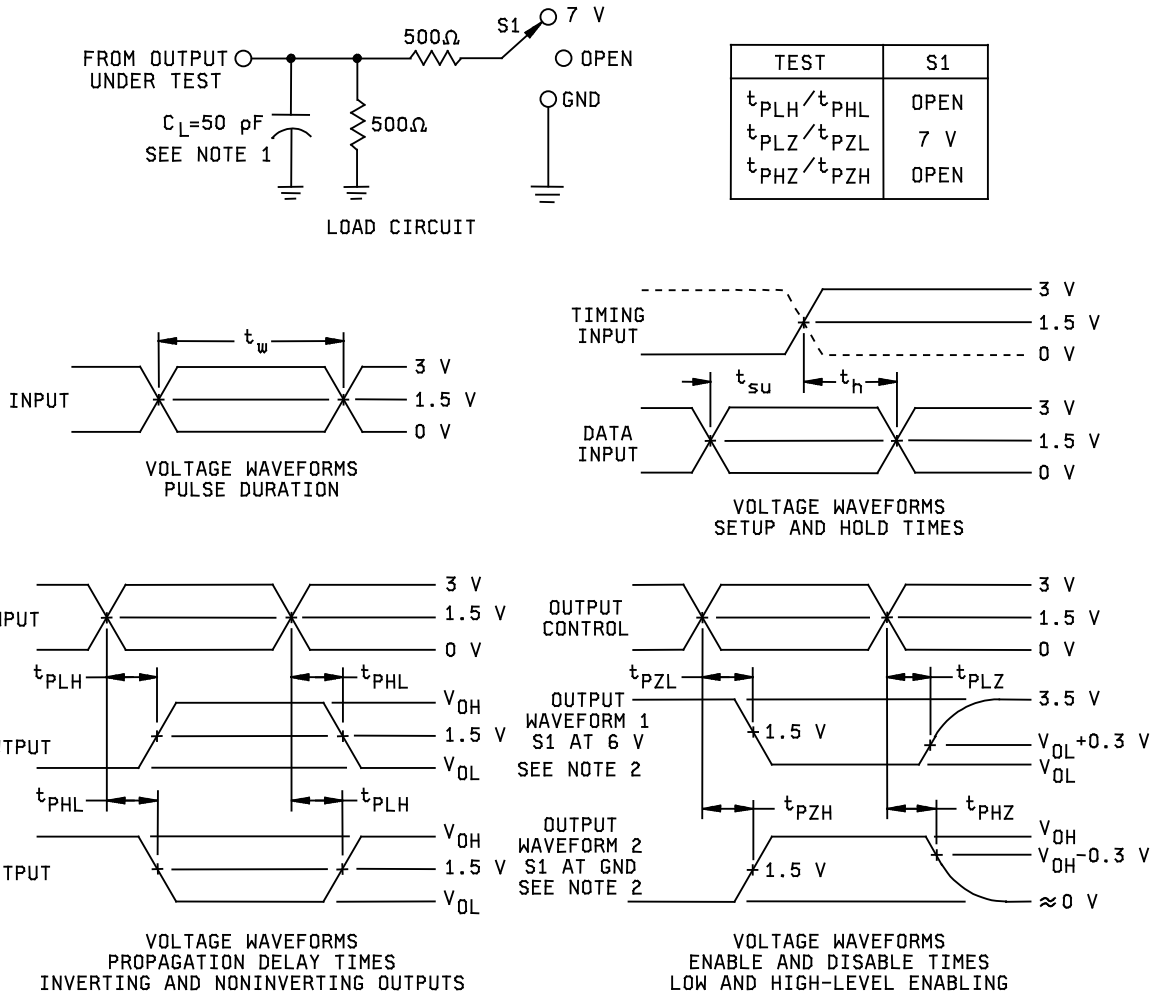


FIGURE 3. Logic diagram.

Inputs		Operation
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

FIGURE 4. Function Table.



NOTES:

1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one transition per measurement.
5. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04738-01XE	01295	SN74ABT245BMDBREP	ABT245MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243