

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-09-16	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-10-24	Thomas M. Hess



CURRENT DESIGN ACTIVITY CAGE CODE 16236
 HAS CHANGED NAMES TO:
 DLA LAND AND MARITIME
 COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B								
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PMIC N/A	PREPARED BY Phu H. Nguyen	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY MM DD 04-07-08	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, DIGITAL, OCTAL BUS TRANSCIVER WITH 3-STATE OUTPUTS, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/04737
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal bus transceiver with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/04737</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC245A-EP	Octal bus transceiver with 3-state outputs.

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V _{CC})	-0.5 V to +6.5 V
Input voltage range, (V _I)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high impedance or power-off stage, (V _O)	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or slow state, (V _O)	-0.5 V to V _{CC} + 0.5 V 2/ 3/
Input clamp current, (I _{IK}) (V _I < 0)	-50 mA
Output clamp current, (I _{OK}) (V _O < 0)	-50 mA
Continuous output current, (I _O)	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance (θ _{JA})	83°C/W 4/
Storage temperature range, (T _{STG}).....	-65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output negative voltage ratings may exceeded if the input and output current ratings are observed.

3/ The value of V_{CC} is provided in the recommended operating conditions table.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 5/

		T _A = 25°C		-40°C to +85°C		Unit
		Min	Max	Min	Max	
Supply voltage, (V _{CC})	Operating	1.65	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
High level input voltage, (V _{IH})	V _{CC} = 1.65 V to 1.95 V	0.65 x V _{CC}		0.65 x V _{CC}		
	V _{CC} = 2.3 V to 2.7 V	1.7		1.7		
	V _{CC} = 2.7 V to 3.6 V	2		2		
Low level input voltage, (V _{IL})	V _{CC} = 1.65 V to 1.95 V		0.35 x V _{CC}		0.35 x V _{CC}	
	V _{CC} = 2.3 V to 2.7 V		0.7		0.7	
	V _{CC} = 2.7 V to 3.6 V		0.8		0.8	
Input voltage, (V _I)		0	5.5	0	5.5	
Output voltage, (V _O)		0	V _{CC}	0	V _{CC}	
High level output current, (I _{OH})	V _{CC} = 1.65		-4		-4	mA
	V _{CC} = 2.3 V		-8		-8	
	V _{CC} = 2.7 V		-12		-12	
	V _{CC} = 3 V		-24		-24	
Low level output current, (I _{OL})	V _{CC} = 1.65		4		4	
	V _{CC} = 2.3 V		8		8	
	V _{CC} = 2.7 V		12		12	
	V _{CC} = 3 V		24		24	
Input transition rise or fall rate, (Δt/Δv)			10		10	ns/V

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JE51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions unless otherwise specified	V _{CC}	T _A = 25°C		-40°C to +85°C		Unit
					Min	Max	Min	Max	
High level output voltage		V _{OH}	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.2		V _{CC} - 0.2		V
			I _{OH} = -4 mA	1.65 V	1.29		1.2		
			I _{OH} = -8 mA	2.3 V	1.9		1.7		
			I _{OH} = -12 mA	2.7 V	2.2		2.2		
				3 V	2.4		2.4		
I _{OH} = -24 mA	3 V	2.3		2.2					
Low level output voltage		V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V		0.1		0.2	
			I _{OL} = 4 mA	1.65 V		0.24		0.45	
			I _{OL} = 8 mA	2.3 V		0.3		0.7	
			I _{OL} = 12 mA	2.7 V		0.4		0.4	
			I _{OL} = 24 mA	3 V		0.55		0.55	
Input current	Control inputs	I _I	V _I = 0 to 5.5 V	3.6 V		±1		±5	μA
Input/output power off leakage current		I _{off}	V _I or V _O = 5.5 V	0		±1		±10	μA
High impedance state output current		I _{OZ} 2/	V _O = 0 to 5.5 V	3.6 V		±1		±10	μA
Quiescent supply current		I _{CC}	V _I = 5.5 V or GND	3.6 V		1		10	μA
			3.6 V ≤ V _I ≤ 5.5 V 3/						
Quiescent supply current delta		ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500		500	μA
Input capacitance	Control inputs	C _i	V _I = V _{CC} or GND,	3.3 V	4 Typ				pF
Input/output capacitance	A or B ports	C _{IO}		3.3 V	5.5 Typ				
Propagation delay time from input A or B to output B or A		t _{pd}		1.8 V ±0.15 V	1	12.2	1	12.7	ns
				2.5 V ±0.2 V	1	7.8	1	8.3	
				2.7 V	1	7.1	1	7.3	
				3.3 V ±0.3 V	1.5	6.1	1.5	6.3	
Enable time from input \overline{OE} to output A or B		t _{en}		1.8 V ±0.15 V	1	14.8	1	15.3	
				2.5 V ±0.2 V	1	10	1	10.5	
				2.7 V	1	9.3	1	9.5	
				3.3 V ±0.3 V	1.5	8.3	1.5	8.5	

See footnote at end of the table.

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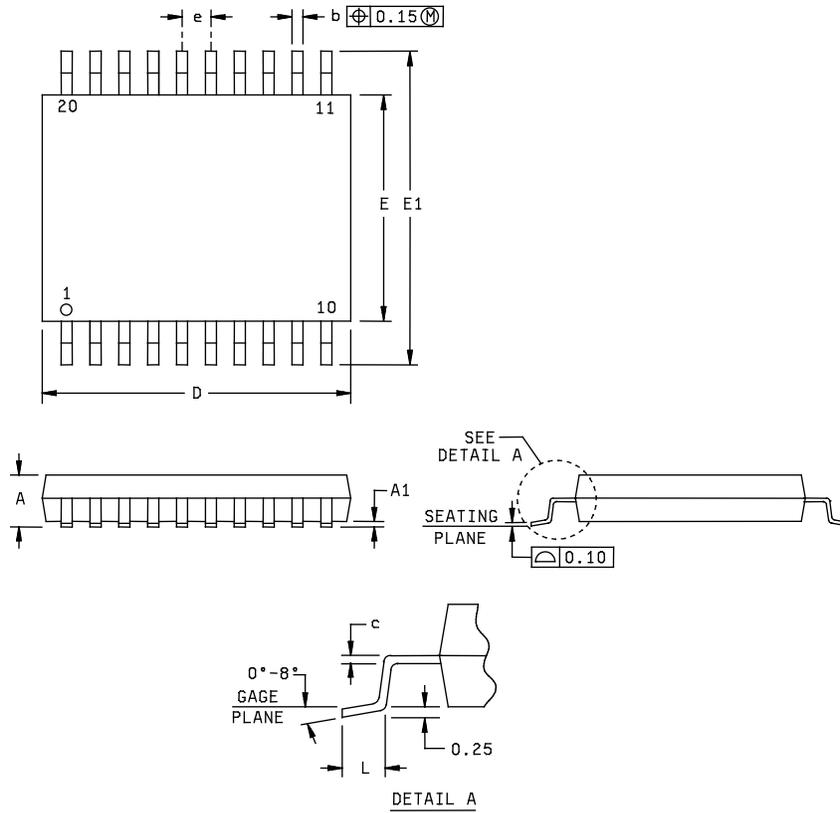
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions unless otherwise specified	V _{CC}	T _A = 25°C		-40°C to +85°C		Unit	
				Min	Max	Min	Max		
Disable time from input \overline{OE} to output A or B	t _{dis}		1.8 V ±0.15 V	1	16.5	1	17	ns	
			2.5 V ±0.2 V	1	9	1	9.5		
			2.7 V	1	8.3	1	8.5		
			3.3 V ±0.3 V	1.7	7.3	1.7	7.5		
Outputs skew time	t _{sk(o)}		3.3 V ±0.3 V				1		
Power dissipation capacitance per transceiver	C _{pd}	f = 10 MHz	Outputs enabled	1.8 V	42 Typ				pF
				2.5 V	43 Typ				
				3.3 V	45 Typ				
			Outputs disabled	1.8 V	1 Typ				
				2.5 V	1 Typ				
				3.3 V	2 Typ				

1. Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2. For I/O ports, the parameter IOZ includes the input leakage current.
3. This applies in the disabled state only.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.047		1.20	E	.168	.176	4.30	4.50
A1	.000	.006	0.05	0.15	E1	.242	.258	6.20	6.60
b	.007	.012	0.19	0.30	e	.025 BSC		0.65 BSC	
c	.006 NOM		0.15 NOM		L	.020	.029	0.50	0.75
D	.250	.258	6.40	6.60					

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines.

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Pin No.	Signal name	Pin No.	Signal name
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	\overline{OE}
10	GND	20	V _{CC}

FIGURE 2. Terminal connections.

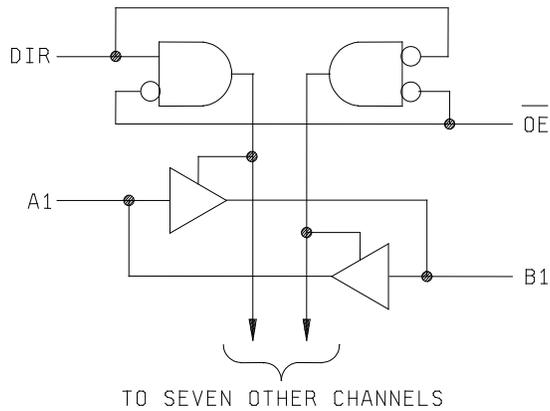
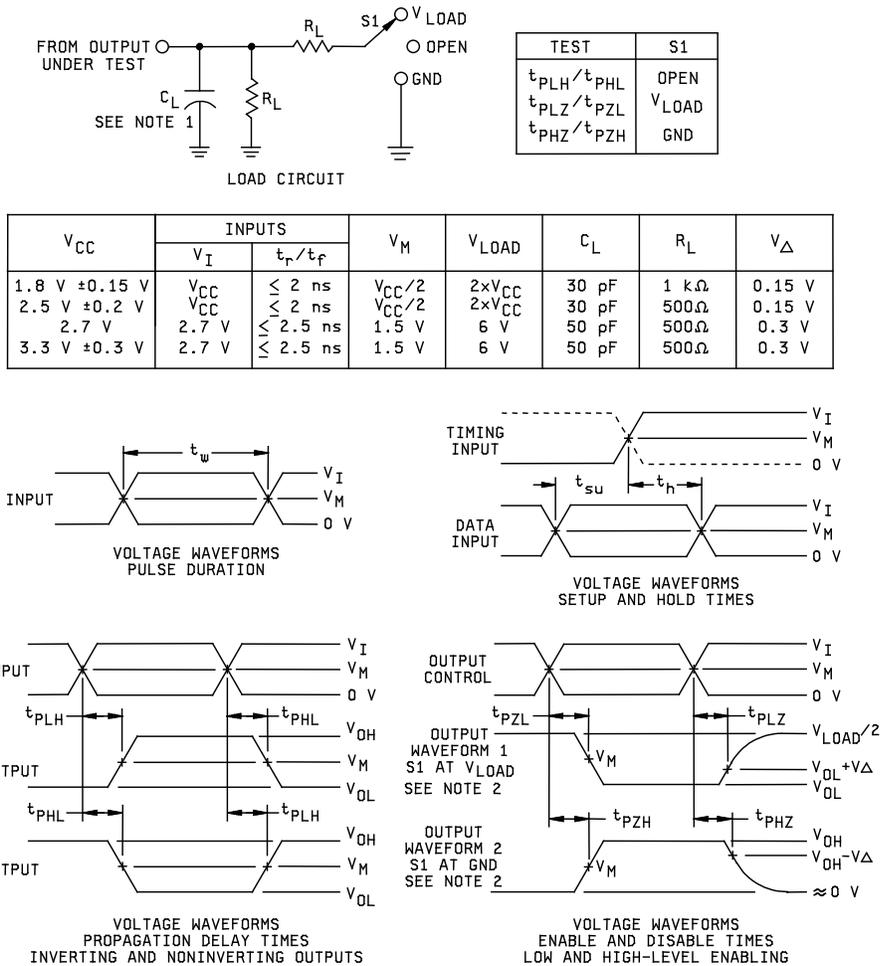


FIGURE 3. Logic diagram.

Inputs		Operation
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

FIGURE 4. Function Table

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Notes:

1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis} .
6. t_{PZL} and t_{PZH} are the same t_{en} .
7. t_{PLH} and t_{PHL} are the same t_{pd} .
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04737-01XE	01295	SN74LVC245AIPWREP	C245AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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