

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single 2-input positive AND gate microcircuit, with an operating temperature range of -40°C to +85°C for device 01, and -55°C to +125°C for device 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/04733</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC1G08-EP	Single 2-input positive AND gate.
02	SN74LVC1G08-EP	Single 2-input positive AND gate.

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	JEDEC MO-203	Plastic small outline
Y	5	JEDEC MO-178	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC})	-0.5 V to +6.5 V
Input voltage range, (V_I)	-0.5 V to +6.5 V <u>2/</u>
Voltage range applied to any output in the high impedance or power-off stage, (V_O)	-0.5 V to +6.5 V <u>2/</u>
Voltage range applied to any output in the high or slow state, (V_O)	-0.5 V to $V_{CC} + 0.5$ V <u>2/ 3/</u>
Input clamp current, (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current, (I_{OK}) ($V_O < 0$)	-50 mA
Continuous output current, (I_O)	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance (θ_{JA}):	
Case X	252°C/W <u>4/</u>
Case Y	256°C/W <u>4/</u>
Storage temperature range, (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage, (V_{CC}):	
Operating	+1.65 V to +5.5 V
Minimum data retention only	+1.5 V
Minimum high level input voltage, (V_{IH}):	
$V_{CC} = 1.65$ V to 1.95 V	+0.65 x V_{CC}
$V_{CC} = 2.3$ V to 2.7 V	+1.7 V
$V_{CC} = 3.0$ to 3.6 V	+2.0 V
$V_{CC} = 4.5$ V to 5.5 V	+0.7 x V_{CC}
Maximum low level input voltage, (V_{IL}):	
$V_{CC} = 1.65$ V to 1.95 V	+0.35 x V_{CC}
$V_{CC} = 2.3$ V to 2.7 V	+0.7 V
$V_{CC} = 3.0$ to 3.6 V	+0.8 V
$V_{CC} = 4.5$ V to 5.5 V	+0.3 x V_{CC}
Input voltage, (V_I)	0.0 V to 5.5 V
Output voltage, (V_O)	0.0 V to V_{CC}
Maximum high level output current, (I_{OH}):	
$V_{CC} = 1.65$ V	-4 mA
$V_{CC} = 2.3$ V	-8 mA
$V_{CC} = 3.0$ V	-16 mA
$V_{CC} = 3.0$ V	-24 mA
$V_{CC} = 4.5$ V	-32 mA
Maximum low level output current, (I_{OL}):	
$V_{CC} = 1.65$ V	4 mA
$V_{CC} = 2.3$ V	8 mA
$V_{CC} = 3.0$ V	16 mA
$V_{CC} = 3.0$ V	24 mA
$V_{CC} = 4.5$ V	32 mA
Maximum Input transition rise or fall rate ($\Delta t/\Delta v$):	
$V_{CC} = 1.8$ V \pm 0.15 V, 2.5 V \pm 0.2 V	20 ns/V
$V_{CC} = 3.3$ V \pm 0.3 V	10 ns/V
$V_{CC} = 5$ V \pm 0.5 V	5 ns/V

- 1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative voltage ratings may exceeded if the input and output current ratings are observed.
- 3/ The value of V_{CC} is provided in the recommended operating conditions table.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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1.4 Recommended operating conditions - Continued.

Operating free air temperature, (T_A):

Device 01	-40°C to +85°C
Device 02	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5 and 6.

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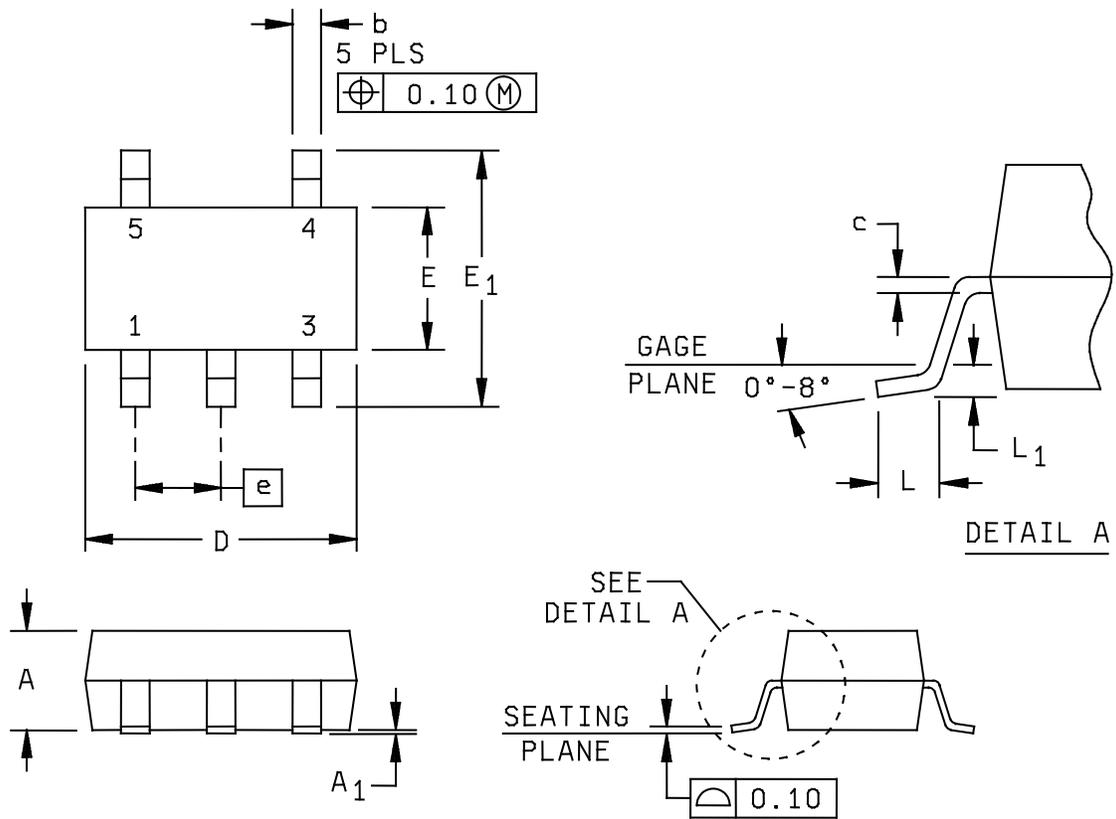
TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions Device 01: $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ Device 02: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}		$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	All	$V_{CC} - 0.1$	V
			$I_{OH} = -4 \text{ mA}$	1.65 V		1.2	
			$I_{OH} = -8 \text{ mA}$	2.3 V		1.9	
			$I_{OH} = -16 \text{ mA}$	3.0 V		2.4	
			$I_{OH} = -24 \text{ mA}$			2.3	
			$I_{OH} = -32 \text{ mA}$	4.5 V		3.8	
Low level output voltage	V_{OL}		$I_{OL} = 100 \mu\text{A}$	1.65 V to 5.5 V		0.1	V
			$I_{OL} = 4 \text{ mA}$	1.65 V		0.45	
			$I_{OL} = 8 \text{ mA}$	2.3 V		0.3	
			$I_{OL} = 16 \text{ mA}$	3.0 V		0.4	
			$I_{OL} = 24 \text{ mA}$			0.55	
			$I_{OL} = 32 \text{ mA}$	4.5 V		0.55	
Input current	A or B inputs	I_I	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V		± 5	μA
Input/output power off leakage current		I_{off}	$V_I \text{ or } V_O = 5.5 \text{ V}$	0 V		± 10	μA
Quiescent supply current		I_{CC}	$V_I = 5.5 \text{ V or GND, } I_O = 0$	1.65 V to 5.5 V		10	μA
Quiescent supply current delta		ΔI_{CC}	One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μA
Input capacitance		C_i	$V_I = V_{CC}$ or GND, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$	3.3 V		4 Typ	pF
Propagation delay time from input A or B to output Y	t_{pd}	$C_L = 15 \text{ pF}$ See figure 5	1.8 V $\pm 0.15 \text{ V}$	01	1.5	7.2	ns
			2.5 V $\pm 0.2 \text{ V}$		0.7	4.4	
			3.3 V $\pm 0.3 \text{ V}$		0.8	3.6	
			5 V $\pm 0.5 \text{ V}$		0.8	3.4	
Propagation delay time from input A or B to output Y	t_{pd}	$C_L = 30 \text{ pF or } 50 \text{ pF}$ See figure 6	1.8 V $\pm 0.15 \text{ V}$		2.4	8	ns
			2.5 V $\pm 0.2 \text{ V}$		1.1	5.5	
			3.3 V $\pm 0.3 \text{ V}$		1	4.5	
			5 V $\pm 0.5 \text{ V}$		1	4	
Propagation delay time from input A or B to output Y	t_{pd}	$C_L = 50 \text{ pF}$ See figure 6	1.8 V $\pm 0.15 \text{ V}$	02	2.4	11	ns
			2.5 V $\pm 0.2 \text{ V}$		1.1	7.5	
			3.3 V $\pm 0.3 \text{ V}$		1	6.5	
			5 V $\pm 0.5 \text{ V}$		1	5	
Power dissipation capacitance	C_{pd}	$f = 10 \text{ MHz}$ $T_A = 25^{\circ}\text{C}$	1.8 V	All	21 Typ		pF
			2.5 V		24 Typ		
			3.3 V		26 Typ		
			5.0 V		31 Typ		

1. Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion.
4. Falls within JEDEC MO-203.

FIGURE 1. Case outlines.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04733</p>
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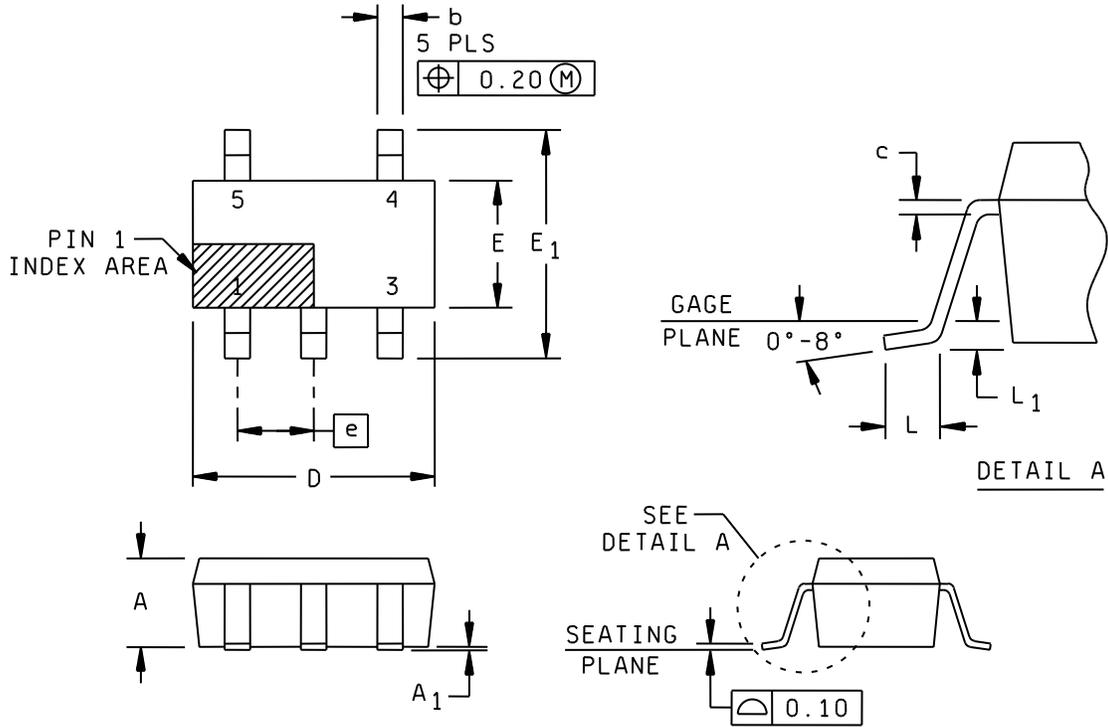
Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.031	.043	0.80	1.10
A1	.000	.004	0.00	0.10
b	.006	.012	0.15	0.30
c	.005 NOM		0.13 NOM	
D	.072	.084	1.85	2.15
E	.043	.055	1.10	1.40
E1	.070	.094	1.80	2.40
e	.025 BSC		0.65 BSC	
L	.010	.018	0.26	0.46
L1	.006 TYP		0.15 TYP	

FIGURE 1. Case outlines - Continued.

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Case Y



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-178, variation AA.

FIGURE 1. Case outlines - Continued.

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Case Y

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.057	---	1.45
A1	.000	.006	0.00	0.15
b	.012	.020	0.30	0.50
c	.003	.009	0.08	0.22
D	.108	.120	2.75	3.05
E	.057	.069	1.45	1.75
E1	.102	.118	2.60	3.00
e	.037 BSC		0.95 BSC	
L	.012	.022	0.30	0.55
L1	.010 BSC		0.25 BSC	

FIGURE 1. Case outlines - Continued.

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Cases X and Y

Pin No.	Signal name
1	A
2	B
3	GND
4	Y
5	V _{CC}

FIGURE 2. Terminal connections.

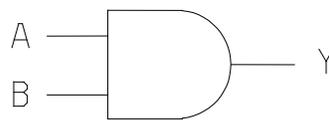
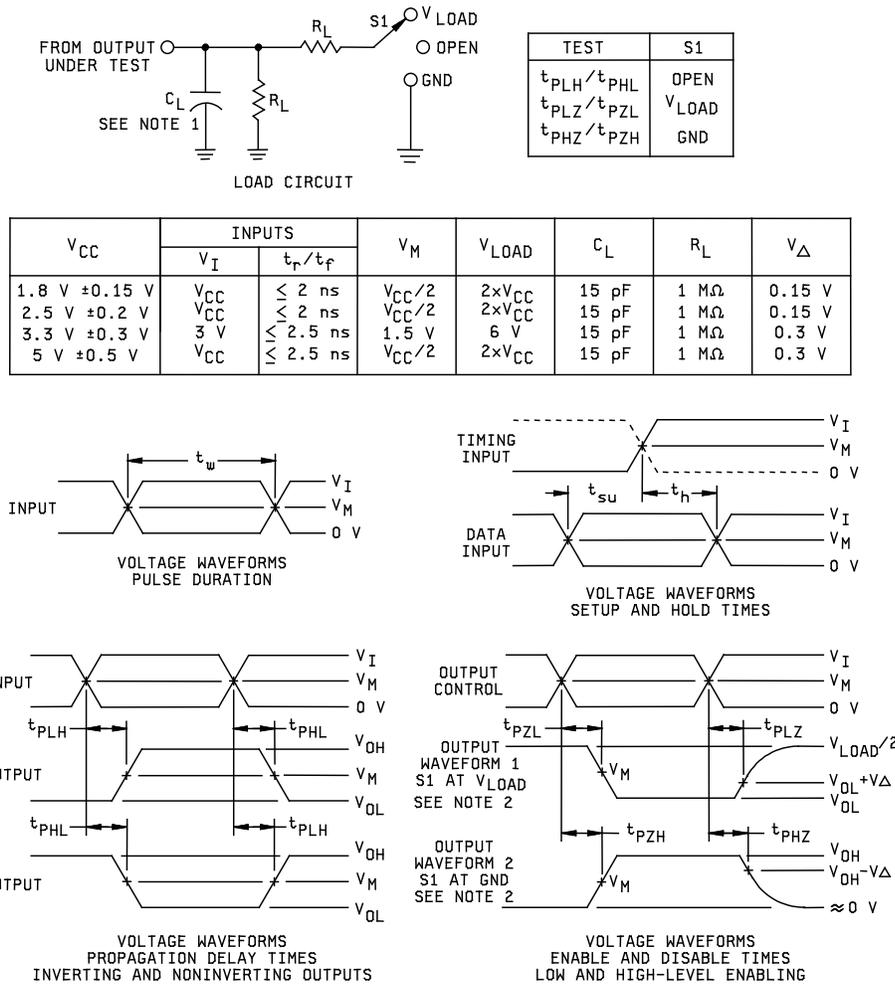


FIGURE 3. Logic diagram.

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L

FIGURE 4. Function Table

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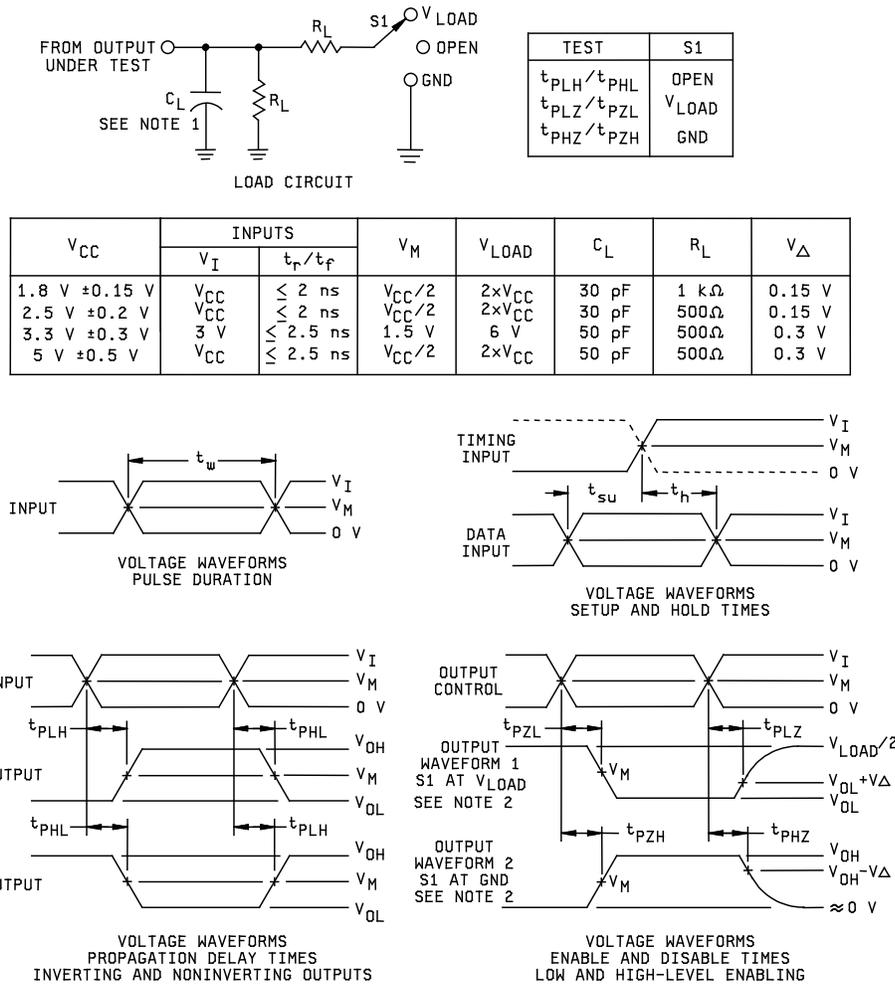


Notes:

1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis}.
6. t_{PZL} and t_{PZH} are the same t_{en}.
7. t_{PLH} and t_{PHL} are the same t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms.

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Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis}.
6. t_{PZL} and t_{PZH} are the same t_{en}.
7. t_{PLH} and t_{PHL} are the same t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 6. Load circuit and voltage waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04733-01XE	01295	SN74LVC1G08IDCKREP	CEO
V62/04733-02XE	01295	SN74LVC1G08MDCKREP	CEO
V62/04733-02YE	01295	SN74LVC1G08MDBVREP	C08O

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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