REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-08-22	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-09-20	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - DRH	23-04-20	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C							
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15							

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Original date of drawing

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https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 3.3-V ABT SCAN TEST DEVICE WITH 18-BIT UNIVERSAL BUS TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04730
REV	C	PAGE 1 OF 15

AMSC N/A

5962-V081-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT scan test device with 18-bit universal bus transceiver microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04730	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVTH182512-EP	3.3-V ABT scan test device with 18-bit universal bus transceiver

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	64	JEDEC MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +4.6 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high state or power-off state (V_O)	-0.5 V to 7 V 2/
Current into any output in the low state (I_O):	
(A port or TDO)	128 mA
(B port)	30 mA
Current into any output in the high state (I_O): 3/	
(A port or TDO)	64 mA
(B port)	30 mA
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Package thermal impedance (θ_{JA})	73°C/W 4/
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	2.7 V to 3.6 V
Minimum high level input voltage (V_{IH})	2 V
Maximum low level input voltage (V_{IL})	0.8 V
Maximum input voltage (V_I)	5.5 V
Maximum high level output current (I_{OH}):	
(A port or TDO)	-32 mA
(B port)	-12 mA
Maximum low level output current (I_{OL}):	
(A port or TDO)	32 mA
(B port)	12 mA
Maximum low level output current (I_{OL}) (A port or TDO)	64 mA 6/
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) (Outputs enabled)	10 ns/V
Operating free-air temperature range (T_A)	-40°C to +85°C

_____

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ Unused control inputs must be held high or low to prevent them from floating.
6/ Current duty cycle ≤ 50%, f ≥ 1 kHz.

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JESD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at https://www.ieee.org/.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V_{IK}	I_I = -18 mA	2.7 V	25°C, -40°C to 85°C	All		-1.2	V
High level output voltage	V_{OH}	A, B, TDO, I_{OH} = -100 µA	2.7 V to 3.6 V			V_{CC} – 0.2		V
		A port, TDO, I_{OH} = -3 mA	2.7 V			2.4		
		A port, TDO, I_{OH} = -8 mA	3 V			2.4		
		A port, TDO, I_{OH} = -32 mA				2		
		B port, I_{OH} = -12 mA				2		
Low level output voltage	V_{OL}	A, B, TDO, I_{OL} = 100 µA	2.7 V				0.2	V
		A port, TDO, I_{OL} = 24 mA					0.5	
		A port, TDO, I_{OL} = 16 mA	3 V				0.4	
		A port, TDO, I_{OL} = 32 mA					0.5	
		A port, TDO, I_{OL} = 64 mA					0.55	
		B port, I_{OL} = 12 mA					0.8	
Input current	I_I	CLK, LE, TCK $V_I = V_{CC}$ or GND	3.6 V				±1	µA
		CLK, LE, TCK, V_I = 5.5 V	0 V or 3.6 V				10	
		$\overline{OE}$, TDI, TMS, V_I = 5.5 V	3.6 V				5	
		$\overline{OE}$, TDI, TMS, $V_I = V_{CC}$					1	
		$\overline{OE}$, TDI, TMS, V_I = 0 V				-25	-100	
		A or B ports, V_I = 5.5 V 2/					20	
		A or B ports, $V_I = V_{CC}$ 2/					1	
		A or B ports, V_I = 0 V 2/					-5	
Input/output power-off leakage current	I_{off}	V_I or V_O = 0 V to 4.5 V	0 V				±100	
Input current (hold)	$I_{I(hold)}$ 3/	A or B ports, V_I = 0.8 V	3 V			75	500	
		A or B ports, V_I = 2 V				-75	-500	
Off-state output current high	I_{OZH}	TDO V_O = 3 V	3.6 V				1	
Off-state output current low	I_{OZL}	TDO V_O = 0.5 V	3.6 V				-1	
3-state output current power-up	I_{OZPU}	TDO V_O = 0.5 V or 3 V	0 V to 1.5 V				±50	
3-state output current power-down	I_{OZPD}	TDO V_O = 0.5 V or 3 V	1.5 V to 0 V				±50	
Quiescent supply current	I_{CC}	Outputs high. $V_I = V_{CC}$ or GND, I_O = 0 A	3.6 V				2	mA
		Outputs low. $V_I = V_{CC}$ or GND, I_O = 0 A					24	
		Outputs disabled. $V_I = V_{CC}$ or GND, I_O = 0 A					2	
Quiescent supply current delta	ΔI_{CC} 4/	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V				0.5	
Input capacitance	C_i	V_I = 3 V or 0 V	3.3 V	25°C		4 TYP		pF
Input/output capacitance	C_{io}	V_O = 3 V or 0 V				10 TYP		
Output capacitance	C_o	V_O = 3 V or 0 V				8 TYP		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Normal Mode								
Clock frequency	f_{clock}	CLKAB or CLKBA	2.7 V	25°C,	All	0	80	MHz
		See figure 5.	3.3 V ±0.3 V	-40°C to 85°C		0	100	
Pulse duration	t_w	CLKAB or CLKBA high or low	2.7 V			5.6		ns
			3.3 V ±0.3 V			4.4		
See figure 5.		LEAB or LEBA high	2.7 V			3		
			3.3 V ±0.3 V			3		
Setup time	t_{su}	A before CLKAB↑	2.7 V			3		ns
		or B before CLKBA↑	3.3 V ±0.3 V			2.8		
See figure 5.		A before LEAB↓ or B	2.7 V			0.7		
		before LEBA↓, CLK high	3.3 V ±0.3 V			1.5		
		A before LEAB↓ or B	2.7 V			1.6		
		before LEBA↓, CLK low	3.3 V ±0.3 V			1.6		
Hold time	t_h	A after CLKAB↑	2.7 V			1.1		ns
		or B after CLKBA↑	3.3 V ±0.3 V			1.4		
See figure 5.		A after LEAB↓	2.7 V			3.5		
		or B after LEBA↓	3.3 V ±0.3 V			3.1		
Test Mode								
Clock frequency	f_{clock}	TCK	2.7 V	25°C,	All	0	40	MHz
		See figure 5.	3.3 V ±0.3 V	-40°C to 85°C		0	50	
Pulse duration	t_w	TCK high or low	2.7 V			10.5		ns
		See figure 5.	3.3 V ±0.3 V			9.5		
Setup time	t_{su}	A, B, CLK, LE, or $\overline{OE}$	2.7 V			7		
		before TCK↑	3.3 V ±0.3 V			6.5		
See figure 5.		TDI before TCK↑	2.7 V			3.5		
			3.3 V ±0.3 V			2.5		
		TMS before TCK↑	2.7 V			3.5		
			3.3 V ±0.3 V			2.5		
Hold time	t_h	A, B, CLK, LE, or $\overline{OE}$	2.7 V			1		
		after TCK↑	3.3 V ±0.3 V			1.7		
See figure 5.		TDI after TCK↑	2.7 V			1		
			3.3 V ±0.3 V			1.5		
		TMS after TCK↑	2.7 V			1		
			3.3 V ±0.3 V			1.5		
Delay time	t_d	Power up to TCK↑	2.7 V			50		
		See figure 5.	3.3 V ±0.3 V			50		
Rise time	t_r	V_{CC} power up	2.7 V			1		
		See figure 5.	3.3 V ±0.3 V			1		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Normal Mode								
Maximum frequency, CLKAB or CLKBA	f_{max}	See figure 5.	2.7 V	25°C, -40°C to 85°C	All	80		MHz
			3.3 V ±0.3 V			100		
Propagation delay time, A to B	t_{PLH}, t_{PHL}		2.7 V				6.4	ns
			3.3 V ±0.3 V			1.5	5.7	
Propagation delay time, B to A	t_{PLH}, t_{PHL}		2.7 V				5.6	ns
			3.3 V ±0.3 V			1.5	4.9	
Propagation delay time, CLKAB to B	t_{PLH}, t_{PHL}		2.7 V				7.7	ns
			3.3 V ±0.3 V			1.5	6.7	
Propagation delay time, CLKBA to A	t_{PLH}, t_{PHL}		2.7 V				6.8	ns
			3.3 V ±0.3 V			1.5	5.8	
Propagation delay time, LEAB to B	t_{PLH}		2.7 V				9.2	ns
			3.3 V ±0.3 V			1.5	8.2	
	t_{PHL}		2.7 V				6.7	
			3.3 V ±0.3 V			1.5	6.2	
Propagation delay time, LEBA to A	t_{PLH}		2.7 V				8.4	ns
			3.3 V ±0.3 V			1.5	7.4	
	t_{PHL}		2.7 V				6.4	
			3.3 V ±0.3 V			1.5	5.7	
Propagation delay time, output enable, $\overline{OEAB}$ or $\overline{OEBA}$ to B or A	t_{PZH}, t_{PZL}		2.7 V				8.7	ns
			3.3 V ±0.3 V			1.5	7.9	
Propagation delay time, output disable, $\overline{OEAB}$ or $\overline{OEBA}$ to B or A	t_{PHZ}, t_{PLZ}		2.7 V				8.9	ns
			3.3 V ±0.3 V			2.5	8.4	
Test Mode								
Maximum frequency, TCK	f_{max}	See figure 5.	2.7 V	25°C, -40°C to 85°C	All	40		MHz
			3.3 V ±0.3 V			50		
Propagation delay time, TCK↓ to A or B	t_{PLH}, t_{PHL}		2.7 V				17	ns
			3.3 V ±0.3 V			2.5	14	
Propagation delay time, TCK↓ to TDO	t_{PLH}		2.7 V				6.5	
			3.3 V ±0.3 V			1	5.5	
	t_{PHL}		2.7 V				7.5	
			3.3 V ±0.3 V			1.5	6.5	
Propagation delay time, output enable, TCK↓ to A or B	t_{PZH}, t_{PZL}		2.7 V				20	
			3.3 V ±0.3 V			4	17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Test Mode (continued)								
Propagation delay time, output enable, TCK↓ to TDO	t_{PZH}	See figure 5.	2.7 V	25°C, -40°C to 85°C	All		6.5	ns
			3.3 V ±0.3 V			1	5.5	
	t_{PZL}		2.7 V				6.5	
			3.3 V ±0.3 V			1.5	5.5	
Propagation delay time, output disable, TCK↓ to A or B	t_{PHZ}		2.7 V				20	ns
			3.3 V ±0.3 V			4	18	
	t_{PLZ}		2.7 V				18.5	
			3.3 V ±0.3 V			4	17	
Propagation delay time, output disable, TCK↓ to TDO	t_{PHZ}		2.7 V				8.5	ns
			3.3 V ±0.3 V			1.5	7	
	t_{PLZ}		2.7 V				8	
			3.3 V ±0.3 V			1.5	7	

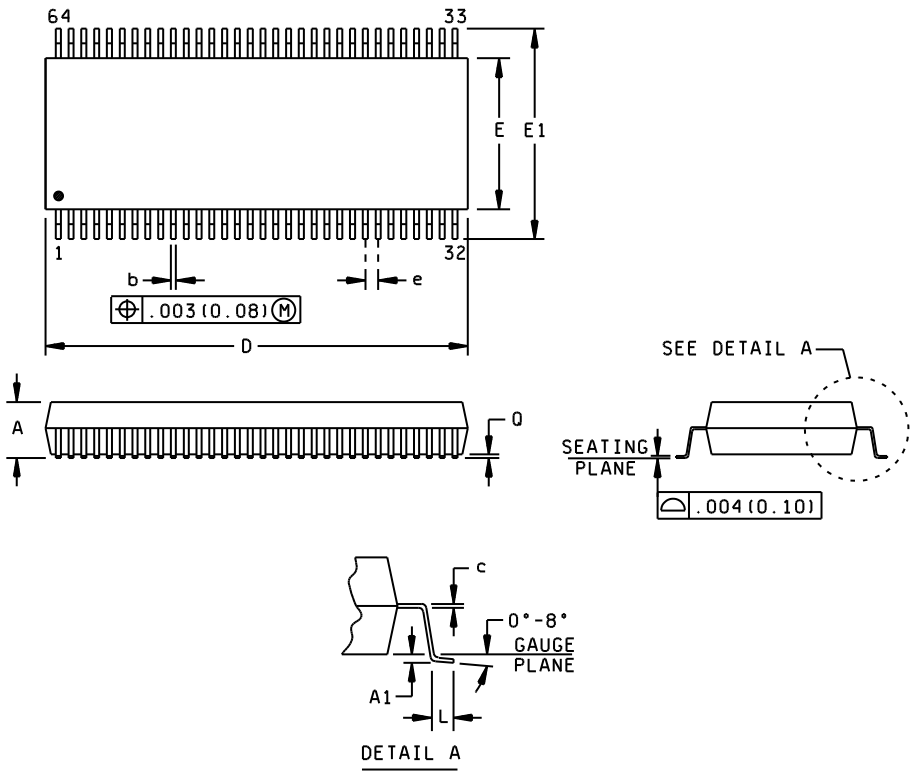
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unused pins at V_{CC} or GND.

3/ The parameter $I_{I(hold)}$ includes the off-state output leakage current.

4/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	6.00	6.20	0.236	0.244
A1	0.25 TYP		0.010 TYP		E1	7.90	8.30	0.311	0.327
b	0.17	0.27	0.007	0.011	e	0.50 TYP		0.020 TYP	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	16.90	17.10	0.665	0.673	Q	0.05	0.15	0.002	0.006

NOTES:
1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-153.
3. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.
4. Body dimensions do not include mold protrusion not to exceed 0.15 millimeters.

FIGURE 1. Case outline.

Function Table 1/
(normal mode, each register)

Inputs				Output
$\overline{OEAB}$	LEAB	CLKAB	A	B
L	L	L	X	B_0 *
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

H = High
L = Low
X = Immaterial
↑ = Low-to-high clock transition.
* = Output level before the indicated steady-state input conditions are established.
Z = High-impedance state

1/ A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, and CLKBA.

FIGURE 2. Function table.

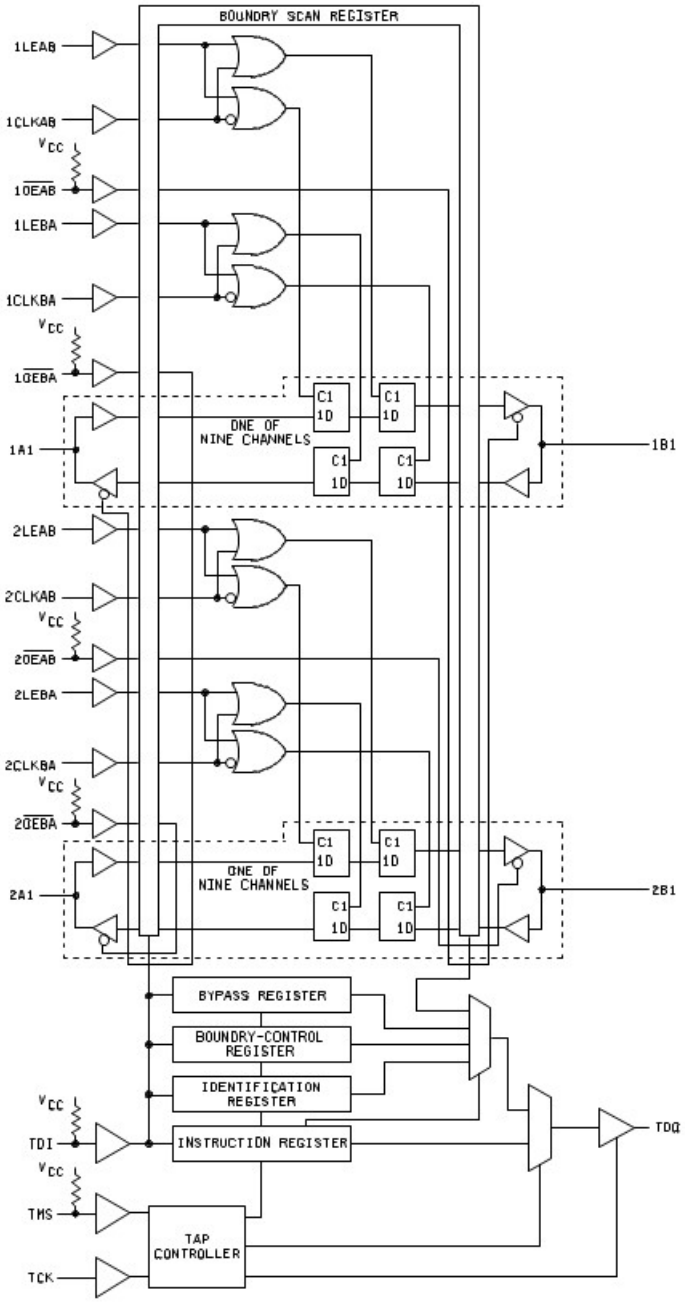


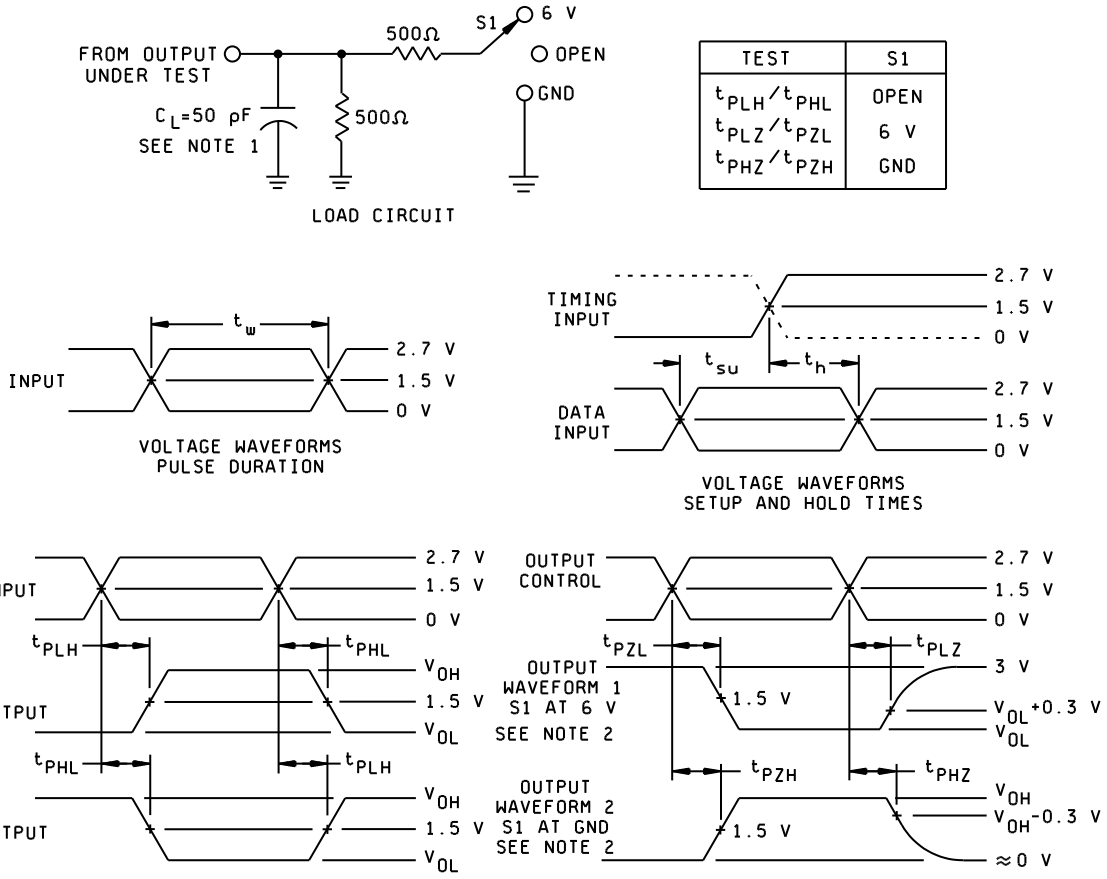
FIGURE 3. Functional block diagram.

Device type		01					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1CLKAB	17	2A2	33	TCK	49	2B1
2	1LEAB	18	2A3	34	TDI	50	1B9
3	$1\overline{OEAB}$	19	GND	35	2CLKBA	51	GND
4	1A1	20	2A4	36	2LEBA	52	1B8
5	1A2	21	2A5	37	$2\overline{OEBA}$	53	1B7
6	GND	22	2A6	38	GND	54	1B6
7	1A3	23	V_{CC}	39	2B9	55	V_{CC}
8	1A4	24	2A7	40	2B8	56	1B5
9	1A5	25	2A8	41	2B7	57	1B4
10	V_{CC}	26	2A9	42	V_{CC}	58	1B3
11	1A6	27	GND	43	2B6	59	GND
12	1A7	28	$2\overline{OEAB}$	44	2B5	60	1B2
13	1A8	29	2LEAB	45	2B4	61	1B1
14	GND	30	2CLKAB	46	GND	62	$1\overline{OEBA}$
15	1A9	31	TDO	47	2B3	63	1LEBA
16	2A1	32	TMS	48	2B2	64	1CLKBA

Terminal Functions

Terminal Name	Description
1A1 – 1A9, 2A1 – 2A9	Normal-function A-bus I/O ports. See function table (figure 2) for normal-mode logic.
1B1 – 1B9, 2B1 – 2B9	Normal-function B-bus I/O ports. See function table (figure 2) for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table (figure 2) for normal-mode logic.
GND	Ground.
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables. See function table (figure 2) for normal-mode logic.
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	Normal-function output enables. See function table (figure 2) for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage.

FIGURE 4. Terminal connections.

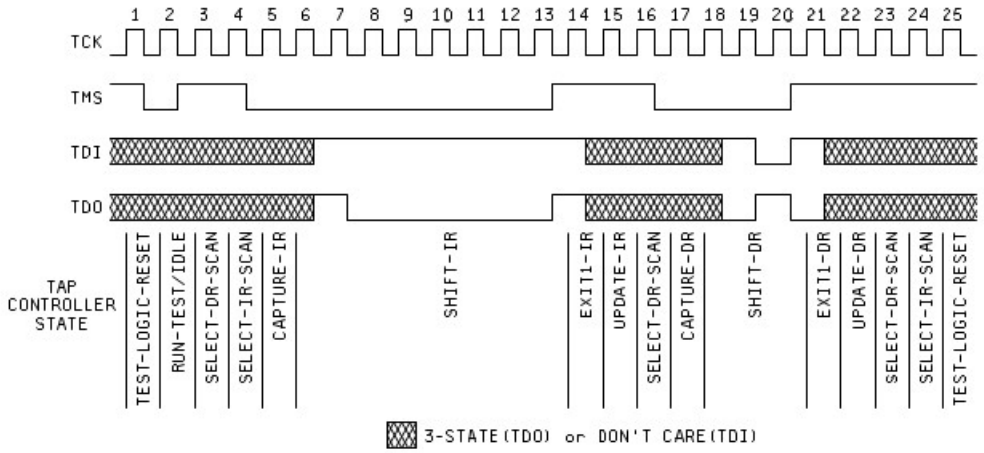


NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Timing waveforms and test circuit.

Timing Example



Explanation of Timing Example

TCK cycle(s)	TAP state after TCK	Description
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7 – 13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19 – 20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	The selected data register is updated with the new data on the falling edge of TCK.
23	Select-Dr-Scan	
24	Select-IR-scan	
25	Test-Logic-Reset	Test operation completed.

FIGURE 5. Timing waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04730-01XE	01295	8V182512IDGGREP	LH182512EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243