REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-08-22	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-09-20	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - DRH	23-04-20	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C												
SHEET	1	2	3	4	5	6	7	8	9	10												

PMIC N/A

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TITLE
MICROCIRCUIT, DIGITAL, ADVANCED CMOS, DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04725
REV C		PAGE 1 OF 10

AMSC N/A

5962-V080-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual positive-edge-triggered D-type flip-flop with clear and preset, TTL compatible inputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04725	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74ACT74-EP	Dual positive-edge-triggered D-type flip-flop with clear and preset, TTL compatible inputs

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MS-012	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7.0 V
Input voltage range (V_I)	-0.5 V to V_{CC} + 0.5 V 2/
Output voltage range (V_O)	-0.5 V to V_{CC} + 0.5 V 2/
Input clamp current (I_{IK}) (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current (I_{OK}) (V_O < 0 or V_O > V_{CC})	±20 mA
Continuous output current (I_O) (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Package thermal impedance (θ_{JA})	86°C/W 3/
Storage temperature range (T_{STG})	-65°C to +150°C 4/

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Minimum high level input voltage (V_{IH})	2 V
Maximum low level input voltage (V_{IL})	0.8 V
Input voltage range (V_I)	0.0 V to V_{CC}
Output voltage range (V_O)	0.0 V to V_{CC}
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	24 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$)	8 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 μA	4.5 V	25°C,	All	4.4		V
			5.5 V	-55°C to 125°C		5.4		
		I_{OH} = -24 mA	4.5 V	25°C		3.86		
				-55°C to 125°C		3.7		
			5.5 V	25°C		4.86		
				-55°C to 125°C		4.7		
Low level output voltage	V_{OL}	I_{OL} = 50 μA	4.5 V	25°C			0.1	V
			5.5 V	-55°C to 125°C			0.1	
		I_{OL} = 24 mA	4.5 V	25°C			0.36	
				-55°C to 125°C			0.5	
			5.5 V	25°C			0.36	
				-55°C to 125°C			0.5	
Input current	I_I	V_I = V_{CC} or GND	5.5 V	25°C			±0.1	μA
				-55°C to 125°C			±1	
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND I_O = 0 A	5.5 V	25°C			2	μA
				-55°C to 125°C			40	
Quiescent supply current delta	ΔI_{CC} 2/	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V	25°C, -55°C to 125°C			1.6	mA
Input capacitance	C_I	V_I = V_{CC} or GND	5 V	25°C		3 TYP		pF
Power dissipation capacitance	C_{pd}	C_L = 50 pF f = 1 MHz	5 V	25°C		45 TYP		pF

See footnotes at end of table.

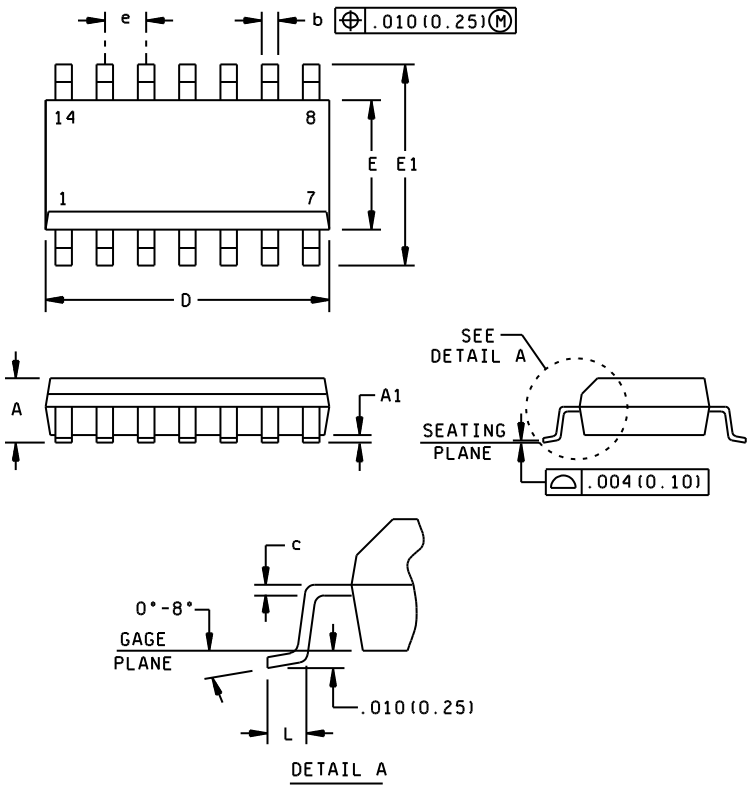
TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Clock frequency	f_{clock}		4.5 V and 5.5 V	25°C	All		145	MHz
				-55°C to 125°C			85	
Pulse duration	t_w	$\overline{PRE}$ or $\overline{CLR}$ low See figure 5	4.5 V and 5.5 V	25°C		5		ns
				-55°C to 125°C		7		
		CLK See figure 5	4.5 V and 5.5 V	25°C		5		
				-55°C to 125°C		7		
Setup time, data before CLK↑	t_{su}	Data See figure 5	4.5 V and 5.5 V	25°C		3		ns
				-55°C to 125°C		4		
		$\overline{PRE}$ or $\overline{CLR}$ inactive See figure 5	4.5 V and 5.5 V	25°C		0		
				-55°C to 125°C		0.5		
Hold time, data after CLK↑	t_h	See figure 5	4.5 V and 5.5 V	25°C		1		ns
				-55°C to 125°C		1		
Maximum frequency	f_{max}		4.5 V and 5.5 V	25°C		145		MHz
				-55°C to 125°C		85		
Propagation delay time, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$	t_{PLH}	See figure 5	4.5 V and 5.5 V	25°C		1	9.5	ns
				-55°C to 125°C		1	11.5	
	t_{PHL}		4.5 V and 5.5 V	25°C		1	10	
				-55°C to 125°C		1	12.5	
Propagation delay time, CLK to Q or $\overline{Q}$	t_{PLH}		4.5 V and 5.5 V	25°C		1	11	ns
				-55°C to 125°C		1	14	
	t_{PHL}		4.5 V and 5.5 V	25°C		1	10	
				-55°C to 125°C		1	12	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.75	---	.069	E	3.81	4.00	.150	.157
A1	0.10	0.25	.004	.010	E1	5.80	6.20	.228	.244
b	0.35	0.51	.014	.020	e	1.27 NOM		.050 NOM	
c	0.20 NOM		.008 NOM		L	0.40	1.12	.016	.044
D	8.55	8.75	.337	.344					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-012.
4. All linear dimensions are shown in inches (millimeters). Metric equivalents are given for general information only.

FIGURE 1. Case outline.

(each flip-flop)

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High level
L = Low level
X = Immaterial
↑ = Rising edge of CLK
* = This configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.
Q_0 = Level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$ = Complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

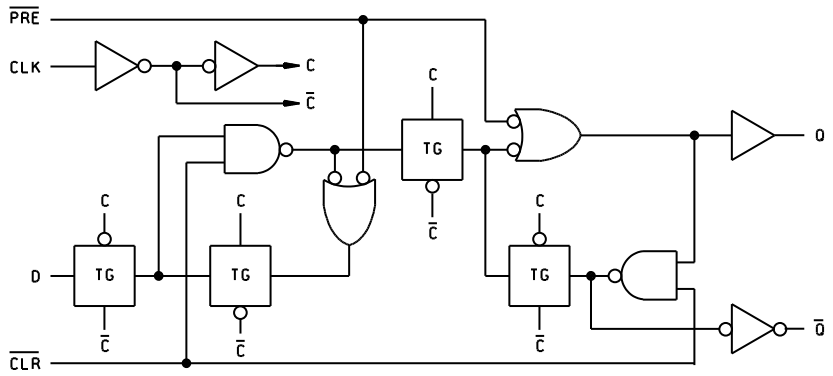
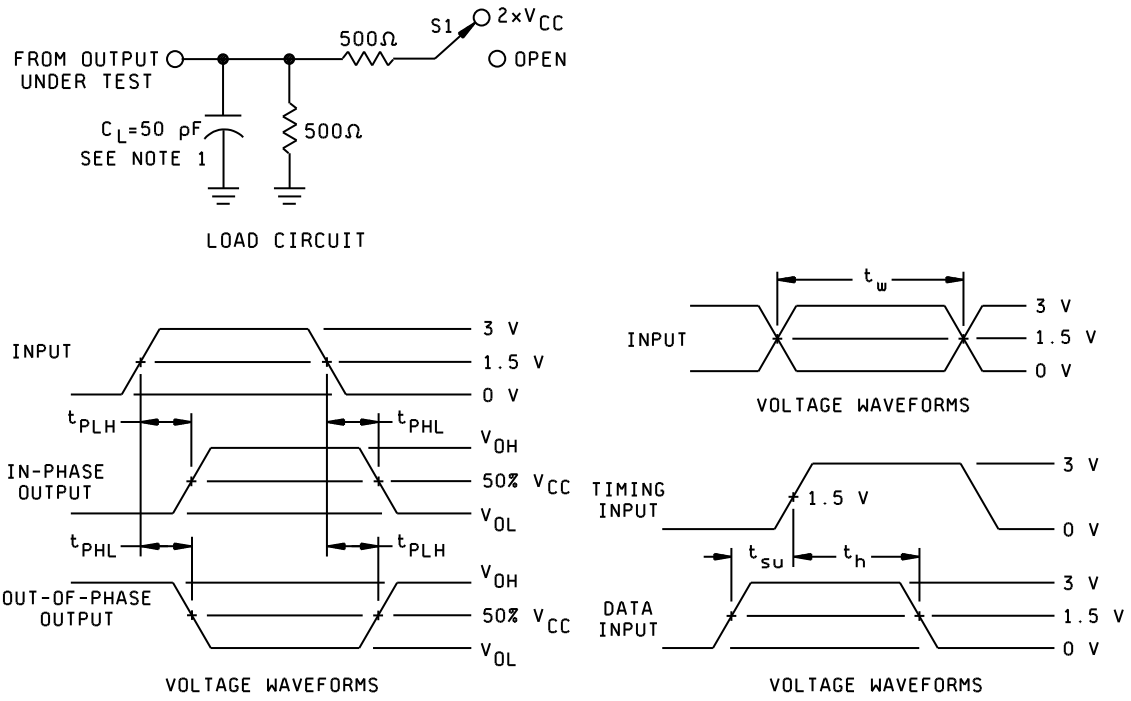


FIGURE 3. Logic diagram.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1$\overline{CLR}$	8	2$\overline{Q}$
2	1D	9	2Q
3	1CLK	10	2$\overline{PRE}$
4	1$\overline{PRE}$	11	2CLK
5	1Q	12	2D
6	1$\overline{Q}$	13	2$\overline{CLR}$
7	GND	14	V_{CC}

FIGURE 4. Terminal connections.



NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
3. The outputs are measured one at a time with one input transition per measurement.
4. For t_{PLH}/t_{PHL} tests, S1 = Open.

FIGURE 5. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04725-01XE	01295	SN74ACT74MDREP	SACT74MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243