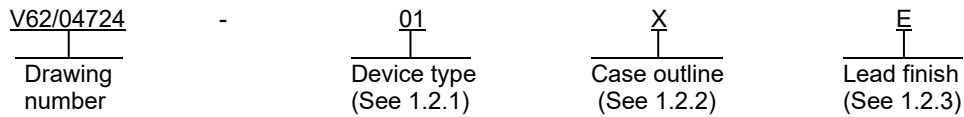


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit buffer/driver with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC16244A-EP	16-bit buffer/driver with 3-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	48	JEDEC MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_i)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_o)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state (V_o)	-0.5 V to $V_{CC} + 0.5$ V 2/ 3/
Input clamp current (I_{IK}) ($V_i < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_o < 0$)	-50 mA
Continuous output current (I_o)	± 50 mA
Continuous current through each V_{CC} or GND	± 100 mA
Package thermal impedance (θ_{JA})	70°C/W 4/
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}):	
Operating	1.65 V to 3.6 V
Data retention only	1.5 V
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 1.65$ V to 1.95 V	0.65 x V_{CC}
$V_{CC} = 2.3$ V to 2.7 V	1.7 V
$V_{CC} = 2.7$ V to 3.6 V	2 V
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 1.65$ V to 1.95 V	0.35 x V_{CC}
$V_{CC} = 2.3$ V to 2.7 V	0.7 V
$V_{CC} = 2.7$ V to 3.6 V	0.8 V
Input voltage range (V_i)	0 V to 5.5 V
Output voltage range (V_o):	
High or low state	0 V to V_{CC}
3-state	0 V to 5.5 V
Maximum high level output current (I_{OH}):	
$V_{CC} = 1.65$ V	-4 mA
$V_{CC} = 2.3$ V	-8 mA
$V_{CC} = 2.7$ V	-12 mA
$V_{CC} = 3$ V	-24 mA
Maximum low level output current (I_{OL}):	
$V_{CC} = 1.65$ V	4 mA
$V_{CC} = 2.3$ V	8 mA
$V_{CC} = 2.7$ V	12 mA
$V_{CC} = 3$ V	24 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$)	10 ns/V
Operating free-air temperature range (T_A)	-40°C to +85°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 3/ The value of V_{CC} is provided in the recommended operating conditions table.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JESD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit	
						Min	Max		
High level output voltage	V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	25°C, -40°C to 85°C	All	V _{CC} - 0.2		V	
		I _{OH} = -4 mA	1.65 V			1.2			
		I _{OH} = -8 mA	2.3 V			1.7			
		I _{OH} = -12 mA	2.7 V			2.2			
			3 V			2.4			
Low level output voltage	V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2	V	
		I _{OL} = 4 mA	1.65 V				0.45		
		I _{OL} = 8 mA	2.3 V				0.7		
		I _{OL} = 12 mA	2.7 V				0.4		
		I _{OL} = 24 mA	3 V				0.55		
Input current	I _I	V _I = 0 V to 5.5 V	3.6 V				±5	μA	
Input/output power-off leakage current	I _{off}	V _I or V _O = 5.5 V	0 V				±10	μA	
3-state output current	I _{OZ}	V _O = 0 V to 5.5 V	3.6 V				±10	μA	
Quiescent supply current	I _{CC}	V _I = V _{CC} or GND I _O = 0 A	3.6 V				20	μA	
		3.6 V ≤ V _I ≤ 5.5 V <u>2</u> / I _O = 0 A					20		
Quiescent supply current delta	ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V				500	μA	
Input capacitance	C _i	V _I = V _{CC} or GND	3.3 V	25°C			5.5 TYP	pF	
Output capacitance	C _o	V _O = V _{CC} or GND					6 TYP	pF	
Power dissipation capacitance per buffer/driver	C _{pd}	Outputs enabled f = 10 MHz	1.8 V				33 TYP	pF	
			2.5 V				35 TYP		
			3.3 V				39 TYP		
		Outputs disabled f = 10 MHz	1.8 V						2 TYP
			2.5 V						3 TYP
			3.3 V						4 TYP

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

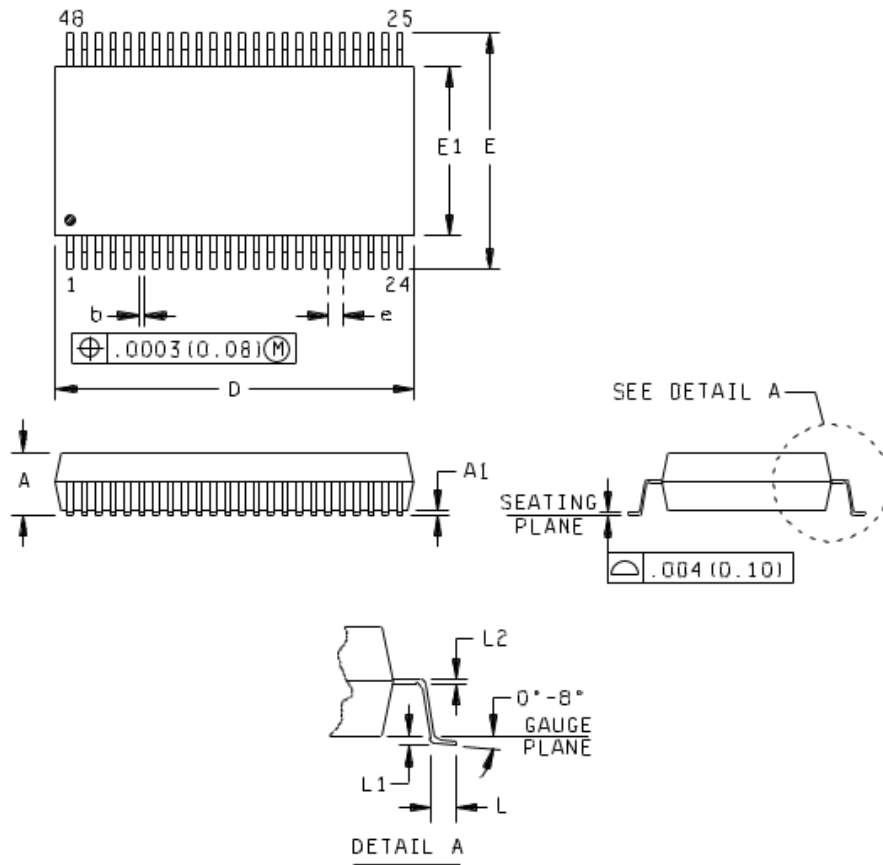
Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Propagation delay time, A to Y	t _{pd}	See figure 5	1.8 V ±0.15 V	25°C, -40°C to 85°C	All	1.5	6.6	ns
			2.5 V ±0.2 V			1	3.9	
			2.7 V			1	4.7	
			3.3 V ±0.3 V			1.1	4.1	
Propagation delay time, output enable, \overline{OE} to Y	t _{en}		1.8 V ±0.15 V			1.5	7.5	ns
			2.5 V ±0.2 V			1	4.7	
			2.7 V			1	5.8	
			3.3 V ±0.3 V			1	4.6	
Propagation delay time, output disable, \overline{OE} to Y	t _{dis}		1.8 V ±0.15 V			1.5	10.3	ns
			2.5 V ±0.2 V			1	5.3	
			2.7 V			1	6.2	
			3.3 V ±0.3 V			1.8	5.8	
Output skew time	t _{sk(o)}		3.3 V ±0.3 V				1	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This applies in the disabled state only.

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Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E1	6.00	6.20	0.236	0.244
A1	0.05	0.15	0.002	0.006	e	0.50 TYP		0.020 TYP	
b	0.17	0.27	0.007	0.011	L	0.50	0.75	0.020	0.030
D	12.40	12.60	0.488	0.496	L1	0.25 TYP		0.010 TYP	
E	7.90	8.30	0.311	0.327	L2	0.15 NOM		0.006 NOM	

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-153.
3. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.
4. Body dimensions do not include mold flash or protrusion not to exceed 0.15 millimeters (0.006 inches).

FIGURE 1. Case outline.

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(each 4-bit buffer)

Inputs		Output
\overline{OE}	A	Y
L	L	H
L	H	L
H	X	Z

H = High
L = Low
X = Immaterial
Z = High impedance state

FIGURE 2. Truth table.

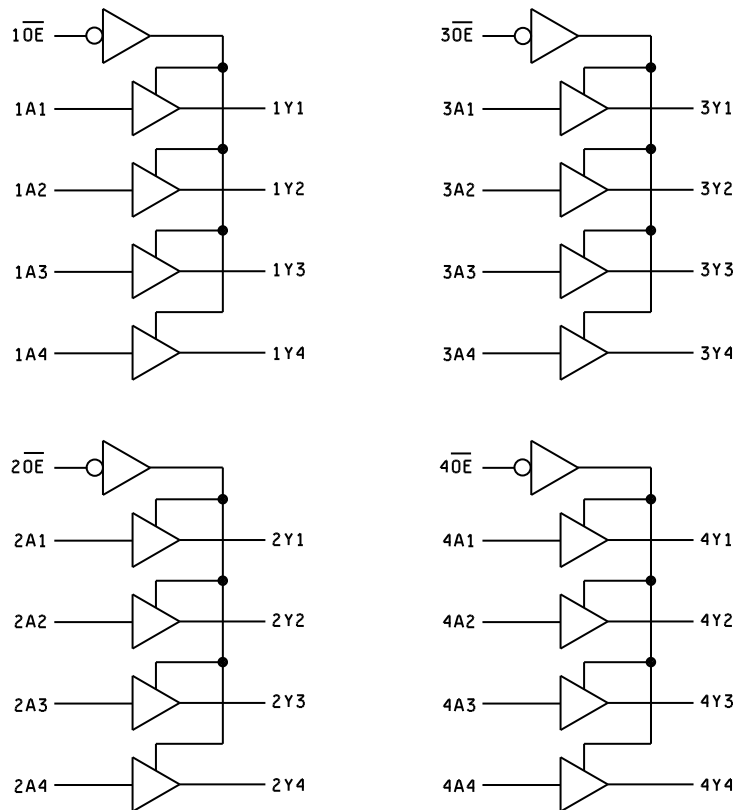


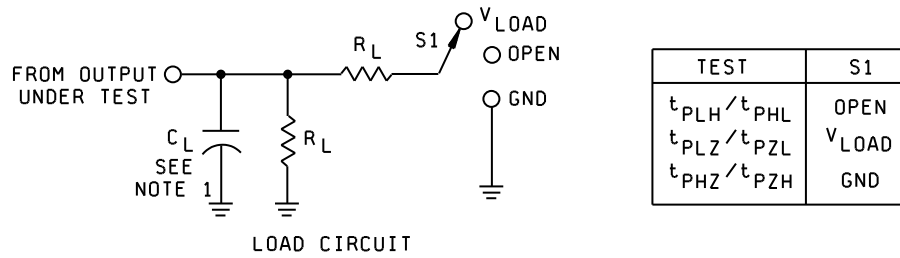
FIGURE 3. Logic diagram.

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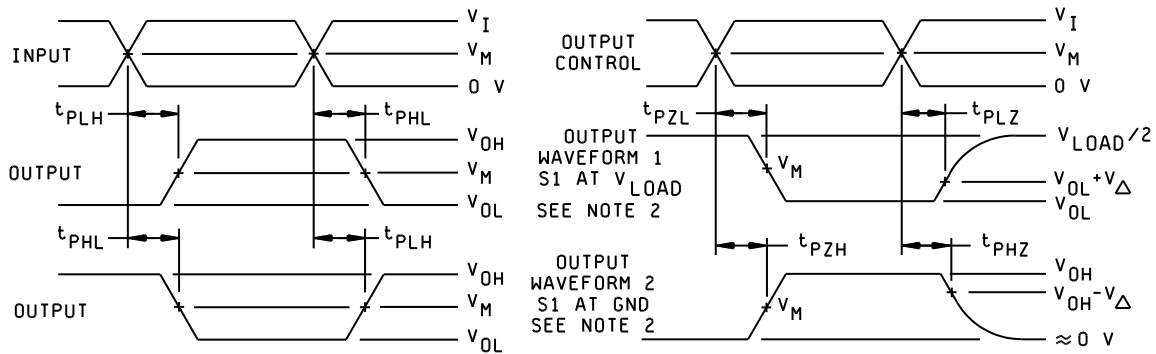
Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{1OE}$	25	$\overline{3OE}$
2	1Y1	26	4A4
3	1Y2	27	4A3
4	GND	28	GND
5	1Y3	29	4A2
6	1Y4	30	4A1
7	V _{cc}	31	V _{cc}
8	2Y1	32	3A4
9	2Y2	33	3A3
10	GND	34	GND
11	2Y3	35	3A2
12	2Y4	36	3A1
13	3Y1	37	2A4
14	3Y2	38	2A3
15	GND	39	GND
16	3Y3	40	2A2
17	3Y4	41	2A1
18	V _{cc}	42	V _{cc}
19	4Y1	43	1A4
20	4Y2	44	1A3
21	GND	45	GND
22	4Y3	46	1A2
23	4Y4	47	1A1
24	$\overline{4OE}$	48	$\overline{2OE}$

FIGURE 4. Terminal connections.

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V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V \pm 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\Omega$.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .

FIGURE 5. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04724-01XE	01295	CLVC16244AIDGGREP	C16244AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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