

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT octal bus transceiver with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C for device type 01, and -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/04723</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVTH245A-EP	3.3-V ABT octal bus transceiver with 3-state outputs
02	SN74LVTH245A-EP	3.3-V ABT octal bus transceiver with 3-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	JEDEC MO-153	Plastic small-outline
Y	20	JEDEC MO-150	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +4.6 V
Input voltage range (V_i).....	-0.5 V to 7 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_o)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high state (V_o).....	-0.5 V to $V_{CC} + 0.5 V$ 2/
Current into any output in the low state (I_o)	128 mA
Current into any output in the high state (I_o).....	64 mA 3/
Input clamp current (I_{IK}) ($V_i < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_o < 0$).....	-50 mA
Package thermal impedance (θ_{JA}):	
Case outline X.....	83°C/W 4/
Case outline Y.....	69.5°C/W 4/
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	2.7 V to 3.6 V
Minimum high level input voltage (V_{IH}).....	2 V
Maximum low level input voltage (V_{IL}).....	0.8 V
Maximum input voltage (V_i).....	5.5 V
Maximum high level output current (I_{OH})	-32 mA
Maximum low level output current (I_{OL})	64 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) (Outputs enabled)	10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$).....	200 μ s/V
Operating free-air temperature range (T_A):	
Device type 01	-40°C to +85°C
Device type 02	-55°C to +125°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 3/ This current flows only when the output is in the high state and $V_o > V_{CC}$.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V _{IK}	I _I = -18 mA	2.7 V	25°C, Device 01: -40°C to +85°C, Device 02: -55°C to +125°C	All		-1.2	V
High level output voltage	V _{OH}	I _{OH} = -100 μA	2.7 V to 3.6 V		All	V _{CC} - 0.2		V
		I _{OH} = -8 mA	2.7 V			2.4		
		I _{OH} = -24 mA	3 V		02	2		
		I _{OH} = -32 mA			01	2		
Low level output voltage	V _{OL}	I _{OL} = 100 μA	2.7 V		All		0.2	V
		I _{OL} = 24 mA					0.5	
		I _{OL} = 16 mA	3.0 V			0.4		
		I _{OL} = 32 mA				0.5		
		I _{OL} = 48 mA		02		0.55		
		I _{OL} = 64 mA		01		0.55		
Input current	I _I	Control inputs V _I = 5.5 V	0 V or 3.6 V	All		10	μA	
		Control inputs V _I = V _{CC} or GND	3.6 V			±1		
		A or B ports <u>2/</u> V _I = 5.5 V	3.6 V			20		
		A or B ports <u>2/</u> V _I = V _{CC}				1		
		A or B ports <u>2/</u> V _I = 0 V				-5		
Input/output power-off leakage current	I _{off}	V _I or V _O = 0 V to 4.5 V	0 V	01		±100	μA	
Input current (hold)	I _{I(hold)}	A or B ports V _I = 0.8 V	3 V	All	75		μA	
		A or B ports V _I = 2 V				-75		
		A or B ports V _I = 0 V to 3.6 V <u>3/</u>	3.6 V		01			+500 -750

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
3-state output current power-up	I _{OZPU}	V _O = 0.5 V to 3 V OE = don't care	0 V to 1.5 V	25°C, Device 01: -40°C to +85°C, Device 02: -55°C to +125°C	All		±100	μA
3-state output current power-down	I _{OZPD}	V _O = 0.5 V to 3 V OE = don't care	1.5 V to 0 V				±100	μA
Quiescent supply current	I _{CC}	Outputs high. V _I = V _{CC} or GND I _O = 0 A	3.6 V					0.19
		Outputs low. V _I = V _{CC} or GND I _O = 0 A			5			
		Outputs disabled. V _I = V _{CC} or GND I _O = 0 A			0.19			
Quiescent supply current delta	ΔI _{CC} 4/	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			0.2	mA	
Input capacitance	C _i	V _I = 3 V or 0 V	3.3 V	25°C	4 TYP		pF	
Input/output capacitance	C _{io}	V _O = 3 V or 0 V			9 TYP		pF	
Propagation delay time, A or B to B or A	t _{PLH}	C _L = 50 pF See figure 5	2.7 V	25°C, Device 01: -40°C to +85°C, Device 02: -55°C to +125°C	01		4	ns
			3.3 V ±0.3 V		02		6	
					2.7 V	01	1.2	
			02			1.2	5.5	
	t _{PHL}		2.7 V		01		4	
			3.3 V ±0.3 V		02		6	
					01	1.2	3.5	
			02		1.2	5.5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Propagation delay <u>time</u> , output enable, OE to A or B	t _{PZH}	C _L = 50 pF See figure 5	2.7 V	25°C, Device 01: -40°C to +85°C, Device 02: -55°C to +125°C	01		7.1	ns
			3.3 V ±0.3 V		02		9.5	
					01	1.3	5.5	
			02		1.3	7.9		
	t _{PZL}		2.7 V		01		6.5	
			3.3 V ±0.3 V		02		7.9	
					01	1.7	5.5	
			02		1.7	7		
Propagation delay <u>time</u> , output disable, OE to A or B	t _{PHZ}	2.7 V	01		6.5	ns		
		3.3 V ±0.3 V	02		7.8			
			01	2.2	5.9			
		02	2.2	7.2				
	t _{PLZ}	2.7 V	01		5.1			
		3.3 V ±0.3 V	02		7.2			
			01	2.2	5			
		02	2.2	7.1				

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

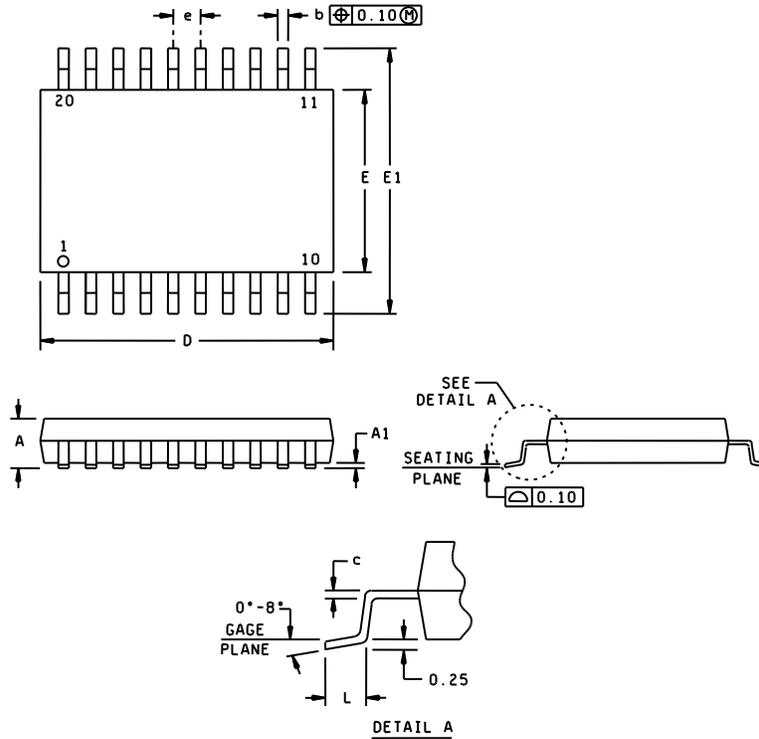
2/ Unused terminals are at V_{CC} or GND.

3/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

4/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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Case X



NOTES:

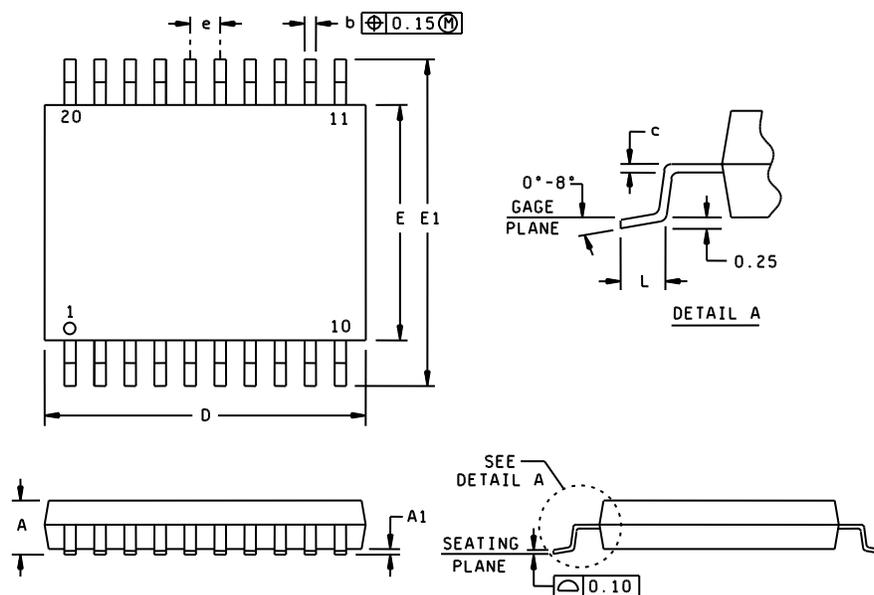
1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-153.
3. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.
4. Body dimensions do not include mold flash or protrusion not to exceed 0.15 millimeters (0.006 inches).

Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 TYP		0.026 TYP	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	6.40	6.60	0.252	0.260					

FIGURE 1. Case outline.

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Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	2.00	---	0.079	E	5.00	5.60	0.197	0.220
A1	0.05	---	0.002	---	E1	7.40	8.20	0.291	0.323
b	0.22	0.38	0.009	0.015	e	0.65 TYP		0.026 TYP	
c	0.09	0.25	0.004	0.010	L	0.55	0.95	0.022	0.037
D	6.90	7.50	0.272	0.295					

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-150.
3. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.
4. Body dimensions do not include mold flash or protrusion not to exceed 0.15 millimeters (0.006 inches).

FIGURE 1. Case outlines - Continued.

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Inputs		Operation
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High
L = Low
X = Immaterial

FIGURE 2. Function table.

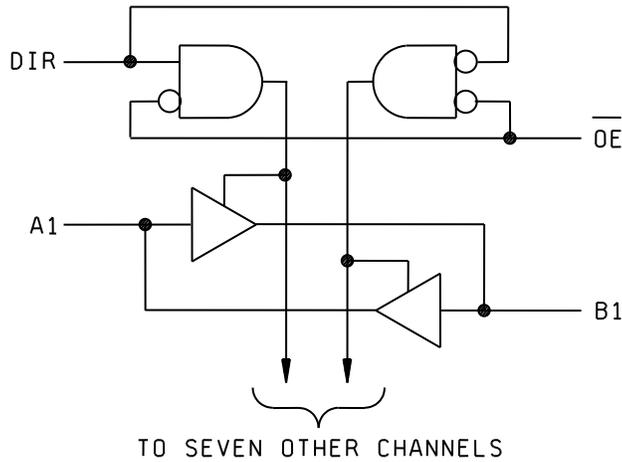


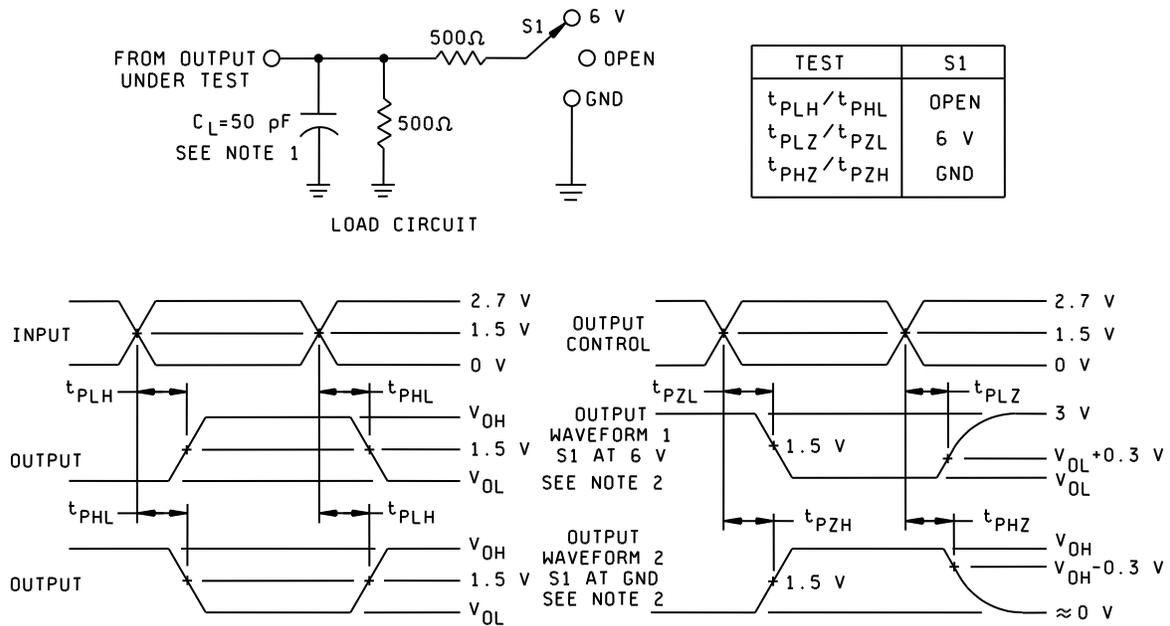
FIGURE 3. Logic diagram.

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Device types	01 and 02
Case outlines	X and Y
Terminal number	Terminal symbol
1	DIR
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	A8
10	GND
11	B8
12	B7
13	B6
14	B5
15	B4
16	B3
17	B2
18	B1
19	\overline{OE}
20	V _{CC}

FIGURE 4. Terminal connections.

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NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50\Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04723-01XE	01295	SN74LVTH245AIPWREP	LH245AEP
V62/04723-02YE	01295	SN74LVTH245AMDBREP	LH245AMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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