

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct lead finish. - CFS	05-12-02	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	11-07-22	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-09-20	Thomas M. Hess



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

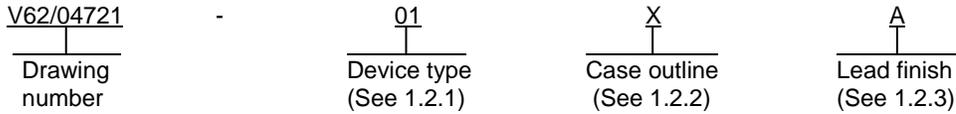
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REV STATUS OF PAGES	REV	C	C	C	C	C	C	C	C	C	C	C	C	C						
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PMIC N/A	PREPARED BY Charles F. Saffle	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 04-06-09	CHECKED BY Charles F. Saffle	TITLE MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 3.3-V ABT 32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/04721
	REV	C	PAGE 1 OF 12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT 32-bit transparent D-type latch with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVTH32373-EP	3.3-V ABT 32-bit transparent D-type latch with 3-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	96	JEDEC MO-205	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 2

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +4.6 V
Input voltage range (V_I)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_O)	-0.5 V to 7 V 2/
Voltage range applied to any output in the high state (V_O)	-0.5 V to $V_{CC} + 0.5$ V 2/
Current into any output in the low state (I_O)	128 mA
Current into any output in the high state (I_O)	64 mA 3/
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Package thermal impedance (θ_{JA})	40°C/W 4/
Storage temperature range (T_{STG})	-65°C to +150°C 5/

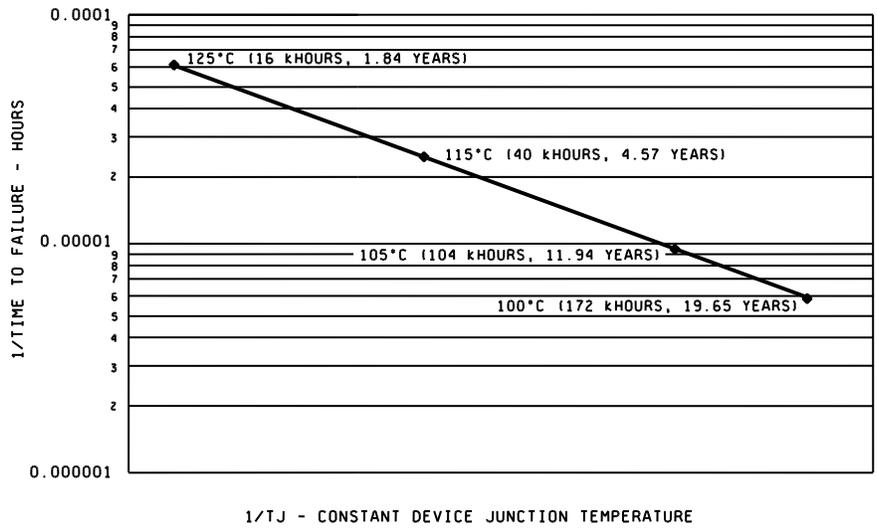


FIGURE 1. Estimated Wirebond Life
Based on Elevated-Temperature Kirkendall-Voiding Failure Mode

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 3/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See figure 1 for additional information on thermal derating.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 3

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC})	2.7 V to 3.6 V
Minimum high level input voltage (V_{IH})	2 V
Maximum low level input voltage (V_{IL})	0.8 V
Maximum input voltage (V_i)	5.5 V
Maximum high level output current (I_{OH})	-32 mA
Maximum low level output current (I_{OL})	64 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) (Outputs enabled).....	10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$).....	200 μ s/V
Operating free-air temperature range (T_A)	-40°C to +85°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 2.

3.5.2 Truth table. The truth table shall be as shown in figure 3.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 5.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 6.

1/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V _{IK}	I _I = -18 mA	2.7 V	25°C, -40°C to 85°C	All		-1.2	V
High level output voltage	V _{OH}	I _{OH} = -100 μA	2.7 V to 3.6 V			V _{CC} - 0.2		V
		I _{OH} = -8 mA	2.7 V	2.4				
		I _{OH} = -32 mA	3 V	2				
Low level output voltage	V _{OL}	I _{OL} = 100 μA	2.7 V			0.2	V	
		I _{OL} = 24 mA				0.5		
		I _{OL} = 16 mA	3 V			0.4		
		I _{OL} = 32 mA				0.5		
		I _{OL} = 64 mA				0.55		
Input current	I _I	V _I = 5.5 V	0 V or 3.6 V			10	μA	
		Control inputs. V _I = V _{CC} or GND	3.6 V			±1		
		Data inputs, V _I = V _{CC}				1		
		Data inputs, V _I = 0 V				-5		
Input/output power-off leakage current	I _{off}	V _I or V _O = 0 V to 4.5 V	0 V			±100	μA	
Input current (hold)	I _{I(hold)}	Data inputs, V _I = 0.8 V	3 V			75	μA	
		Data inputs, V _I = 2 V				-75		
		Data inputs. V _I = 0 V to 3.6 V 2/	3.6 V			±500		
Off state output current high	I _{OZH}	V _O = 3 V	3.6 V			5	μA	
Off state output current low	I _{OZL}	V _O = 0.5 V	3.6 V			-5	μA	
3-state output current power-up	I _{OZPU}	V _O = 0.5 V to 3 V OE = don't care	0 V to 1.5 V			±100	μA	
3-state output current power-down	I _{OZPD}	V _O = 0.5 V to 3 V OE = don't care	1.5 V to 0 V			±100	μA	
Quiescent supply current	I _{CC}	Outputs high. V _I = V _{CC} or GND, I _O = 0 A	3.6 V			0.38	mA	
		Outputs low. V _I = V _{CC} or GND, I _O = 0 A				10		
		Outputs disabled. V _I = V _{CC} or GND, I _O = 0 A				0.38		
Quiescent supply current delta	ΔI _{CC} 4/	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			0.2	mA	
Input capacitance	C _i	V _I = 3 V or 0 V	3.3 V	25°C		3 TYP		pF
Output capacitance	C _o	V _O = 3 V or 0 V				9 TYP		pF

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 5

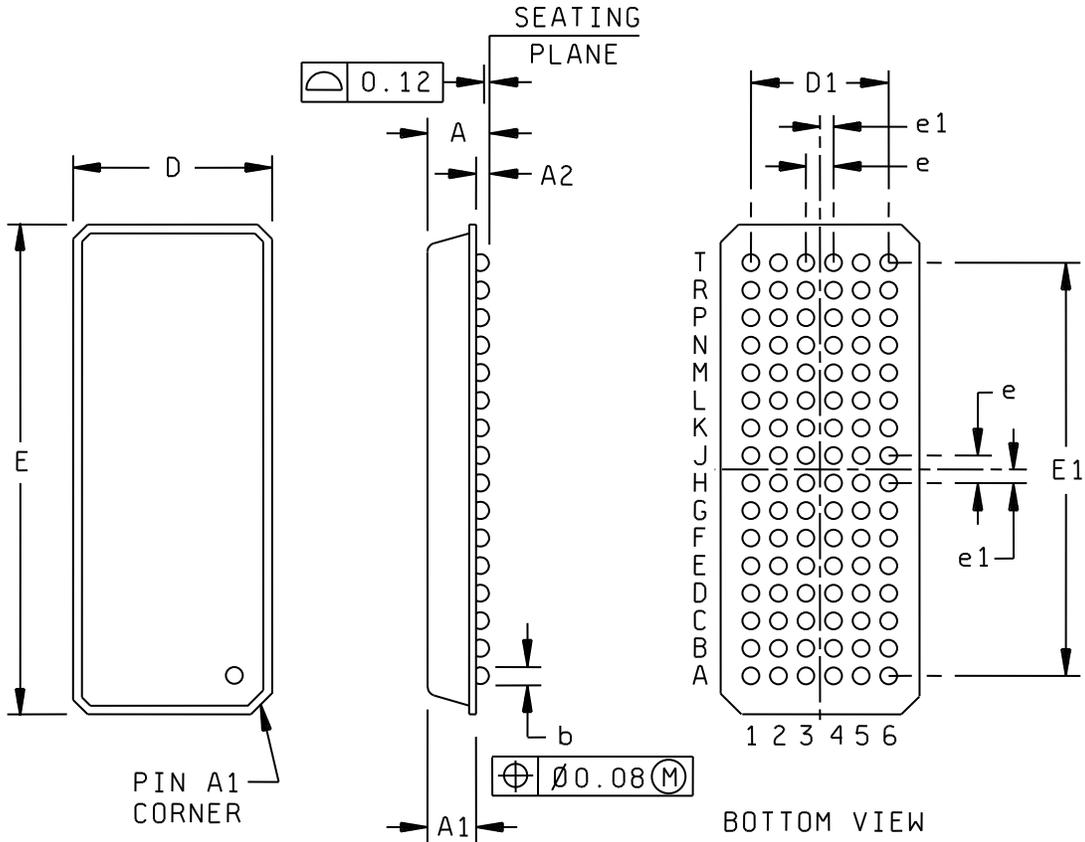
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Pulse duration, LE high	t _w	See figure 6.	2.7 V	25°C, -40°C to 85°C	All	3		ns
			3.3 V ±0.3 V			3		
Setup time, data before LE↓	t _{su}		2.7 V			0.6		
			3.3 V ±0.3 V			1		
Hold time, data after LE↓	t _h		2.7 V			1.1		
			3.3 V ±0.3 V			1		
Propagation delay time, D to Q	t _{PLH}		2.7 V				4.2	
			3.3 V ±0.3 V			1.5	3.8	
	t _{PHL}		2.7 V				4	
	3.3 V ±0.3 V		1.5			3.6		
Propagation delay time, LE to Q	t _{PLH}		2.7 V				4.8	
			3.3 V ±0.3 V			2.1	4.3	
	t _{PHL}		2.7 V				4	
	3.3 V ±0.3 V		2.1			4		
Propagation delay time, output enable, OE to Q	t _{PZH}		2.7 V				5.1	
			3.3 V ±0.3 V			1.5	4.3	
	t _{PZL}		2.7 V				4.7	
	3.3 V ±0.3 V		1.5			4.3		
Propagation delay time, output disable, OE to Q	t _{PHZ}		2.7 V				5.4	
			3.3 V ±0.3 V			2.4	5	
	t _{PLZ}		2.7 V				4.8	
	3.3 V ±0.3 V		2			4.7		
Output skew time	t _{sk(o)}		3.3 V ±0.3 V				0.5	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
- 3/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 6

Case X



NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-205 variation CC.
3. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.
4. This package is tin-lead (SnPb).

FIGURE 2. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04721</p>
		<p>REV C</p>	<p>PAGE 7</p>

Case X

Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.40	---	0.551	D1	4.00 NOM		0.157 NOM	
A1	0.85	0.95	0.033	0.037	E	13.40	13.60	0.528	0.535
A2	0.35	0.45	0.014	0.018	E1	12.00 NOM		0.472 NOM	
b	0.45	0.55	0.018	0.022	e	0.80 NOM		0.031 NOM	
D	5.40	5.60	0.213	0.220	e1	0.40 NOM		0.016 NOM	

FIGURE 2. Case outline - Continued.

(each 8-bit latch)

Inputs			Output
OE	LE	\overline{D}	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

H = High
 L = Low
 X = Immaterial
 Z = High-impedance state
 Q₀ = Level of Q before the indicated steady-state input conditions were established.

FIGURE 3. Truth table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 8

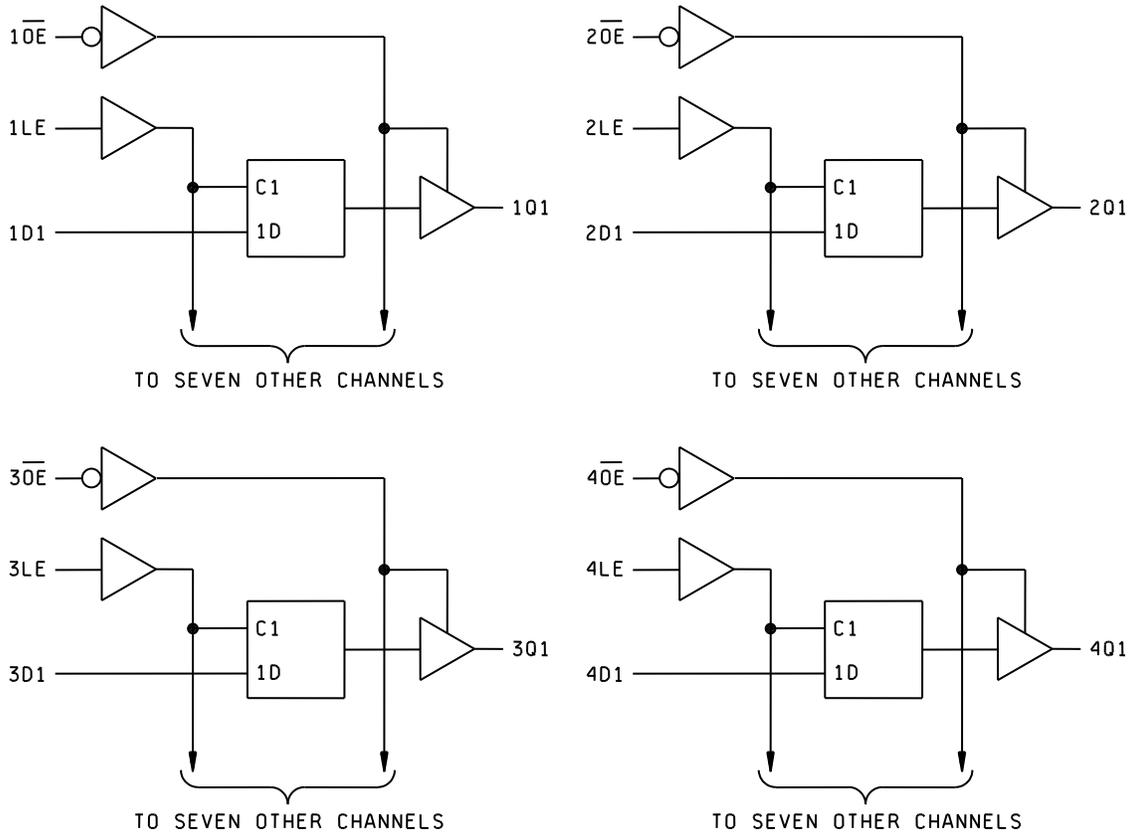


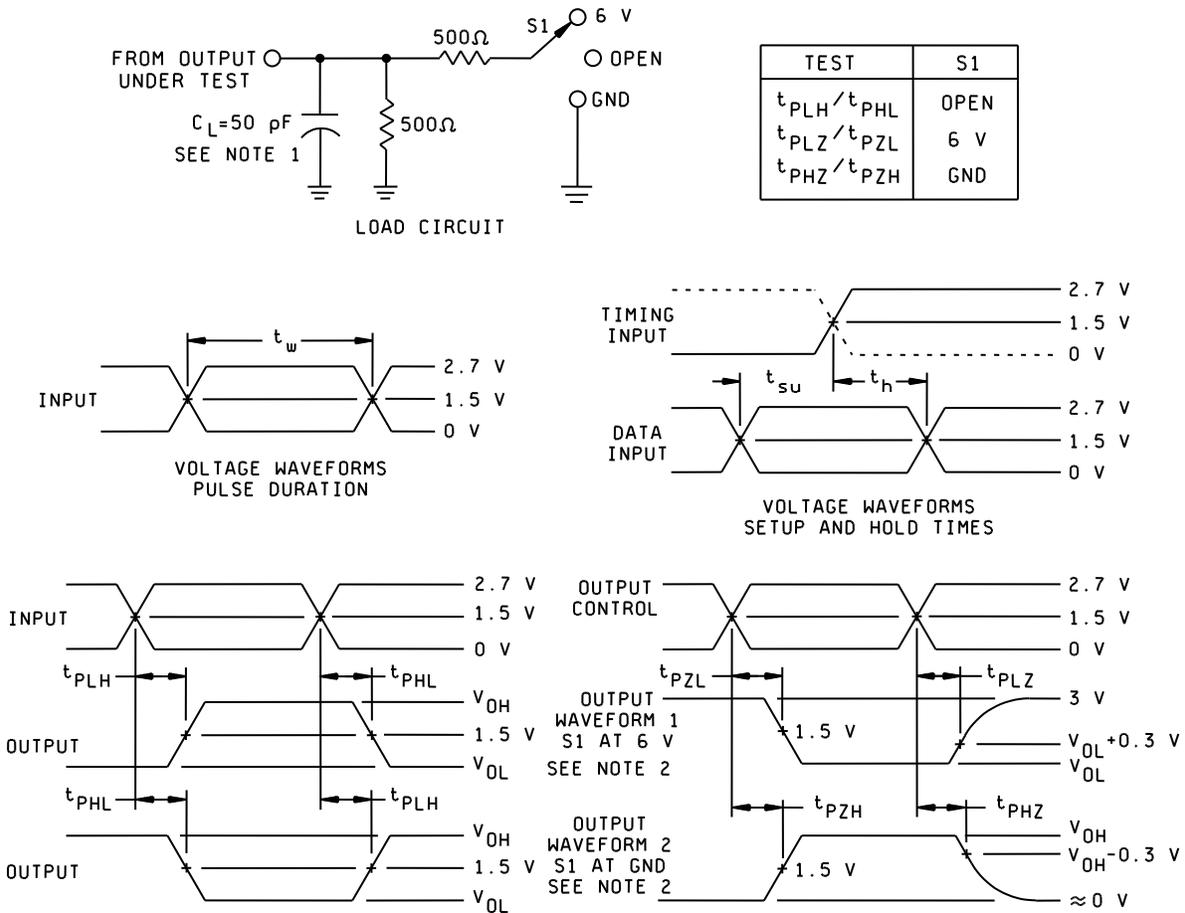
FIGURE 4. Logic diagram.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/04721</p>
		<p>REV C</p>	<p>PAGE 9</p>

Device type		01					
Case outline		X					
Terminal number	Terminal symbol						
A1	1Q2	E1	2Q2	J1	3Q2	N1	4Q2
A2	1Q1	E2	2Q1	J2	3Q1	N2	4Q1
A3	1OE	E3	GND	J3	3OE	N3	GND
A4	1LE	E4	GND	J4	3LE	N4	GND
A5	1D1	E5	2D1	J5	3D1	N5	4D1
A6	1D2	E6	2D2	J6	3D2	N6	4D2
B1	1Q4	F1	2Q4	K1	3Q4	P1	4Q4
B2	1Q3	F2	2Q3	K2	3Q3	P2	4Q3
B3	GND	F3	1V _{cc}	K3	GND	P3	2V _{cc}
B4	GND	F4	1V _{cc}	K4	GND	P4	2V _{cc}
B5	1D3	F5	2D3	K5	3D3	P5	4D3
B6	1D4	F6	2D4	K6	3D4	P6	4D4
C1	1Q6	G1	2Q6	L1	3Q6	R1	4Q6
C2	1Q5	G2	2Q5	L2	3Q5	R2	4Q5
C3	1V _{cc}	G3	GND	L3	2V _{cc}	R3	GND
C4	1V _{cc}	G4	GND	L4	2V _{cc}	R4	GND
C5	1D5	G5	2D5	L5	3D5	R5	4D5
C6	1D6	G6	2D6	L6	3D6	R6	4D6
D1	1Q8	H1	2Q7	M1	3Q8	T1	4Q7
D2	1Q7	H2	2Q8	M2	3Q7	T2	4Q8
D3	GND	H3	2OE	M3	GND	T3	4OE
D4	GND	H4	2LE	M4	GND	T4	4LE
D5	1D7	H5	2D8	M5	3D7	T5	4D8
D6	1D8	H6	2D7	M6	3D8	T6	4D7

FIGURE 5. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 10



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50\Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 6. Timing waveforms and test circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 11

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04721-01XA	01295	CLVTH32373IGKEREP	L373EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04721
		REV C	PAGE 12