

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device type 02 and case outline Y. - PHN	06-08-22	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-08-24	Thomas M. Hess



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

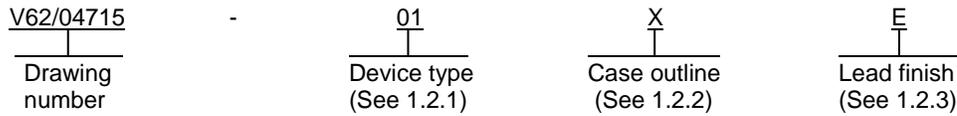
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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B	B	B						
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PMIC N/A	PREPARED BY Charles F. Saffle	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	
Original date of drawing YY-MM-DD 04-05-04	CHECKED BY Charles F. Saffle	TITLE MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 3.3-V ABT 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/04715
	REV B		PAGE 1 OF 12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT 16-bit registered transceiver with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C and an extended operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01 <u>1/</u>	SN74LVTH16543-EP	3.3-V ABT 16-bit registered transceiver with 3-state outputs
02 <u>2/</u>	SN74LVTH16543-EP	3.3-V ABT 16-bit registered transceiver with 3-state outputs

1.2.2 Case outline. The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	56	MO-153	Plastic small-outline
Y	56	MO-118	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium

1/ Device type 01 operates at -40°C to +85°C.
2/ Device type 02 operates at -55°C to +125°C.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 2

1.3 Absolute maximum ratings. 3/

Supply voltage range (V_{CC})	-0.5 V to 4.6 V	
Input voltage range (V_I)	-0.5 V to 7.0 V	4/
Voltage range applied to any output in the high-impedance or power-off state (V_O)	-0.5 V to 7 V	4/
Voltage range applied to any output in the high state (V_O)	-0.5 V to $V_{CC} + 0.5 V$	4/
Current into any output in the low state (I_{OL})	128 mA	
Current into any output in the high state (I_{OH})	64 mA	5/
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA	
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA	
Package thermal impedance (θ_{JA}): 6/		
Case X	81°C/W	
Case Y	73.5°C/W	
Storage temperature range (T_{STG})	-65°C to 150°C	7/

1.4 Recommended operating conditions. 8/

Supply voltage range (V_{CC})	2.7 V to 3.6 V
Minimum high level input voltage (V_{IH})	2 V
Maximum low level input voltage (V_{IL})	0.8 V
Maximum input voltage (V_I)	5.5 V
Maximum high level output current (I_{OH})	-32 mA
Maximum low level output current (I_{OL})	64 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) (Outputs enabled)	10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$)	200 μ s/V
Operating free-air temperature range (T_A):	
Device type 01	-40°C to +85°C
Device type 02	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

- 3/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 4/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 5/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 6/ The package thermal impedance is calculated in accordance with JESD 51.
- 7/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer data for additional information on enhanced plastic packaging
- 8/ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 3

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions -40°C ≤ T _A ≤ +85°C 2/ -55°C ≤ T _A ≤ +125°C 3/ 4/		V _{CC}	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V _{IK}	I _I = -18 mA		2.7 V	All		-1.2	V
High level output voltage	V _{OH}	I _{OH} = -100 μA		2.7 V to 3.6 V		V _{CC} - 0.2		V
		I _{OH} = -8 mA		2.7 V		2.4		
		I _{OH} = -32 mA		3.0 V		2		
Low level output voltage	V _{OL}	I _{OL} = 100 μA		2.7 V			0.2	V
		I _{OL} = 24 mA		2.7 V		0.5		
		I _{OL} = 16 mA		3.0 V		0.4		
		I _{OL} = 32 mA		3.0 V		0.5		
		I _{OL} = 64 mA		3.0 V	01	0.55		
Input current	Control inputs	I _I	V _I = V _{CC} or GND		3.6 V	All	±1	μA
	A or B port		V _I = 5.5 V		0 V or 3.6 V			
			V _I = 5.5 V		3.6 V	01	20	
			V _I = 5.5 V			02	100	
			V _I = V _{CC}			All	1	
			V _I = 0				-5	
Input/output power-off leakage current	I _{off}	V _I or V _O = 0 to 4.5 V		0 V	01	±100	μA	
Input current (hold)	A or B port	I _{I(hold)}	V _I = 0.8 V		3.0 V	All	75	μA
			V _I = 2 V				-75	
			V _I = 0 V to 3.6 V		3.6 V 6/			
3-state output current power-up			V _O = 0.5 V to 3 V, OE = don't care	0 V to 1.5 V		±100	μA	
3-state output current power-down				1.5 V to 0 V		±100	μA	
Quiescent supply current	I _{CC}	I _O = 0, V _I = V _{CC} or GND	Outputs high	3.6 V			0.19	mA
			Outputs low				5	
			Outputs disabled				0.19	
Quiescent supply current delta	ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		3.0 V to 3.6 V		0.2	mA	
Input capacitance	C _i	V _I = 3 V or 0 V, T _A = 25°C		3.3 V		4 Typ	pF	
Input/output capacitance	C _{i/o}	V _O = 3 V or 0 V, T _A = 25°C		3.3 V		10 Typ		

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 5

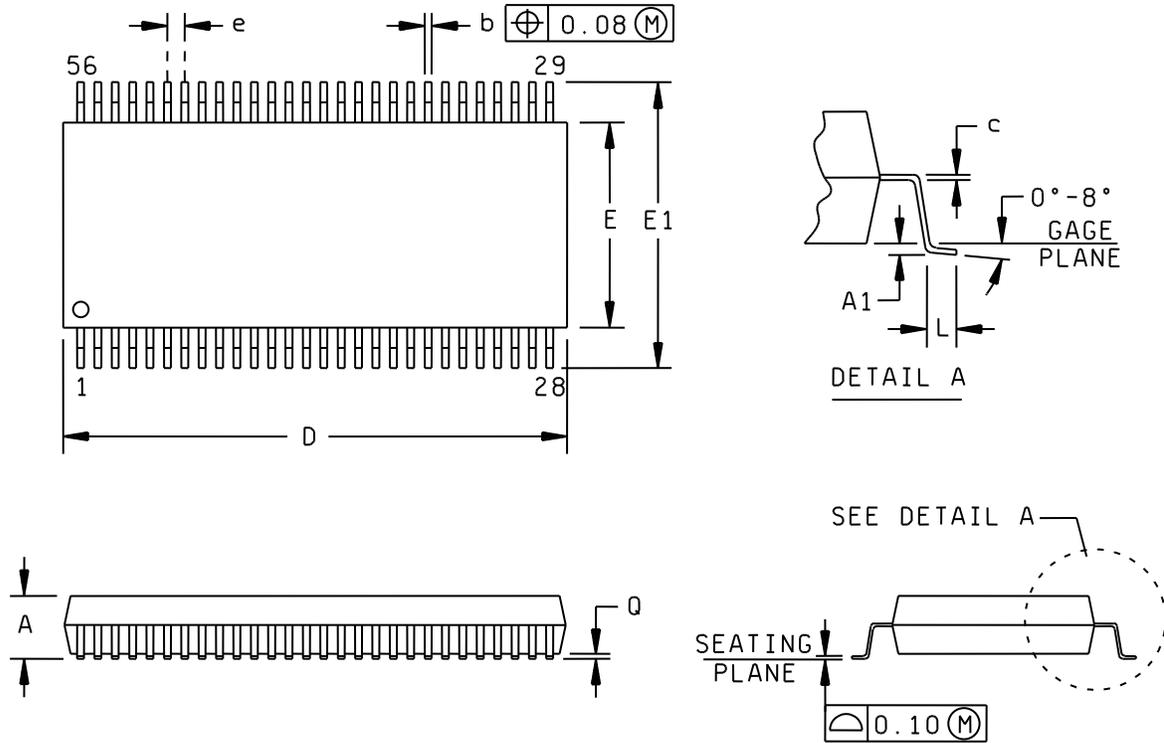
TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Device type 01				Device type 02				Unit
			V _{CC} = 3.3 V ±0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ±0.3 V		V _{CC} = 2.7 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
Timing requirements 4/ (See figure 5)											
Pulse duration, \overline{LEAB} or \overline{LEBA} low		t _w	3.3		3.3		3.3		3.3		ns
Setup time	A or B before \overline{LEAB} ↑ or \overline{LEBA} ↑	Data high	0.5		0.5		0.7		0.9		
		Data low	0.8		1.3		1.2		1.9		
	A or B before \overline{CEAB} ↑ or \overline{CEBA} ↑	Data high	0		0		0.5		0.8		
		Data low	0.6		1.1		1.1		1.9		
Hold time	A or B before \overline{LEAB} ↑ or \overline{LEBA} ↑	Data high	1.5		0.7		1.5		1.0		
		Data low	1.2		1.3		1.2		1.5		
	A or B before \overline{CEAB} ↑ or \overline{CEBA} ↑	Data high	1.7		0.9		1.7		1.1		
		Data low	1.6		1.8		1.6		1.9		
Switching characteristics 8/ (see figure 5)											
Propagation delay time, from input A or B to output B or A		t _{PLH}	1.2	3.2		3.7	1.2	4.7		6.5	ns
		t _{PHL}	1.2	3.2		3.7	1.2	5.4		6.5	
Propagation delay time, from input \overline{LE} to output A or B		t _{PLH}	1.3	3.9		4.9	1.3	7.3		7.8	
		t _{PHL}	1.3	3.9		4.9	1.3	6.9		7.8	
Enable time, from input \overline{OE} to output A or B		t _{PZH}	1.3	4.3		5.4	1.3	6.5		7.4	
		t _{PZL}	1.3	4.3		5.4	1.3	6.7		7.4	
Disable time, from input \overline{OE} to output A or B		t _{PHZ}	2	4.7		5.2	2	5.7		7.2	
		t _{PLZ}	2	4.4		4.5	2	5.1		6.9	
Enable time, from input \overline{CE} to output A or B		t _{PZH}	1.3	4.5		5.6	1.3	6.5		7.6	
		t _{PZL}	1.3	4.5		5.6	1.3	6.4		7.6	
Disable time, from input \overline{CE} to output A or B		t _{PHZ}	2	4.9		5.4	2	5.3		7.4	
		t _{PLZ}	2	4.7		4.9	2	5.1		6.9	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ For device type 01.
- 3/ For device type 02.
- 4/ Over recommended operating free air temperature range (unless otherwise noted).
- 5/ Unused terminals are at V_{CC} or GND.
- 6/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
- 7/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
- 8/ Over recommended operating free air temperature range, C_L = 50 pF (unless otherwise noted).

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 6

Case X



Dimensions					
Symbol	Millimeter		Symbol	Millimeter	
	Min	Max		Min	Max
A		1.20	E	6.00	6.20
A1	0.25 TYP		E1	7.90	8.30
b	0.17	0.27	e	0.50 BSC	
c	0.15 NOM		L	0.50	0.75
D	13.90	14.10	Q	0.05	0.15

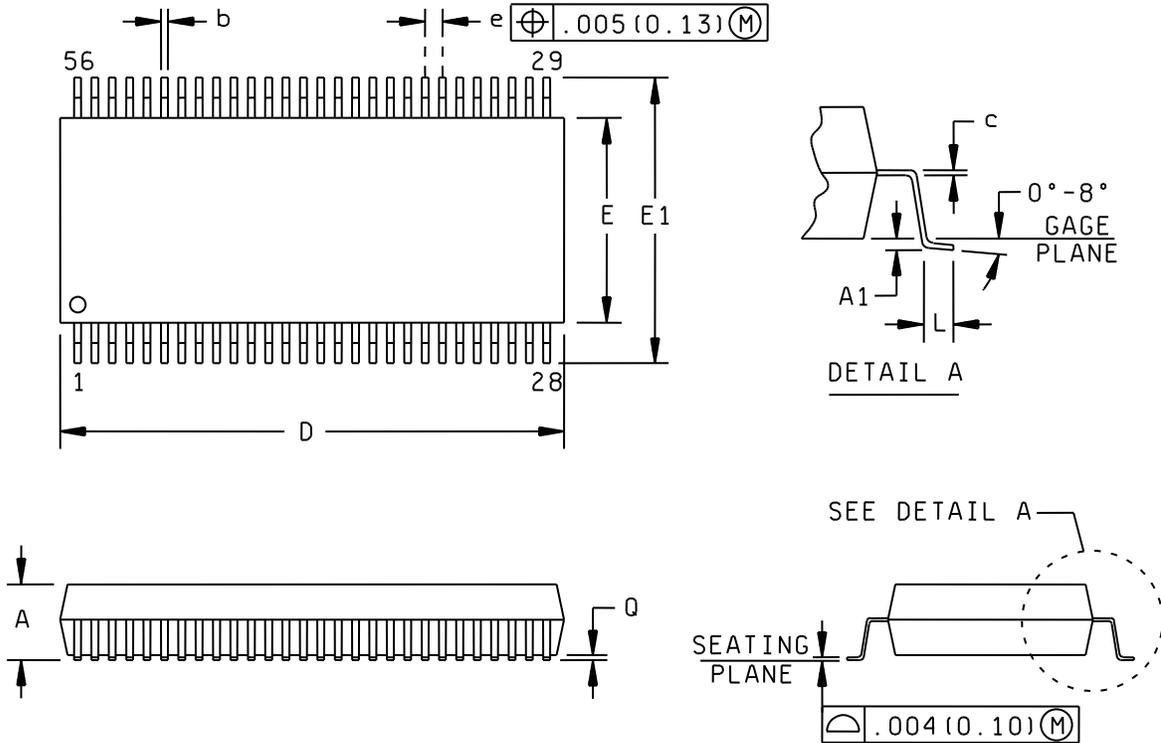
NOTES:

1. All linear dimensions are in millimeters.
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 7

Case Y



Dimensions									
Symbol	Inch		Millimeter		Symbol	Inch		Millimeter	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.110		2.79	E	.291	.299	7.39	7.59
A1	.010 Typ		0.25 Typ		E1	.395	.420	10.03	10.67
b	.008	.013	0.20	0.34	e	.025 BSC		0.63 BSC	
c	.005	.010	0.13	0.25	L	.020	.040	0.51	1.02
D	.720	.730	18.29	18.54	Q	.008		0.20	

NOTES:

1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed .006 inch (0.15 millimeter).
4. Fall within JEDEC MO-118.

FIGURE 1. Case outline - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 8

Function table 1/

Inputs				Output B
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ 2/
L	L	L	L	L
L	L	L	H	H

H = High voltage level
X = Immaterial

L = Low voltage level
Z = High-impedance state

- 1/ A-to-B data flow is shown; B to A flow control is the same, except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .
- 2/ Output level before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

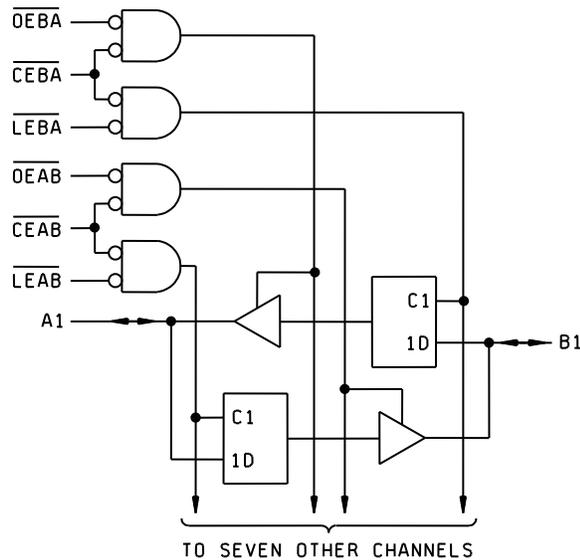


FIGURE 3. Logic diagram.

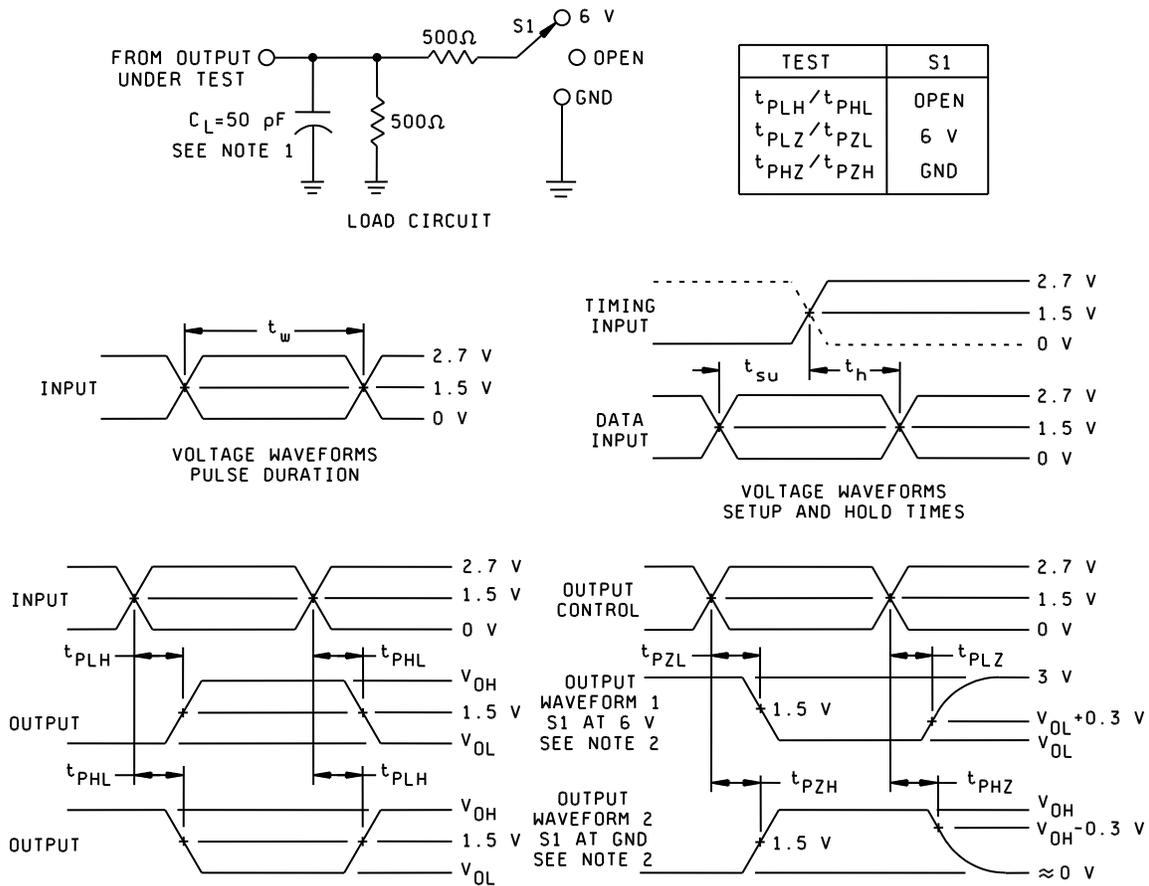
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 9

Case X and Y

Terminal number	Terminal symbol						
1	1 \overline{OEAB}	15	2A1	29	2 \overline{OEBA}	43	1B8
2	1 \overline{LEAB}	16	2A2	30	2 \overline{LEBA}	44	1B7
3	1 \overline{CEAB}	17	2A3	31	2 \overline{CEBA}	45	1B6
4	GND	18	GND	32	GND	46	GND
5	1A1	19	2A4	33	2B8	47	1B5
6	1A2	20	2A5	34	2B7	48	1B4
7	V _{CC}	21	2A6	35	V _{CC}	49	1B3
8	1A3	22	V _{CC}	36	2B6	50	V _{CC}
9	1A4	23	2A7	37	2B5	51	1B2
10	1A5	24	2A8	38	2B4	52	1B1
11	GND	25	GND	39	GND	53	GND
12	1A6	26	2 \overline{CEAB}	40	2B3	54	1 \overline{CEBA}
13	1A7	27	2 \overline{LEAB}	41	2B2	55	1 \overline{LEBA}
14	1A8	28	2 \overline{OEAB}	42	2B1	56	1 \overline{OEBA}

FIGURE 4. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 10



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, and $t_f \leq 2.5 \text{ ns}$.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 11

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Vendor item drawing administrative control number ^{1/}	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04715-01XE	01295	CLVTH16543IDGGREP	LH16543EP
V62/04715-02YE	01295	CLVTH16543MDLREP	LH16543MEP

^{1/} The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04715
		REV B	PAGE 12