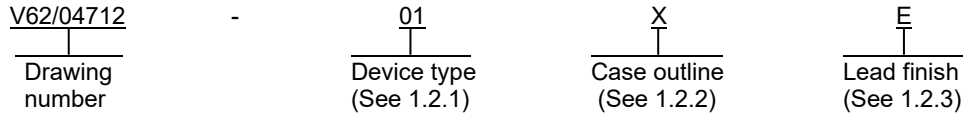




1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT 16-bit transparent D-type latch with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C for device type 01 and extended operating temperature range of -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01 <u>1/</u>	SN74LVTH16373-EP	3.3-V ABT 16-bit transparent D-type latch with 3-state outputs
02 <u>2/</u>	SN74LVTH16373-EP	3.3-V ABT 16-bit transparent D-type latch with 3-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	48	JEDEC MO-153	Plastic small-outline
Y	48	JEDEC MO-118	Plastic small-outline
Z	56	JEDEC MO-225	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Operates at -40°C to +85°C.  
2/ Operates at -55°C to +125°C.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		<b>REV E</b>	<b>PAGE 2</b>

1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to 4.6 V
Input voltage range ( $V_i$ ) .....	-0.5 V to 7 V 2/
Voltage range applied to any output in the high-impedance or power-off state ( $V_o$ ) .....	-0.5 V to 7 V 2/
Voltage range applied to any output in the high state ( $V_o$ ) .....	-0.5 V to $V_{CC} + 0.5 V$ 2/
Maximum current into any output in the low state ( $I_o$ ) .....	128 mA
Maximum current into any output in the high state ( $I_o$ ) .....	64 mA 3/
Input clamp current ( $I_{IK}$ ) ( $V_i < 0$ ) .....	-50 mA
Output clamp current ( $I_{OK}$ ) ( $V_o < 0$ ) .....	-50 mA
Storage temperature range ( $T_{STG}$ ) .....	-65°C to 150°C

1.4 ESD ratings.

Electrostatic discharge V(ESD)	
Human-body model (HBM), per A114-A .....	±4000 V
Charged device model (CDM), per JEDEC specification JESD22-C101 .....	±3000 V 4/
Machine model (MM), per A115-A .....	200 V

1.5 Recommended operating conditions. 5/

Supply voltage range ( $V_{CC}$ ) .....	2.7 V to 3.6 V
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V
Maximum low level input voltage ( $V_{IL}$ ) .....	0.8 V
Maximum input voltage ( $V_i$ ) .....	5.5 V
Maximum high level output current ( $I_{OH}$ ) .....	-32 mA
Maximum low level output current ( $I_{OL}$ ) .....	64 mA
Maximum input transition rise or fall rate ( $\Delta t/\Delta v$ ) (Outputs enabled) .....	10 ns/V
Minimum power-up ramp rate ( $\Delta t/\Delta V_{CC}$ ) .....	200 $\mu$ s/V
Operating free-air temperature range ( $T_A$ ):	
Device type 01 .....	-40°C to +85°C
Device type 02 .....	-55°C to +125°C

1.6 Thermal Information.

Thermal metric 6/ 7/	Case outline X	Case outline Y	Case outline Z	Units
Junction to ambient thermal resistance, $R_{\theta JA}$	68.9	60.3	62.5	°C/W
Junction to case (top) thermal resistance, $R_{\theta JCTop}$	14.6	31	24.7	
Junction to board thermal resistance, $R_{\theta JB}$	35.8	32.1	28.9	
Junction to top characterization parameter, $\Psi_{JT}$	2.4	9.3	0.9	
Junction to board characterization parameter, $\Psi_{JB}$	35.5	31.8	28	

- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 3/ This current flows only when the output is in the high state and  $V_o > V_{CC}$ .
- 4/ JESD document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- 5/ All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.
- 6/ For more information about traditional and new thermal metrics, see manufacturer the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
- 7/ The package thermal impedance is calculated in accordance with JESD 51-7.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		REV E	PAGE 3

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JESD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JEP157 – Recommended ESD-CDM target levels

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		<b>REV E</b>	<b>PAGE 4</b>

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ Device type: All	V <sub>CC</sub>	Limits		Unit
				Min	Max	
Input clamp voltage	V <sub>IK</sub>	I <sub>I</sub> = -18 mA	2.7 V		-1.2	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	2.7 V to 3.6 V	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -8 mA	2.7 V	2.4		
		I <sub>OH</sub> = -32 mA	3 V	2		
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V		0.2	V
		I <sub>OL</sub> = 24 mA			0.5	
		I <sub>OL</sub> = 16 mA	3 V		0.4	
		I <sub>OL</sub> = 32 mA			0.5	
		I <sub>OL</sub> = 64 mA			0.55	
Input current	I <sub>I</sub>	V <sub>I</sub> = 5.5 V	0 V or 3.6 V		10	μA
		Control inputs. V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		±1	
		Data inputs. V <sub>I</sub> = V <sub>CC</sub>			1	
		Data inputs. V <sub>I</sub> = 0 V			-5	
Input/output power-off leakage current	I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V	0 V		±100	μA
Input current (hold)	I <sub>I(hold)</sub>	Data inputs, V <sub>I</sub> = 0.8 V	3 V	75		μA
		Data inputs, V <sub>I</sub> = 2 V		-75		
		Data inputs. V <sub>I</sub> = 0 V to 3.6 V	3.6 V 3/		±650	
3-state output leakage current high	I <sub>OZH</sub>	V <sub>O</sub> = 3 V	3.6 V		5	μA
3-state output leakage current low	I <sub>OZL</sub>	V <sub>O</sub> = 0.5 V	3.6 V		-5	μA
3-state output current power-up	I <sub>OZPU</sub>	V <sub>O</sub> = 0.5 V to 3 V $\overline{OE}$ = don't care	0 V to 1.5 V		±100	μA
3-state output current power-down	I <sub>OZPD</sub>	V <sub>O</sub> = 0.5 V to 3 V $\overline{OE}$ = don't care	1.5 V to 0 V		±100	μA
Quiescent supply current	I <sub>CC</sub>	Outputs high. V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 A	3.6 V		0.19	mA
		Outputs low. V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 A			5	
		Outputs disabled. V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 A			0.19	
Quiescent supply current delta	ΔI <sub>CC</sub> 4/	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		0.2	mA
Input capacitance	C <sub>i</sub>	V <sub>I</sub> = 3 V or 0 V	3.3 V	3 TYP		pF
Output capacitance	C <sub>o</sub>	V <sub>O</sub> = 3 V or 0 V		9 TYP		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		REV E	PAGE 5

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 5/ Device type: 01	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>Timing Requirements</b>						
Pulse duration, LE high	t <sub>w</sub>	See figure 5.	2.7 V	3		ns
			3.3 V ±0.3 V	3		
Setup time, data before LE↓	t <sub>su</sub>		2.7 V	0.6		
			3.3 V ±0.3 V	1		
Hold time, data after LE↓	t <sub>h</sub>		2.7 V	1.1		
			3.3 V ±0.3 V	1		
<b>Switching Characteristics</b>						
Propagation delay time, D to Q	t <sub>PLH</sub>	C <sub>L</sub> = 50 pF See figure 5.	2.7 V		4.2	ns
			3.3 V ±0.3 V	1.5	3.8	
	t <sub>PHL</sub>		2.7 V		4	
			3.3 V ±0.3 V	1.5	3.6	
Propagation delay time, LE to Q	t <sub>PLH</sub>		2.7 V		4.8	ns
			3.3 V ±0.3 V	2.1	4.3	
	t <sub>PHL</sub>		2.7 V		4	
			3.3 V ±0.3 V	2.1	4	
Propagation delay time, output enable, OE to Q	t <sub>PZH</sub>		2.7 V		5.1	ns
			3.3 V ±0.3 V	1.5	4.3	
	t <sub>PZL</sub>	2.7 V		4.7		
		3.3 V ±0.3 V	1.5	4.3		
Propagation delay time, output disable, OE to Q	t <sub>PHZ</sub>	2.7 V		5.4	ns	
		3.3 V ±0.3 V	2.4	5		
	t <sub>PLZ</sub>	2.7 V		4.8		
		3.3 V ±0.3 V	2	4.7		
Output skew	t <sub>sk(0)</sub>	C <sub>L</sub> = 50 pF	3.3 V ±0.3 V		0.5	ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		REV E	PAGE 6

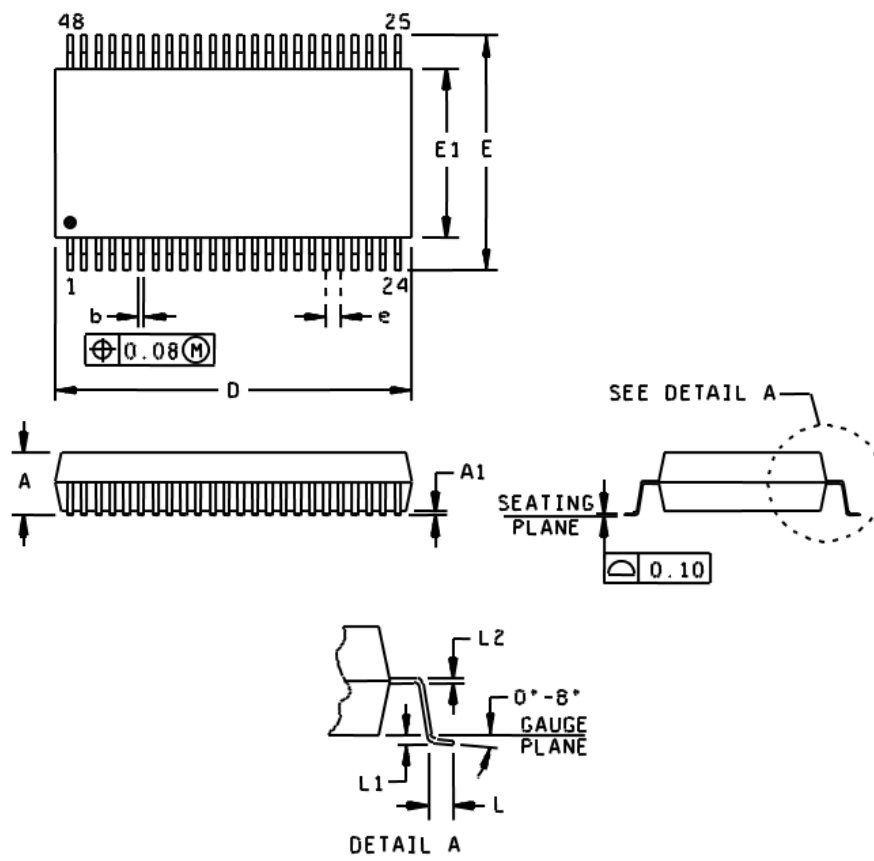
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 6/ Device type: 02	V <sub>CC</sub>	Limits		Unit	
				Min	Max		
<b>Timing Requirements</b>							
Pulse duration, LE high	t <sub>w</sub>	See figure 5.	2.7 V	3		ns	
			3.3 V ±0.3 V	3			
Setup time, data before LE↓	t <sub>su</sub>		2.7 V	1			
			3.3 V ±0.3 V	1.6			
Hold time, data after LE↓	t <sub>h</sub>		2.7 V	1.5			
			3.3 V ±0.3 V	1.4			
<b>Switching Characteristics</b>							
Propagation delay time, D to Q	t <sub>PLH</sub>	C <sub>L</sub> = 50 pF See figure 5.	2.7 V		5.5	ns	
	t <sub>PHL</sub>		3.3 V ±0.3 V	1.5	5		
Propagation delay time, LE to Q	t <sub>PLH</sub>		2.7 V		5.3	ns	
			3.3 V ±0.3 V	1.5	4.8		
Propagation delay time, output enable, $\overline{OE}$ to Q	t <sub>PHL</sub>		2.7 V		5.9		ns
			3.3 V ±0.3 V	2.1	5.4		
Propagation delay time, output disable, $\overline{OE}$ to Q	t <sub>PZH</sub>		2.7 V		4.9	ns	
			3.3 V ±0.3 V	2.1	4.9		
Propagation delay time, output enable, $\overline{OE}$ to Q	t <sub>PZL</sub>		2.7 V		7.9	ns	
			3.3 V ±0.3 V	1.5	7		
Propagation delay time, output disable, $\overline{OE}$ to Q	t <sub>PHZ</sub>	2.7 V		7.2	ns		
		3.3 V ±0.3 V	1.5	6.2			
Propagation delay time, output disable, $\overline{OE}$ to Q	t <sub>PLZ</sub>	2.7 V		7.9	ns		
		3.3 V ±0.3 V	1.8	7.2			
Output skew	t <sub>sk(0)</sub>	2.7 V		5.4	ns		
		3.3 V ±0.3 V	2	5.2			
Output skew	t <sub>sk(0)</sub>	C <sub>L</sub> = 50 pF	3.3 V ±0.3 V	0.5		ns	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over operating free-air temperature range (unless otherwise noted); all typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
- 3/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
- 4/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.
- 5/ Over recommended operating conditions (unless otherwise noted); T<sub>A</sub> = -40°C to 85°C.
- 6/ Over recommended operating conditions (unless otherwise noted); T<sub>A</sub> = -55°C to 125°C.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		REV E	PAGE 7

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E1	6.00	6.20	0.236	0.244
A1	0.05	0.15	0.002	0.006	e	0.50 BSC		0.020 BSC	
b	0.17	0.27	0.007	0.011	L	0.50	0.75	0.020	0.030
D	12.40	12.60	0.488	0.496	L1	0.25 TYP		0.010 TYP	
E	7.90	8.30	0.311	0.327	L2	0.15 NOM		0.006 NOM	

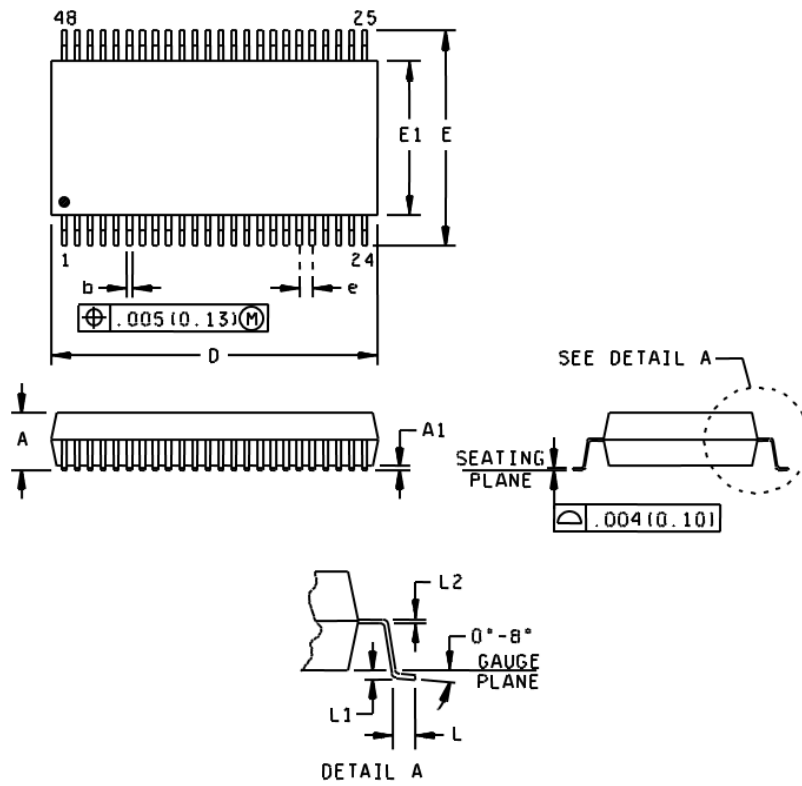
NOTES:

1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/04712
		REV E	PAGE 8

Case Y



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.110	---	2.79	E1	0.291	0.299	7.39	7.59
A1	0.008	---	0.20	---	L	0.020	0.040	0.51	1.02
b	0.008	0.0135	0.203	0.343	L1	0.010 TYP		0.25 TYP	
D	0.620	0.630	15.75	16.00	L2	0.005	0.010	0.13	0.25
e	0.025 BSC		0.635 BSC		n	48 leads		48 leads	
E	0.395	0.420	10.03	10.67					

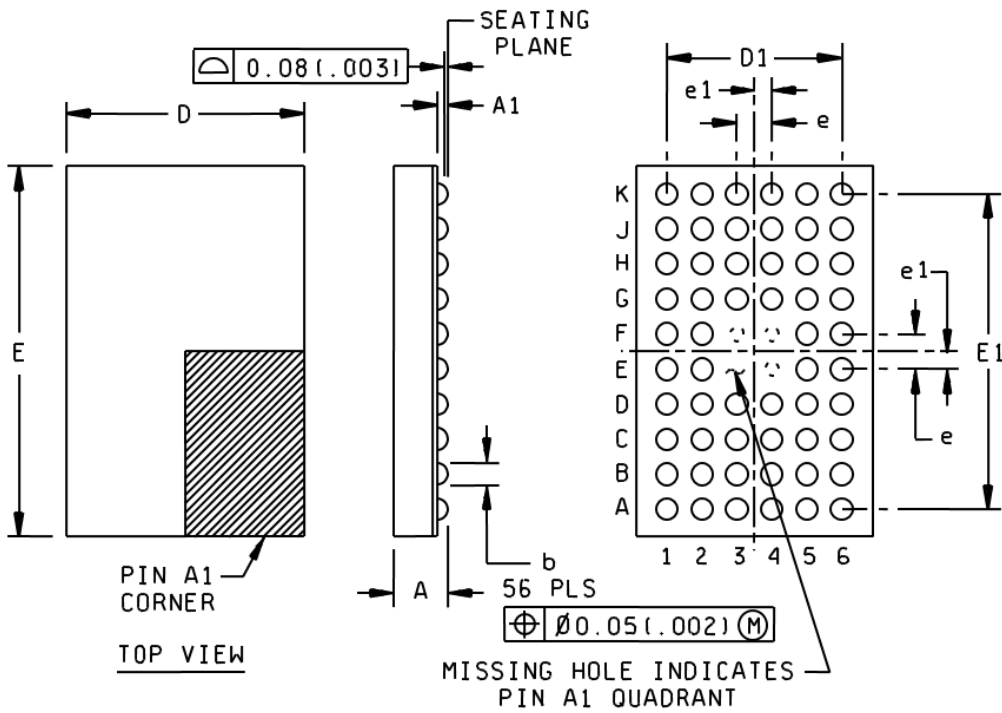
NOTES:

1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 in (0.15 millimeters).
4. Fall within JEDEC MO-118.

FIGURE 1. Case outlines – continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/04712
		REV E	PAGE 9

Case Z



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.039	---	1.00	E	0.272	0.280	6.90	7.10
A1	0.006	0.010	0.15	0.25	E1	0.230 BSC		5.85 BSC	
b	0.014	0.018	0.35	0.45	e	0.026 BSC		0.65 BSC	
D	0.173	0.181	4.40	4.60	e1	0.013 BSC		0.325 BSC	
D1	0.128 BSC		3.25 BSC		n	56 leads		56 leads	

NOTES:

1. All linear dimensions are in millimeters (inches).
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-225 variation BA.

FIGURE 1. Case outlines – continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		<b>REV E</b>	<b>PAGE 10</b>

(each 8-bit section)

Inputs			Output
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

H = High voltage level  
 L = Low voltage level  
 X = Immaterial  
 Z = High impedance state  
 Q<sub>0</sub> = Level of Q before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

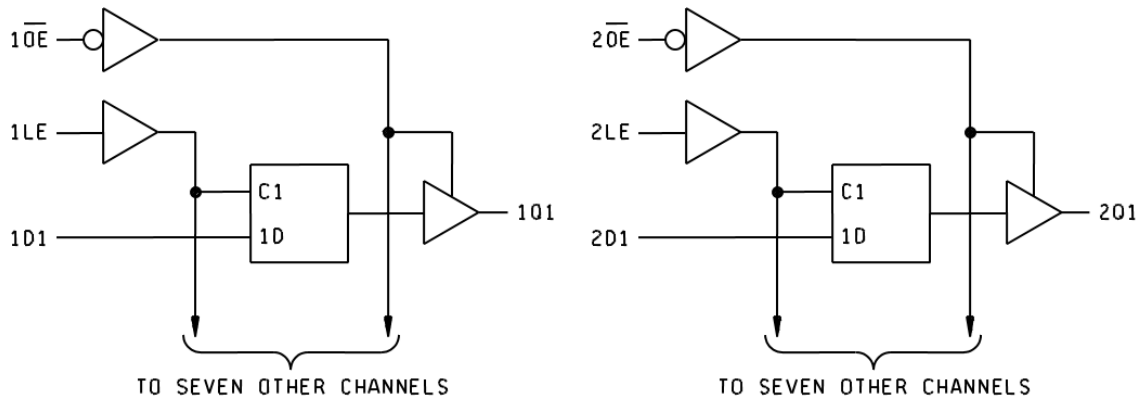


FIGURE 3. Logic diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/04712
		REV E	PAGE 11

Device type 01			
Case outlines X and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{1OE}$	25	2LE
2	1Q1	26	2D8
3	1Q2	27	2D7
4	GND	28	GND
5	1Q3	29	2D6
6	1Q4	30	2D5
7	V <sub>CC</sub>	31	V <sub>CC</sub>
8	1Q5	32	2D4
9	1Q6	33	2D3
10	GND	34	GND
11	1Q7	35	2D2
12	1Q8	36	2D1
13	2Q1	37	1D8
14	2Q2	38	1D7
15	GND	39	GND
16	2Q3	40	1D6
17	2Q4	41	1D5
18	V <sub>CC</sub>	42	V <sub>CC</sub>
19	2Q5	43	1D4
20	2Q6	44	1D3
21	GND	45	GND
22	2Q7	46	1D2
23	2Q8	47	1D1
24	$\overline{2OE}$	48	1LE

FIGURE 4. Terminal connections.

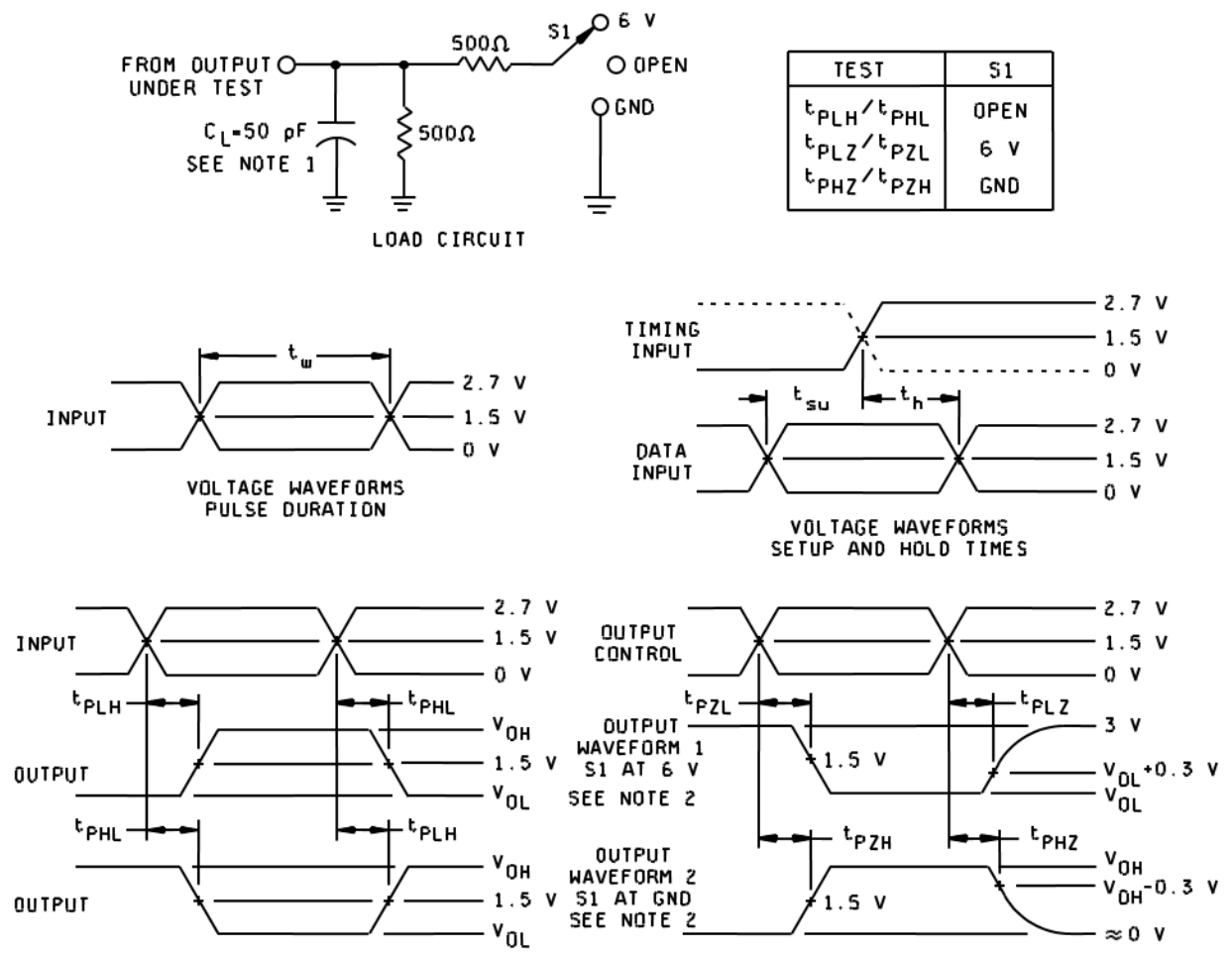
<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		REV E	PAGE 12

Device type 01			
Case outlines Z			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	1 $\overline{OE}$	F1	2Q1
A2	NC	F2	2Q2
A3	NC	F5	2D2
A4	NC	F6	2D1
A5	CN	G1	2Q3
A6	1LE	G2	2Q4
B1	1Q2	G3	GND
B2	1Q1	G4	GND
B3	GND	G5	2D4
B4	GND	G6	2D3
B5	1D1	H1	2Q5
B6	1D2	H2	2Q6
C1	1Q4	H3	V <sub>cc</sub>
C2	1Q3	H4	V <sub>cc</sub>
C3	V <sub>cc</sub>	H5	2D6
C4	V <sub>cc</sub>	H6	2D5
C5	1D3	J1	2Q7
C6	1D4	J2	2Q8
D1	1Q6	J3	GND
D2	1Q5	J4	GND
D3	GND	J5	2D8
D4	GND	J6	2D7
D5	1D5	K1	2 $\overline{OE}$
D6	1D6	K2	NC
E1	1Q8	K3	NC
E2	1Q7	K4	NC
E5	1D7	K5	NC
E6	1D8	K6	2LE

NC = No internal connection.

FIGURE 4. Terminal connections - continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		REV E	PAGE 13



NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_o = 50 \text{ } \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ , and  $t_f \leq 2.5 \text{ ns}$ .
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/04712
		REV E	PAGE 14

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04712-01XE	01295	CLVTH16373IDGGREP	LH16373EP
V62/04712-01YE	01295	CLVTH16373IDLREP	LH16373EP
V62/04712-01ZA	<u>2/</u>	CLVTH16373IGQLREP	LL373EP
V62/04712-02ZA	01295	CLVTH16373MGQLREP	H16373MEP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ Not available from an approved source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/04712</b>
		REV E	PAGE 15