REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add new device case outline Y. Update boilerplate to current revision. - CFS	04-11-22	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	11-06-14	David J. Corbett
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-07-19	Thomas M. Hess
D	Update boilerplate paragraphs to current VID description requirements. - DRH	23-01-18	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	D	D	D	D	D	D	D	D	D	D	D	D										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12										

PMIC N/A

Original date of drawing

04-04-23

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TITLE
MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04711
REV D		PAGE 1 OF 12

AMSC N/A

5962-V047-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT 16-bit edge-triggered D-type flip-flop with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04711	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVTH16374-EP	3.3-V ABT 16-bit edge-triggered D-type flip-flop with 3-state outputs

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MO-153	Plastic small-outline
Y	48	MO-118	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 4.6 V
Input voltage range (V_I) ..... -0.5 V to 7 V 2/
Voltage range applied to any output
in the high-impedance or power-off state (V_O) ..... -0.5 V to 7 V 2/
Voltage range applied to any output
in the high state (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/
Current into any output in the low state (I_O) ..... 128 mA
Current into any output in the high state (I_O) ..... 64 mA 3/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Package thermal impedance (θ_{JA}) ..... 70°C/W 4/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}) ..... 2.7 V to 3.6 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Maximum input voltage (V_I) ..... 5.5 V
Maximum high level output current (I_{OH}) ..... -32 mA
Maximum low level output current (I_{OL}) ..... 64 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) (Outputs enabled) ..... 10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$) ..... 200 µs/V
Operating free-air temperature range (T_A) ..... -40°C to +85°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V_{IK}	I_I = -18 mA	2.7 V	25°C,	All		-1.2	V
High level output voltage	V_{OH}	I_{OH} = -100 µA	2.7 V to 3.6 V	-40°C to 85°C		V_{CC} – 0.2		V
		I_{OH} = -8 mA	2.7 V			2.4		
		I_{OH} = -32 mA	3 V			2		
Low level output voltage	V_{OL}	I_{OL} = 100 µA	2.7 V				0.2	V
		I_{OL} = 24 mA					0.5	
		I_{OL} = 16 mA	3 V				0.4	
		I_{OL} = 32 mA					0.5	
		I_{OL} = 64 mA					0.55	
Input current	I_I	V_I = 5.5 V	0 V or 3.6 V				10	µA
		Control inputs. $V_I = V_{CC}$ or GND	3.6 V				±1	
		Data inputs. $V_I = V_{CC}$					1	
		Data inputs. V_I = 0 V					-5	
Input/output power-off leakage current	I_{off}	V_I or V_O = 0 to 4.5 V	0 V				±100	µA
Input current (hold)	$I_{I(hold)}$	Data inputs, V_I = 0.8 V	3 V			75		µA
		Data inputs, V_I = 2 V				-75		
		Data inputs. V_I = 0 V to 3.6 V	3.6 V 2/				±500	
3-state output leakage current high	I_{OZH}	V_O = 3 V	3.6 V				5	µA
3-state output leakage current low	I_{OZL}	V_O = 0.5 V	3.6 V				-5	µA
3-state output current power-up	I_{OZPU}	V_O = 0.5 V to 3 V $\overline{OE}$ = don't care	0 V to 1.5 V				±100	µA
3-state output current power-down	I_{OZPD}	V_O = 0.5 V to 3 V $\overline{OE}$ = don't care	1.5 V to 0 V				±100	µA
Quiescent supply current	I_{CC}	Outputs high. $V_I = V_{CC}$ or GND, I_O = 0 A	3.6 V				0.19	mA
		Outputs low. $V_I = V_{CC}$ or GND, I_O = 0 A					5	
		Outputs disabled. $V_I = V_{CC}$ or GND, I_O = 0 A					0.19	
Quiescent supply current delta	ΔI_{CC} 3/	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V				0.2	mA
Input capacitance	C_i	V_I = 3 V or 0 V	3.3 V			3 TYP		pF
Output capacitance	C_o	V_O = 3 V or 0 V				9 TYP		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

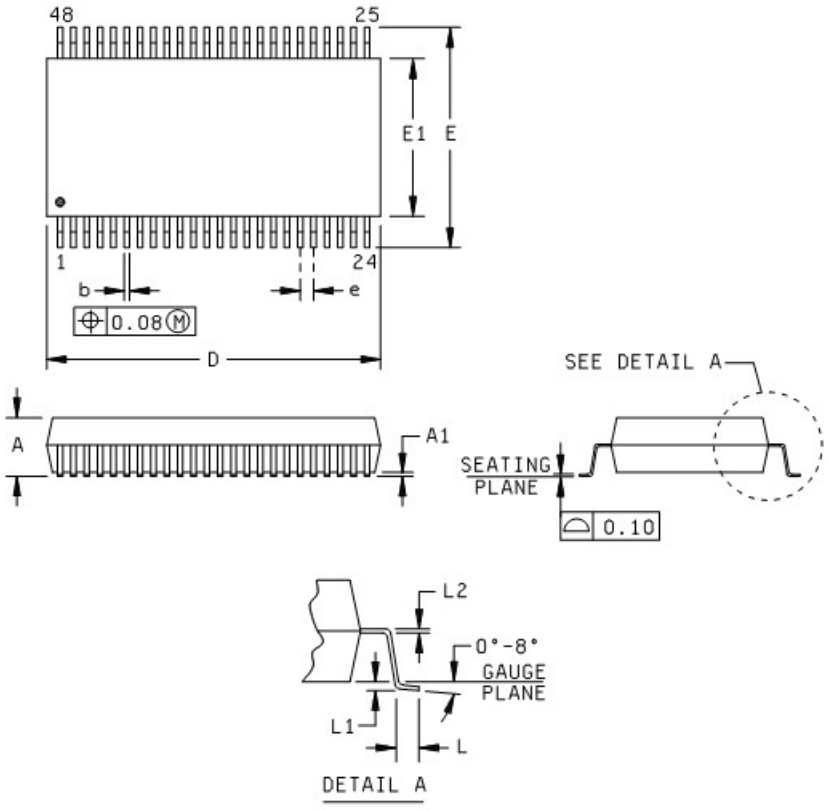
Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Clock frequency	f_{clock}		2.7 V	25°C,	All		160	MHz
			3.3 V ±0.3 V	-40°C to 85°C			160	
Pulse duration, CLK high or low	t_w	See figure 5.	2.7 V			3		ns
			3.3 V ±0.3 V			3		
Setup time, data before CLK↑	t_{su}	High or low	2.7 V			2		ns
		See figure 5.	3.3 V ±0.3 V			1.8		
Hold time, data after CLK↑	t_h	High or low	2.7 V			0.1		ns
		See figure 5.	3.3 V ±0.3 V			0.8		
Maximum frequency	f_{max}	C_L = 50 pF	2.7 V			160		MHz
			3.3 V ±0.3 V			160		
Propagation delay time, CLK to Q	t_{PLH}	C_L = 50 pF	2.7 V				5.2	ns
		See figure 5.	3.3 V ±0.3 V			1.9	4.5	
	t_{PHL}		2.7 V				4.2	
			3.3 V ±0.3 V			2.1	4	
Propagation delay time, output enable, $\overline{OE}$ to Q	t_{PZH}		2.7 V				5.4	
			3.3 V ±0.3 V			1.5	4.5	
	t_{PZL}		2.7 V				5	
			3.3 V ±0.3 V			1.5	4.4	
Propagation delay time, output disable, $\overline{OE}$ to Q	t_{PHZ}		2.7 V				5.4	
			3.3 V ±0.3 V			2.4	5	
	t_{PLZ}		2.7 V				4.8	
			3.3 V ±0.3 V			2	4.6	
Output skew	$t_{sk(0)}$	C_L = 50 pF	3.3 V ±0.3 V				0.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

3/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X

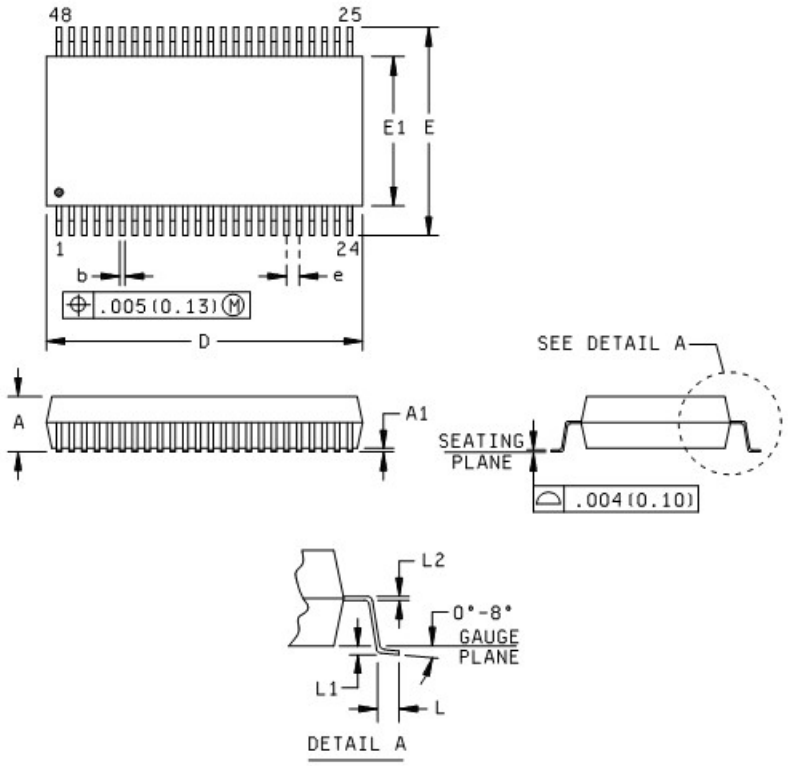


Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E1	6.00	6.20	0.236	0.244
A1	0.05	0.15	0.002	0.006	e	0.50 BSC		0.020 BSC	
b	0.17	0.27	0.007	0.011	L	0.50	0.75	0.020	0.030
D	12.40	12.60	0.488	0.496	L1	0.25 TYP		0.010 TYP	
E	7.90	8.30	0.311	0.327	L2	0.15 NOM		0.006 NOM	

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline.

Case Y



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	.110	---	2.79	E1	.291	.299	7.39	7.59
A1	.008	---	0.20	---	e	.025 BSC		0.635 BSC	
b	.008	.0135	0.203	0.343	L	.020	.040	0.51	1.02
D	.620	.630	15.75	16.00	L1	.010 TYP		0.25 TYP	
E	.395	.420	10.03	10.67	L2	.005	.010	0.13	0.25

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 inches (0.15 millimeters).
4. Falls within JEDEC MO-118.

FIGURE 1. Case outlines - Continued.

(each flip-flop)

Inputs			Output
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

H = High voltage level X = Immaterial
L = Low voltage level Z = High impedance state
Q_0 = Level of Q before the indicated steady-state input conditions were established.
↑ = Low to high transition

FIGURE 2. Truth table.

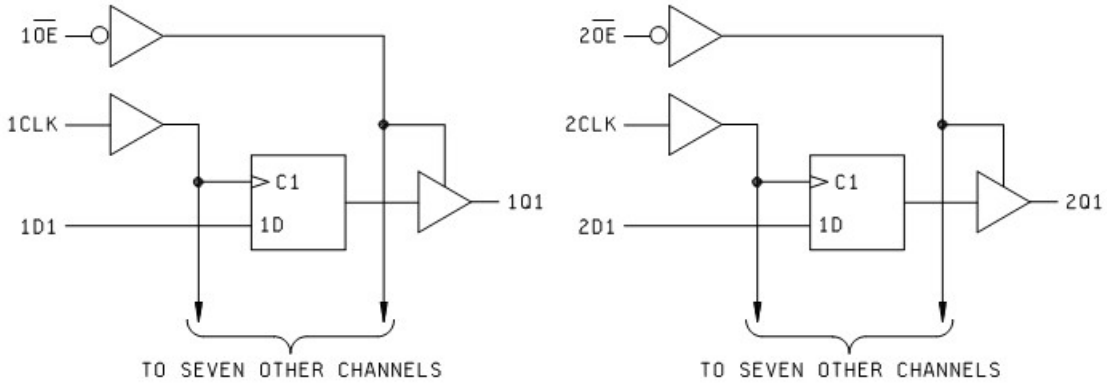
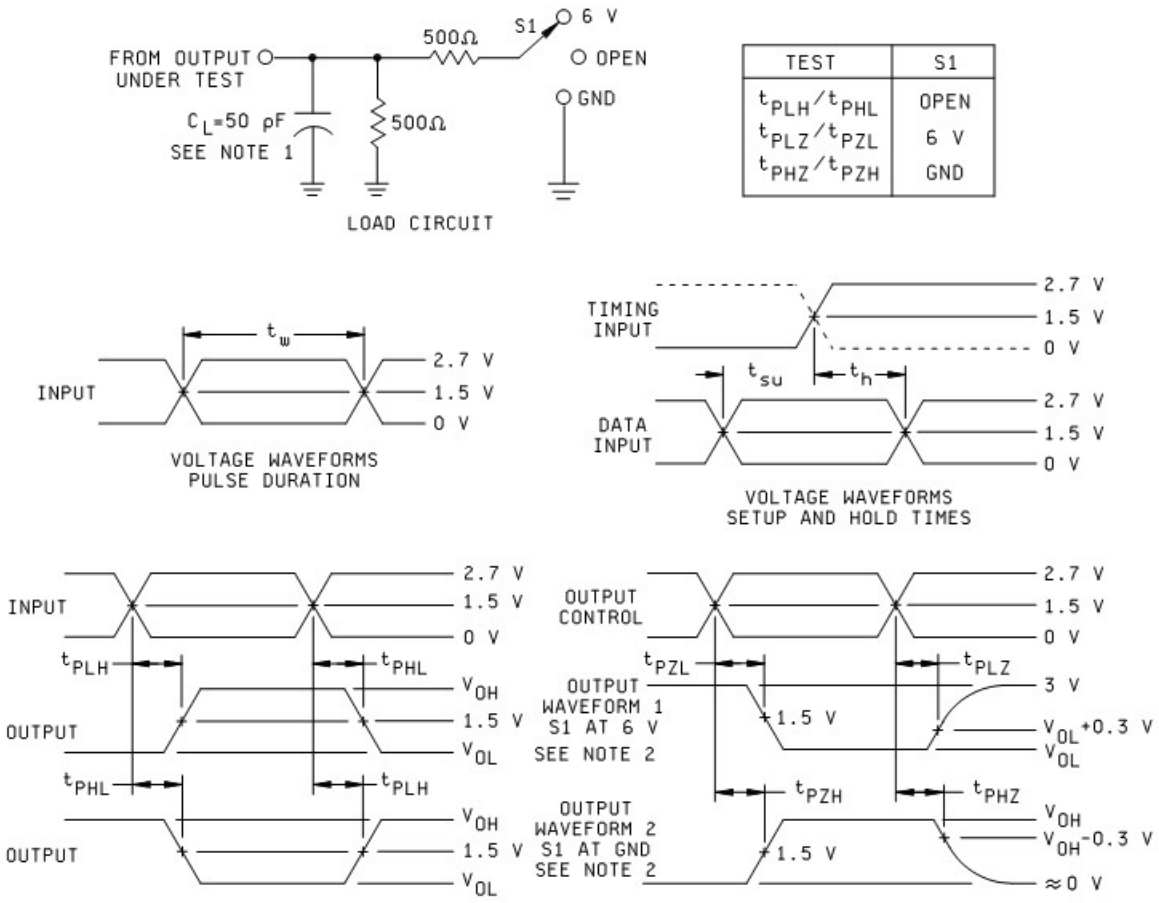


FIGURE 3. Logic diagram.

Device type 01			
Case outline X and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$1\overline{OE}$	25	2CLK
2	1Q1	26	2D8
3	1Q2	27	2D7
4	GND	28	GND
5	1Q3	29	2D6
6	1Q4	30	2D5
7	V_{CC}	31	V_{CC}
8	1Q5	32	2D4
9	1Q6	33	2D3
10	GND	34	GND
11	1Q7	35	2D2
12	1Q8	36	2D1
13	2Q1	37	1D8
14	2Q2	38	1D7
15	GND	39	GND
16	2Q3	40	1D6
17	2Q4	41	1D5
18	V_{CC}	42	V_{CC}
19	2Q5	43	1D4
20	2Q6	44	1D3
21	GND	45	GND
22	2Q7	46	1D2
23	2Q8	47	1D1
24	$2\overline{OE}$	48	1CLK

FIGURE 4. Terminal connections.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, and t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04711-01XE	2/	CLVTH16374IDGGREP	LH16374EP
V62/04711-01YE	01295	CLVTH16374IDLREP	LH16374EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not available from an approved source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243