

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-04-18	David J. Corbett
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-06-20	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - DRH	22-11-15	Muhammad A. Akbar

**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

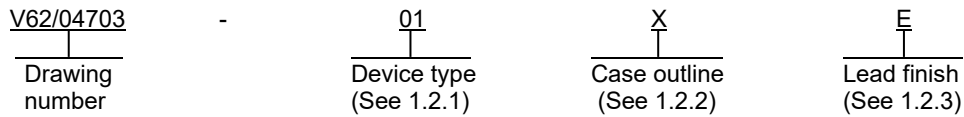
REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14						

PMIC N/A Original date of drawing 04-04-12	PREPARED BY Charles F. Saffle		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime	
	CHECKED BY Charles F. Saffle		TITLE MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess			
	SIZE A	CAGE CODE 16236	DWG NO. V62/04703	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance decade counter/divider with 10 decoded outputs microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	CD74HC4017-EP	Decade counter/divider with 10 decoded outputs

1.2.2 Case outlines. The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MS-012	Plastic small-outline
Y	16	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +7 V 2/
Input clamp current (I_{IK}) ($V_I < -0.5$ or $V_I > V_{CC} + 0.5$)	± 20 mA
Output clamp current (I_{OK}) ($V_O < -0.5$ or $V_O > V_{CC} + 0.5$)	± 20 mA
Source or sink current per output pin (I_O) ($V_O > -0.5$ or $V_O < V_{CC} + 0.5$)	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance (θ_{JA}):	
Case outline X	73°C/W 3/
Case outline Y	108°C/W 3/
Maximum junction temperature (T_J)	150°C
Lead temperature (during soldering):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	300°C
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC})	2 V to 6 V
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 2$ V	1.5 V
$V_{CC} = 4.5$ V	3.15 V
$V_{CC} = 6$ V	4.2 V
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 2$ V	0.5 V
$V_{CC} = 4.5$ V	1.35 V
$V_{CC} = 6$ V	1.8 V
Input voltage range (V_I)	0 V to V_{CC}
Output voltage range (V_O)	0 V to V_{CC}
Input transition (rise and fall) time (t_i):	
$V_{CC} = 2$ V	0 to 1000 ns
$V_{CC} = 4.5$ V	0 to 500 ns
$V_{CC} = 6$ V	0 to 400 ns
Operating free-air temperature range (T_A)	-40°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ All voltages are referenced to GND unless otherwise specified.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEESD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	CMOS loads V _I = V _{IH} or V _{IL} I _O = -0.02 mA	2 V	25°C, -40°C to 125°C	All	1.9		V
			4.5 V			4.4		
			6 V			5.9		
		TTL loads V _I = V _{IH} or V _{IL} I _O = -4 mA	4.5 V	25°C, -40°C to 125°C		3.98		
			6 V	25°C, -40°C to 125°C		5.48		
							5.2	
Low level output voltage	V _{OL}	CMOS loads V _I = V _{IH} or V _{IL} I _O = -0.02 mA	2 V	25°C, -40°C to 125°C		0.1	V	
			4.5 V			0.1		
			6 V			0.1		
		TTL loads V _I = V _{IH} or V _{IL} I _O = -4 mA	4.5 V	25°C, -40°C to 125°C		0.26		
			6 V	25°C, -40°C to 125°C		0.4		
								0.26
Input current	I _I	V _I = V _{CC} or GND	6 V	25°C, -40°C to 125°C		±0.1	µA	
						±1		
Quiescent supply current	I _{CC}	V _I = V _{CC} or GND I _O = 0 mA	6 V	25°C, -40°C to 125°C		8	µA	
						160		
Input capacitance	C _{IN}	C _L = 50 pF		25°C, -40°C to 125°C		10	pF	
						10		
Power dissipation capacitance	C _{pd} 2/	C _L = 15 pF Input t _r , t _f = 6 ns	5 V	25°C		39 TYP	pF	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Maximum clock frequency	f _{max}	See figure 5.	2 V	25°C,	All	6		MHz
				-40°C to 125°C		4		
			4.5 V	25°C,		30		
				-40°C to 125°C		20		
			6 V	25°C,		35		
				-40°C to 125°C		23		
Pulse duration	t _w	CP See figure 5.	2 V	25°C,	All	80		ns
				-40°C to 125°C		120		
			4.5 V	25°C,		16		
				-40°C to 125°C		24		
			6 V	25°C,		14		
				-40°C to 125°C		20		
		MR See figure 5.	2 V	25°C,		80		
				-40°C to 125°C		120		
			4.5 V	25°C,		16		
				-40°C to 125°C		24		
			6 V	25°C,		14		
				-40°C to 125°C		20		
Setup time	t _{su}	CE to CP See figure 5.	2 V	25°C,	All	75		
				-40°C to 125°C		110		
			4.5 V	25°C,		15		
				-40°C to 125°C		22		
			6 V	25°C,		13		
				-40°C to 125°C		19		
		MR inactive See figure 5.	2 V	25°C,		5		
				-40°C to 125°C		5		
			4.5 V	25°C,		5		
				-40°C to 125°C		5		
			6 V	25°C,		5		
				-40°C to 125°C		5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit	
						Min	Max		
Hold time	t _h	\overline{CE} to CP See figure 5.	2 V	25°C	All	0		ns	
				-40°C to 125°C		0			
			4.5 V	25°C		0			
				-40°C to 125°C		0			
			6 V	25°C		0			
				-40°C to 125°C		0			
Propagation delay time, CP to Decade out	t _{pd}	C _L = 50 pF See figure 5.	2 V	25°C			230		
				-40°C to 125°C			345		
			4.5 V	25°C			46		
				-40°C to 125°C			69		
			6 V	25°C			39		
				-40°C to 125°C			59		
		C _L = 50 pF See figure 5.	5 V	25°C			19 TYP		
		Propagation delay time, CP to TC	t _{pd}	C _L = 50 pF See figure 5.	2 V	25°C			230
						-40°C to 125°C			345
					4.5 V	25°C			46
-40°C to 125°C							69		
6 V	25°C						39		
	-40°C to 125°C						59		
C _L = 50 pF See figure 5.	5 V			25°C			19 TYP		
Propagation delay time, \overline{CE} to Decade out	t _{pd}			C _L = 50 pF See figure 5.	2 V	25°C			250
						-40°C to 125°C			375
					4.5 V	25°C			50
		-40°C to 125°C					75		
		6 V	25°C				43		
			-40°C to 125°C				64		
		C _L = 50 pF See figure 5.	5 V	25°C			21 TYP		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit	
						Min	Max		
Propagation delay time, \overline{CE} to TC	t _{pd}	C _L = 50 pF See figure 5.	2 V	25°C	All		250	ns	
				-40°C to 125°C			375		
			4.5 V	25°C		50			
				-40°C to 125°C		75			
			6 V	25°C		43			
				-40°C to 125°C		64			
		C _L = 15 pF, See figure 5.	5 V	25°C		21 TYP			
		Propagation delay time, MR to Decade out		C _L = 50 pF See figure 5.	2 V	25°C			230
						-40°C to 125°C			345
					4.5 V	25°C			46
-40°C to 125°C						69			
6 V	25°C					39			
	-40°C to 125°C					59			
C _L = 15 pF, See figure 5.	5 V			25°C		19 TYP			
Propagation delay time, MR to TC				C _L = 50 pF See figure 5.	2 V	25°C		230	
						-40°C to 125°C		345	
					4.5 V	25°C		46	
		-40°C to 125°C				69			
		6 V	25°C			39			
			-40°C to 125°C			59			
		C _L = 15 pF, See figure 5.	5 V	25°C		19 TYP			
		Transition rise and fall time	t _t	C _L = 50 pF See figure 5.	2 V	25°C		75	
						-40°C to 125°C		110	
					4.5 V	25°C		15	
-40°C to 125°C						22			
6 V	25°C					13			
	-40°C to 125°C					19			
C _L = 15 pF, See figure 5.	5 V			25°C		60 TYP			
Maximum frequency, CP	f _{mas}			C _L = 15 pF, See figure 5.	5 V	25°C		60 TYP	MHZ

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ C_{PD} is used to determine the dynamic power consumption per package.

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + \sum(C_L \times V_{CC}^2 \times f_o)$$

f_i = input frequency

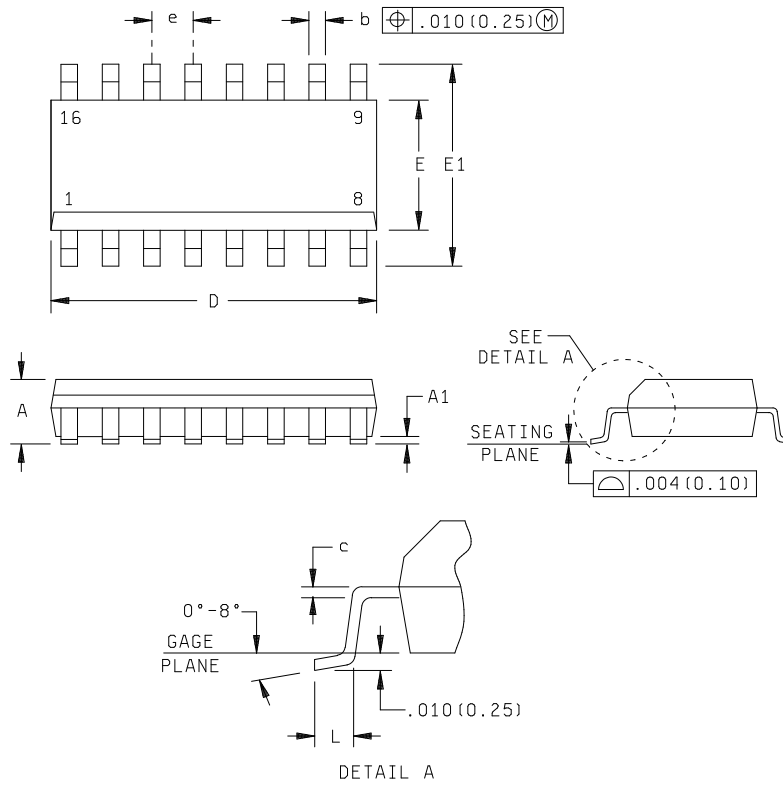
f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	.069	---	1.75	E	.150	.157	3.81	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.014	.020	0.35	0.51	e	.050 TYP		1.27 TYP	
c	.008 NOM		0.20 NOM		L	.016	.044	0.40	1.12
D	.386	.394	9.80	10.00					

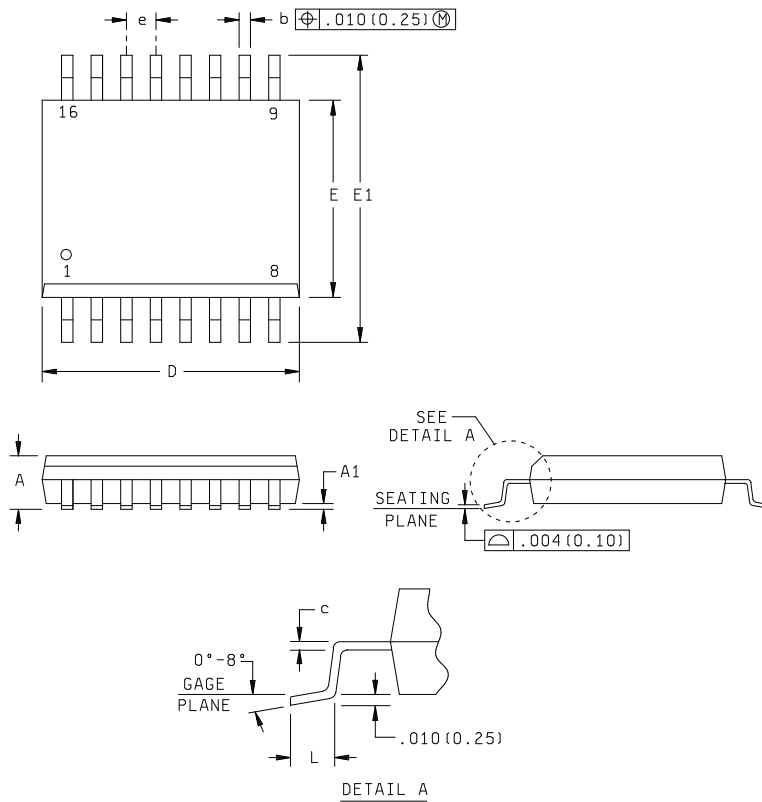
NOTES:

1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed .006 inches (0.15 millimeters).
4. Falls within JEDEC MS-012.

FIGURE 1. Case outlines.

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Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	.047	E	4.30	4.50	.169	.177
A1	0.05	0.15	.002	.006	E1	6.20	6.60	.244	.260
b	0.19	0.30	.007	.012	e	0.65 TYP		.026 TYP	
c	0.15 NOM		.006 NOM		L	0.50	0.75	.020	.030
D	4.90	5.10	.193	.201					

NOTES:

1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (.006 inches).
4. Falls within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

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Inputs			Output State <u>1/</u>
CP	CE	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H, 1-9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

1/ If $n < 5$, TC = H, otherwise TC = L.

H = High voltage level ↑ = Transition from low to high level.
L = Low voltage level ↓ = Transition from high to low level.
X = Immaterial

FIGURE 2. Truth table.

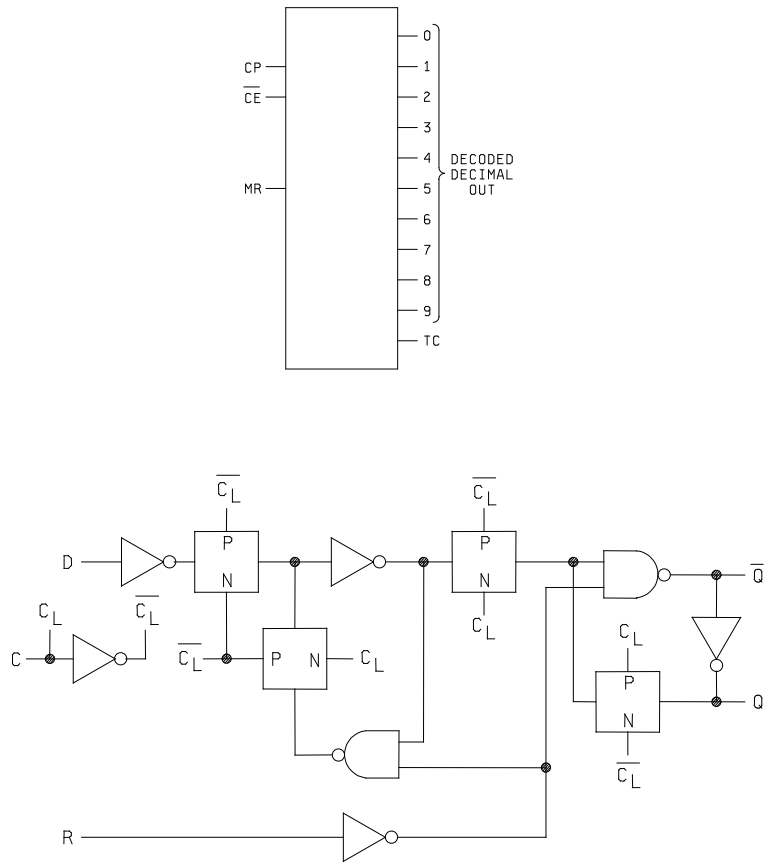


FIGURE 3. Logic diagram.

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Device type 01			
Case outlines X and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	5	9	
2	1	10	4
3	0	11	9
4	2	12	TC
5	6	13	\overline{CE}
6	7	14	CP
7	3	15	MR
8	GND	16	V _{cc}

FIGURE 4. Terminal connections.

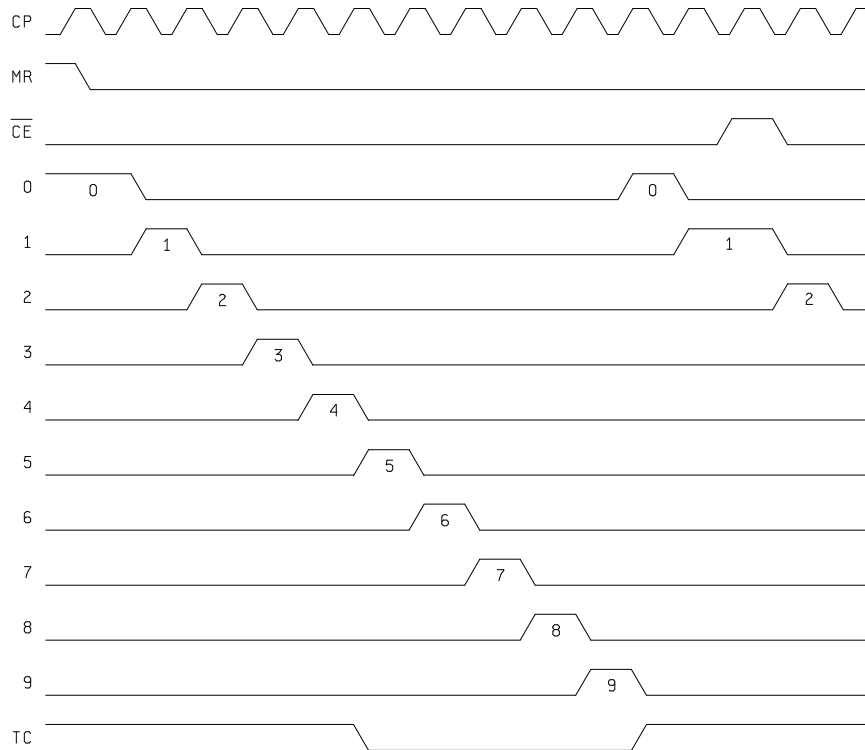
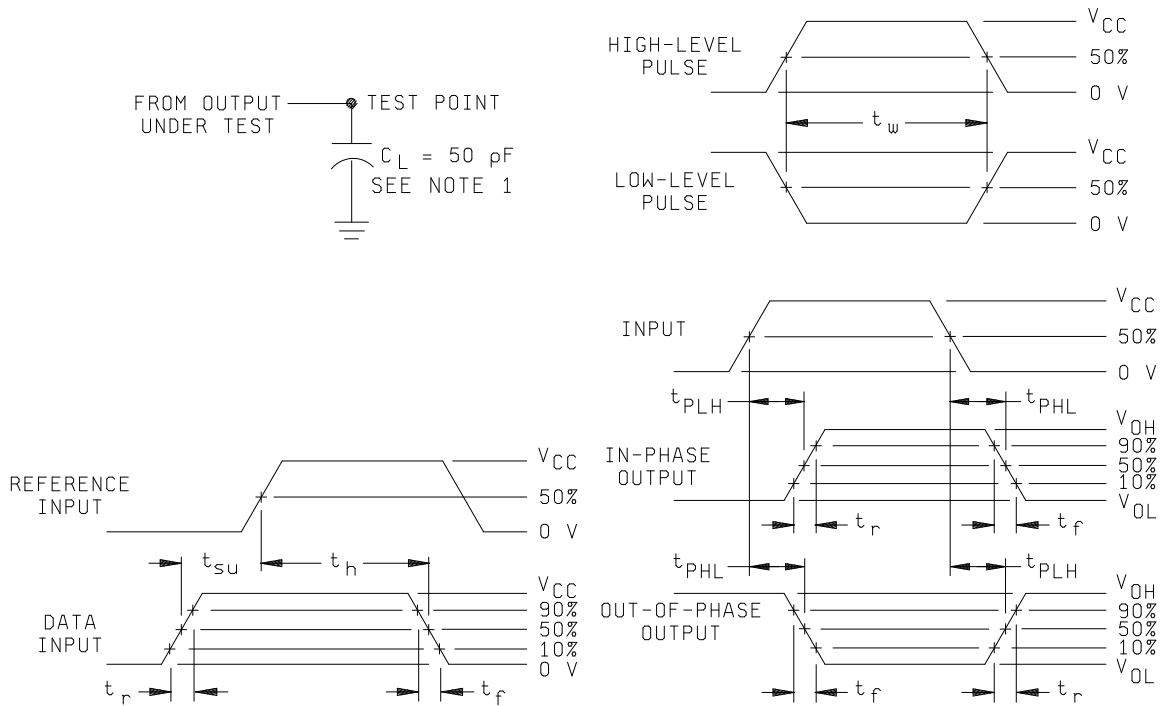


FIGURE 5. Timing waveforms and test circuit.

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NOTES:

1. C_L includes probe and jig capacitance.
2. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_o = 50\Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
3. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLH} and t_{PHL} are the same as t_{pd} .

FIGURE 5. Timing waveforms and test circuit - Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04703-01XE	01295	CD74HC4017QM96EP	HC4017E
V62/04703-01YE	01295	CD74HC4017QPWREP	HC4017E

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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