REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	11-02-01	David J. Corbett
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-06-20	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - DRH	22-11-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																							
SHEET																							
REV	C	C	C	C	C	C	C	C	C	C	C	C	C										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13										

PMIC N/A

Original date of drawing

04-04-12

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DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, 8-STAGE SYNCHRONOUS DOWN COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04702
REV C		PAGE 1 OF 13

AMSC N/A

5962-V017-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8-stage synchronous down counter microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04702	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	CD74HC40103-EP	8-stage synchronous down counter

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-012	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to +7 V 2/
Input clamp current (I_{IK}) ($V_I < -0.5$ or $V_I > V_{CC} +0.5$) ..... ±20 mA
Output clamp current (I_{OK}) ($V_O < -0.5$ or $V_O > V_{CC} +0.5$) ..... ±20 mA
Source or sink current per output pin (I_O) ($V_O > -0.5$ or $V_O < V_{CC} +0.5$) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance (θ_{JA}) ..... 73°C/W 3/
Maximum junction temperature (T_J) ..... 150°C
Lead temperature (during soldering):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . ..... 300°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltages are referenced to GND unless otherwise specified.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC}) ..... 2 V to 6 V
Minimum high level input voltage (V_{IH}):
V_{CC} = 2 V ..... 1.5 V
V_{CC} = 4.5 V ..... 3.15 V
V_{CC} = 6 V ..... 4.2 V
Maximum low level input voltage (V_{IL}):
V_{CC} = 2 V ..... 0.5 V
V_{CC} = 4.5 V ..... 1.35 V
V_{CC} = 6 V ..... 1.8 V
Input voltage range (V_I) ..... 0 V to V_{CC}
Output voltage range (V_O) ..... 0 V to V_{CC}
Input transition (rise and fall) time (t_t):
V_{CC} = 2 V ..... 0 to 1000 ns
V_{CC} = 4.5 V ..... 0 to 500 ns
V_{CC} = 6 V ..... 0 to 400 ns
Operating free-air temperature range (T_A) ..... -40°C to +125°C

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JESD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	CMOS loads	2 V	25°C,	All	1.9		V
		$V_I = V_{IH}$ or V_{IL}	4.5 V	-40°C to 125°C		4.4		
		I_O = -0.02 mA	6 V			5.9		
		TTL loads	4.5 V	25°C		3.98		
		$V_I = V_{IH}$ or V_{IL}, I_O = -4 mA		-40°C to 125°C		3.7		
		TTL loads	6 V	25°C		5.48		
		$V_I = V_{IH}$ or V_{IL}, I_O = -5.2 mA		-40°C to 125°C		5.2		
Low level output voltage	V_{OL}	CMOS loads	2 V	25°C,			0.1	V
		$V_I = V_{IH}$ or V_{IL}	4.5 V	-40°C to 125°C			0.1	
		I_O = -0.02 mA	6 V				0.1	
		TTL loads	4.5 V	25°C			0.26	
		$V_I = V_{IH}$ or V_{IL}, I_O = -4 mA		-40°C to 125°C			0.4	
		TTL loads	6 V	25°C			0.26	
		$V_I = V_{IH}$ or V_{IL}, I_O = -5.2 mA		-40°C to 125°C			0.4	
Input current	I_I	$V_I = V_{CC}$ or GND	6 V	25°C			±0.1	µA
				-40°C to 125°C			±1	
Quiescent supply current	I_{CC}	$V_I = V_{CC}$ or GND	6 V	25°C			8	µA
		I_O = 0 mA		-40°C to 125°C			160	
Input capacitance	C_{IN}	C_L = 50 pF		25°C			10	pF
				-40°C to 125°C			10	
Power dissipation capacitance	C_{pd} 2/	Input t_r, t_f = 6 ns	5 V	25°C		25 TYP		pF
Pulse duration	t_w	CP	2 V	25°C		165		ns
		See figure 5.		-40°C to 125°C		250		
			4.5 V	25°C		33		
				-40°C to 125°C		50		
			6 V	25°C		28		
				-40°C to 125°C		43		
		$\overline{PL}$	2 V	25°C		125		
		See figure 5.		-40°C to 125°C		190		
			4.5 V	25°C		25		
				-40°C to 125°C		38		
			6 V	25°C		21		
				-40°C to 125°C		32		
		$\overline{MR}$	2 V	25°C		125		
		See figure 5.		-40°C to 125°C		190		
			4.5 V	25°C		25		
				-40°C to 125°C		38		
			6 V	25°C		21		
				-40°C to 125°C		32		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Maximum frequency	f_{mas} 3/	CP frequency See figure 5.	2 V	25°C	All	3		MHz
				-40°C to 125°C		2		
			4.5 V	25°C		15		
				-40°C to 125°C		10		
			6 V	25°C		18		
				-40°C to 125°C		12		
Setup time	t_{su}	P to CP See figure 5.	2 V	25°C		100		ns
				-40°C to 125°C		150		
			4.5 V	25°C		20		
				-40°C to 125°C		30		
			6 V	25°C		17		
				-40°C to 125°C		26		
		$\overline{PE}$ to CP See figure 5.	2 V	25°C		75		
				-40°C to 125°C		110		
			4.5 V	25°C		15		
				-40°C to 125°C		22		
			6 V	25°C		13		
				-40°C to 125°C		19		
		$\overline{TE}$ to CP See figure 5.	2 V	25°C		150		
				-40°C to 125°C		225		
			4.5 V	25°C		30		
				-40°C to 125°C		45		
			6 V	25°C		26		
				-40°C to 125°C		38		
		To CP, $\overline{MR}$ inactive See figure 5.	2 V	25°C		50		
				-40°C to 125°C		75		
			4.5 V	25°C		10		
				-40°C to 125°C		15		
			6 V	25°C		9		
				-40°C to 125°C		13		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Hold time	t_h	P to CP See figure 5.	2 V	25°C	All	5		ns
				-40°C to 125°C		5		
			4.5 V	25°C		5		
				-40°C to 125°C		5		
			6 V	25°C		5		
				-40°C to 125°C		5		
		$\overline{TE}$ to CP See figure 5.	2 V	25°C		0		
				-40°C to 125°C		0		
			4.5 V	25°C		0		
				-40°C to 125°C		0		
			6 V	25°C		0		
				-40°C to 125°C		0		
		$\overline{PE}$ to CP See figure 5.	2 V	25°C		2		
				-40°C to 125°C		2		
			4.5 V	25°C		2		
				-40°C to 125°C		2		
			6 V	25°C		2		
				-40°C to 125°C		2		
Propagation delay time, CP to $\overline{TC}$ (asynchronous preset)	t_{pd}	C_L = 50 pF See figure 5.	2 V	25°C			300	
				-40°C to 125°C			450	
			4.5 V	25°C			60	
				-40°C to 125°C			90	
			6 V	25°C			51	
				-40°C to 125°C			77	
		C_L = 15 pF, See figure 5.	5 V	25°C		25 TYP		
Propagation delay time, CP to $\overline{TC}$ (synchronous preset)		C_L = 50 pF See figure 5.	2 V	25°C			300	
				-40°C to 125°C			450	
			4.5 V	25°C			60	
				-40°C to 125°C			90	
			6 V	25°C			51	
				-40°C to 125°C			77	
		C_L = 15 pF, See figure 5.	5 V	25°C		25 TYP		
Propagation delay time, $\overline{TE}$ to $\overline{TC}$		C_L = 50 pF See figure 5.	2 V	25°C			200	
				-40°C to 125°C			300	
			4.5 V	25°C			40	
				-40°C to 125°C			60	
			6 V	25°C			34	
				-40°C to 125°C			51	
		C_L = 15 pF, See figure 5.	5 V	25°C		17 TYP		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Propagation delay time, $\overline{PL}$ to $\overline{TC}$	t_{pd}	C_L = 50 pF See figure 5.	2 V	25°C	All		275	ns
				-40°C to 125°C			415	
			4.5 V	25°C			55	
				-40°C to 125°C			83	
			6 V	25°C			47	
				-40°C to 125°C			71	
		C_L = 15 pF, See figure 5.	5 V	25°C		23 TYP		
Propagation delay time, $\overline{MR}$ to $\overline{TC}$		C_L = 50 pF See figure 5.	2 V	25°C			275	
				-40°C to 125°C			415	
			4.5 V	25°C			55	
				-40°C to 125°C			83	
			6 V	25°C			47	
				-40°C to 125°C			71	
		C_L = 15 pF, See figure 5.	5 V	25°C		23 TYP		
Transition rise and fall time	t_t	C_L = 50 pF	2 V	25°C			75	ns
				-40°C to 125°C			110	
			4.5 V	25°C			15	
				-40°C to 125°C			22	
			6 V	25°C			13	
				-40°C to 125°C			19	
Maximum frequency, CP	f_{mas}	C_L = 15 pF, See figure 5.	5 V	25°C		25 TYP		MHz

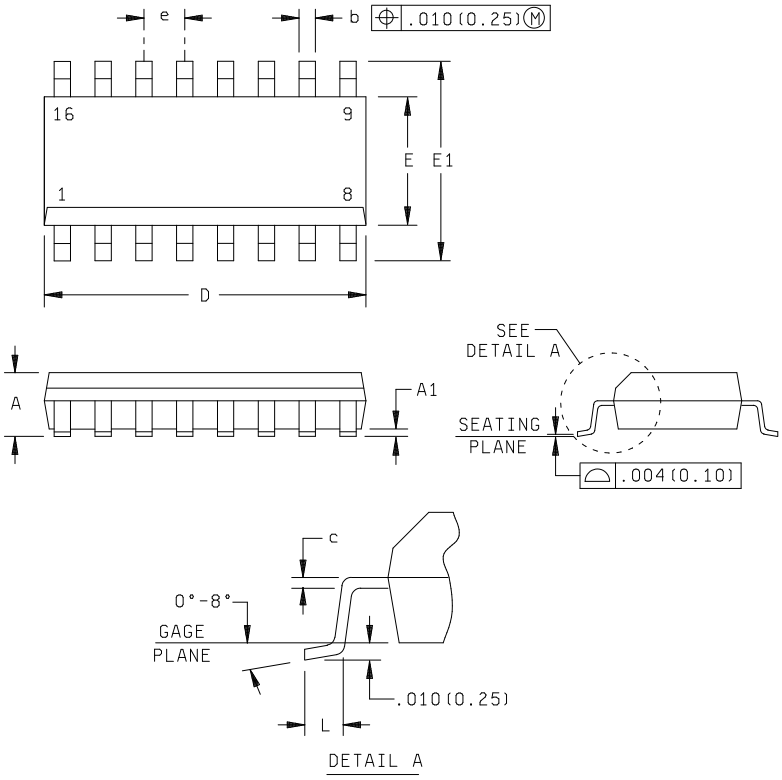
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ C_{PD} is used to determine the dynamic power consumption per package.
$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_o)$
f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

3/ Noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, count enables ($\overline{PE}$ or $\overline{TE}$) to clock setup times, and count enables ($\overline{PE}$ or $\overline{TE}$) to clock hold times determine maximum clock frequency. For example, with this device:

$$CP\ f_{max} = \frac{1}{\text{CP to TC prop delay + TE to CP setup time + TE to CP hold time}} = \frac{1}{60 + 30 + 0} \approx 11\ \text{MHz}$$

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	.069	---	1.75	E	.150	.157	3.81	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.014	.020	0.35	0.51	e	.050 TYP		1.27 TYP	
c	.008 NOM		0.20 NOM		L	.016	.044	0.40	1.12
D	.386	.394	9.80	10.00					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 inches (0.15 millimeters).
4. Falls within JEDEC MS-012.

FIGURE 1. Case outline.

Function Table 1/

Control Inputs				Preset Mode	Action
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	Synchronous	Inhibit counter
H	H	H	L		Count down
H	H	L	X		Preset on next positive clock transition
H	L	X	X	Asynchronous	Preset asynchronously
L	X	X	X		Clear to maximum count

1/ See figure 5 for timing diagram.

Clock connected to clock output.
Synchronous operation: Changes occur on negative-to-positive clock transitions.
Load inputs: MSB = P7, LSB = P0

H = High voltage level
L = Low voltage level
X = Immaterial

FIGURE 2. Function table.

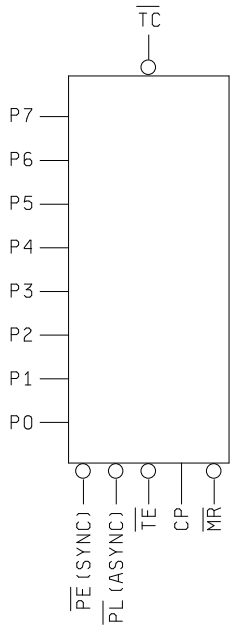


FIGURE 3. Logic diagram.

Case outlines: X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CP	9	$\overline{PL}$ (ASYNC)
2	$\overline{MR}$	10	P4
3	$\overline{TE}$	11	P5
4	P0	12	P6
5	P1	13	P7
6	P2	14	$\overline{TC}$
7	P3	15	$\overline{PE}$ (SYNC)
8	GND	16	V_{CC}

FIGURE 4. Terminal connections.

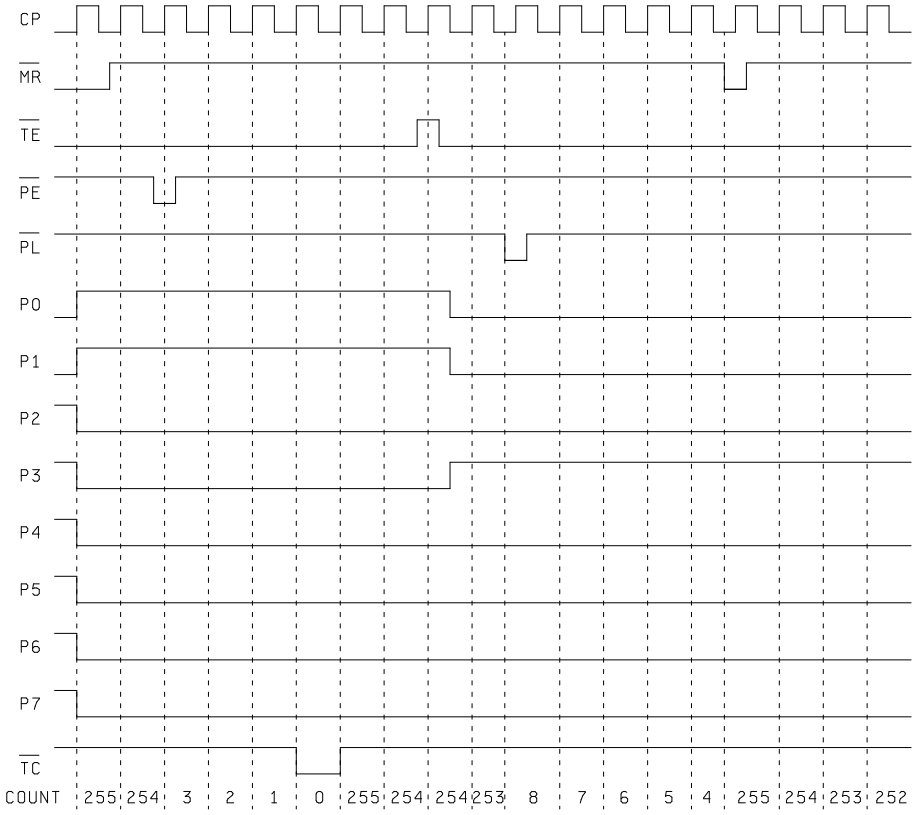
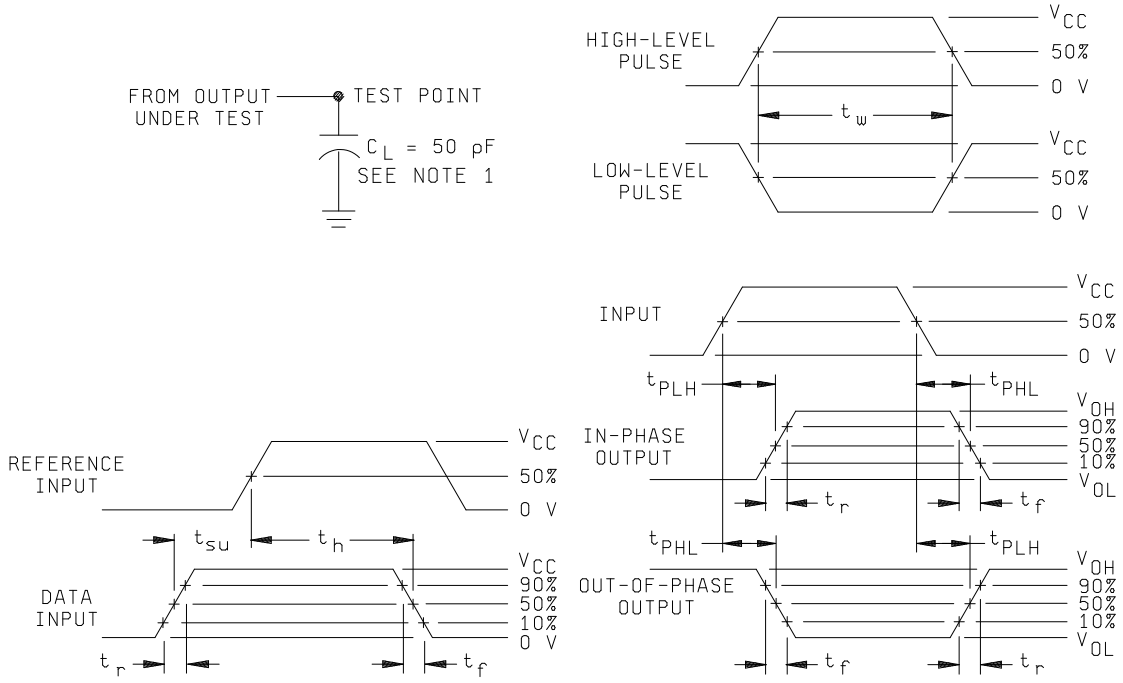


FIGURE 5. Timing waveforms and test circuit.



NOTES:

1. C_L includes probe and jig capacitance.
2. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
3. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 5. Timing waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04702-01XE	01295	CD74HC40103QM96EP	HC40103QEP

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243