

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal buffer and line driver with three-state outputs microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/04698</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	X	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	74HCT244-EP	Octal buffer and line driver with three-state outputs, TTL compatible inputs

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MO-153	Plastic small-outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7.0 V
Input clamp current (I_{IK}) ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA 2/
Output clamp current (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA 2/
Continuous output current (I_O) ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Storage temperature range (T_{STG})	-65°C to 150°C
Package thermal impedance (θ_{JA}): 3/	
X package	83°C/W

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Input voltage range (V_I)	0.0 V to V_{CC}
Output voltage range (V_O)	0.0 V to V_{CC}
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 4.5$ V to 5.5 V	2.0 V
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 4.5$ V to 5.5 V	0.8 V
Maximum input transition rise or fall time ($\Delta t/\Delta v$)	500 ns
Operating free-air temperature range (T_A)	-40°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimensions. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	V _I = V _{IH} or V _{IL} 2/ I _{OH} = -20 μA	4.5 V	25°C, -40°C to 125°C	All	4.4		V
				25°C		3.98		
				-40°C to 125°C		3.7		
Low level output voltage	V _{OL}	V _I = V _{IH} or V _{IL} 2/ I _{OL} = 20 μA	4.5 V	25°C, -40°C to 125°C	All		0.1	V
				25°C			0.26	
				-40°C to 125°C			0.40	
Input current	I _I	V _I = V _{CC} or 0 V	5.5 V	25°C	All		±100	nA
				-40°C to 125°C			±1000	
Three-state output leakage current	I _{OZ}	V _I = V _{IH} or V _{IL} 2/ V _O = V _{CC} or 0 V	5.5 V	25°C	All		±0.5	μA
				-40°C to 125°C			±10.0	
Quiescent supply current	I _{CC}	V _I = V _{CC} or 0 V I _O = 0 A	5.5 V	25°C	All		8.0	μA
				-40°C to 125°C			160.0	
Quiescent supply current delta, TTL input levels	ΔI _{CC} 3/	One input at 0.5 V or 2.4 V Other inputs at 0.0 V or V _{CC}	5.5 V	25°C	All		2.4	mA
				-40°C to 125°C			3.0	
Input capacitance	C _I		4.5 V to 5.5 V	25°C, -40°C to 125°C	All		10	pF
Power dissipation capacitance per buffer/driver	C _{PD}	No load		25°C	All	40 typical		pF
Propagation delay time, A to Y	t _{pd}	C _L = 50 pF See figure 5	4.5 V	25°C	All		28	ns
				-40°C to 125°C			42	
			5.5 V	25°C			25	
				-40°C to 125°C			38	
			4.5 V	25°C			45	
				-40°C to 125°C			68	
5.5 V	25°C		40					
	-40°C to 125°C		61					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Propagation delay time, output enable, \overline{OE} to Y	t _{en}	C _L = 50 pF See figure 5	4.5 V	25°C	All		35	ns
				-40°C to 125°C			53	
			5.5 V	25°C			32	
				-40°C to 125°C			48	
		C _L = 150 pF See figure 5	4.5 V	25°C			52	
				-40°C to 125°C			79	
			5.5 V	25°C			47	
				-40°C to 125°C			71	
Propagation delay time, output disable, \overline{OE} to Y	t _{dis}	C _L = 50 pF See figure 5	4.5 V	25°C	All		35	ns
				-40°C to 125°C			53	
			5.5 V	25°C			32	
				-40°C to 125°C			48	
Output transition time	t _t	C _L = 50 pF See figure 5	4.5 V	25°C	All		12	ns
				-40°C to 125°C			18	
			5.5 V	25°C			11	
				-40°C to 125°C			16	
		C _L = 150 pF See figure 5	4.5 V	25°C			42	
				-40°C to 125°C			63	
			5.5 V	25°C			38	
				-40°C to 125°C			57	

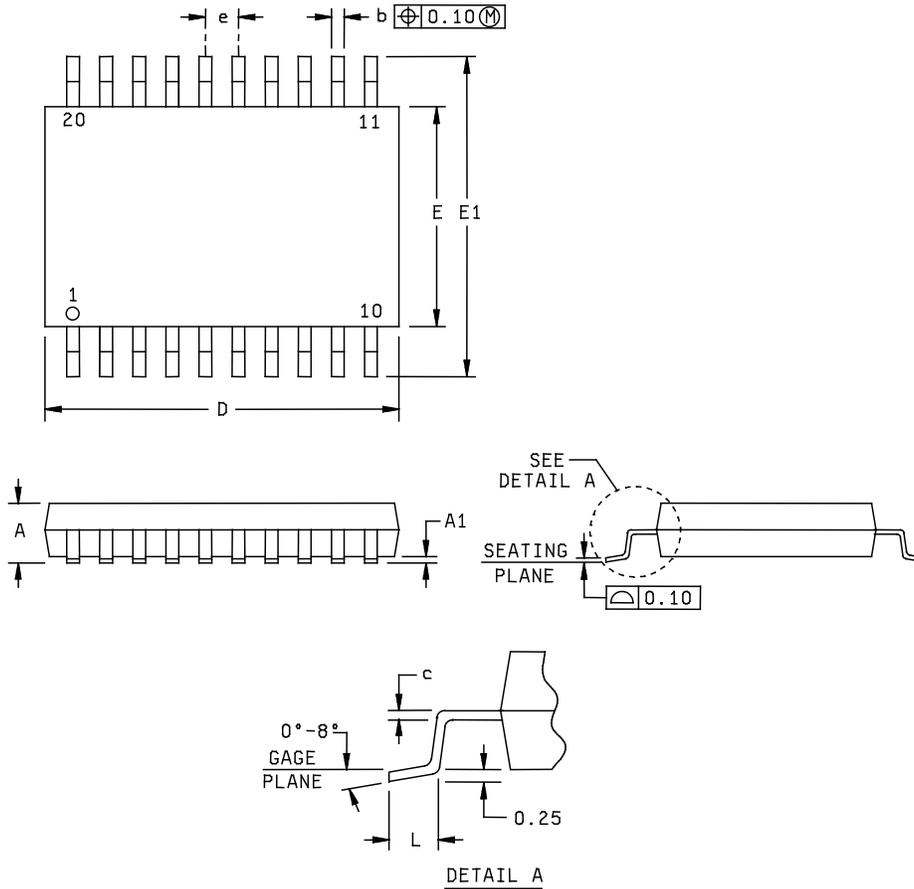
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4 herein.

3/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0.0 V or V_{CC}.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.15 NOM		L	0.50	0.75
D	6.40	6.60			

NOTES:

1. All linear dimensions are in millimeters.
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline.

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Each buffer/driver		
Inputs		Output
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

H = High voltage level Z = High impedance
L = Low voltage level X = Don't care

FIGURE 2. Truth table.

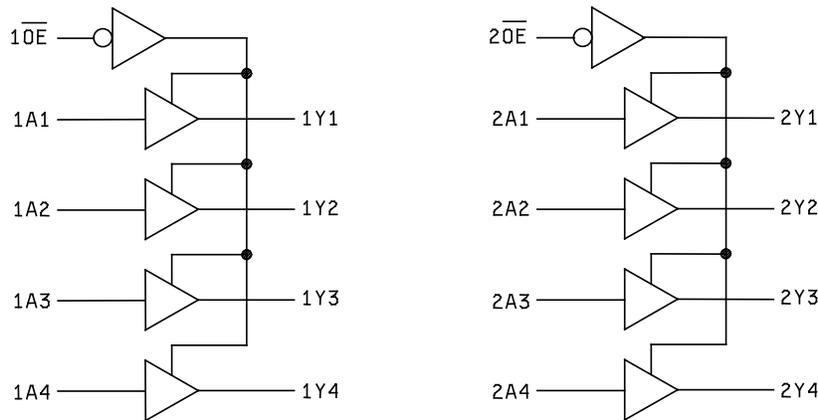
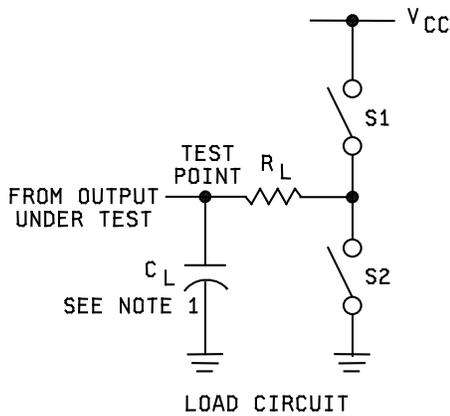


FIGURE 3. Logic diagram.

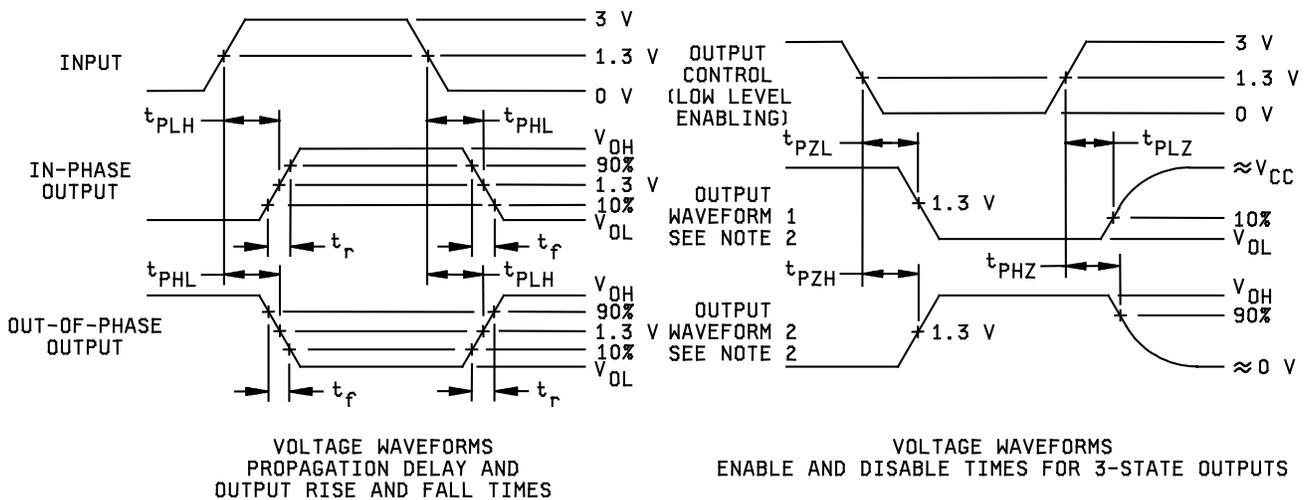
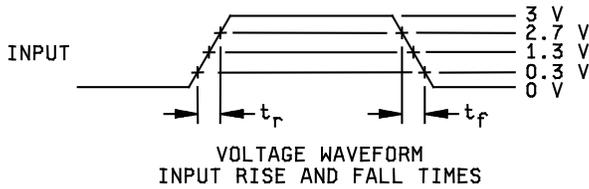
Device type 01			
Case outlines: X and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$1\overline{OE}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	$2\overline{OE}$
10	GND	20	V_{CC}

FIGURE 4. Terminal connections.

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PARAMETER		R _L	C _L	S1	S2
t _{en}	t _{PZH}	1 kΩ	50 pF	OPEN	CLOSED
	t _{PZL}		or 150 pF	CLOSED	OPEN
t _{dis}	t _{PHZ}	1 kΩ	50 pF	OPEN	CLOSED
	t _{PLZ}			CLOSED	OPEN
t _{pd} or t _t		—	50 pF or 150 pF	OPEN	OPEN



NOTES:

- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}; t_{PZL} and t_{PZH} are the same as t_{en}; t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 5. Test circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number ^{1/}	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04698-01XE	01295	SN74HCT244QPWREP	SHT244EP

^{1/} The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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