REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-12-08	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-05-20	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	23-01-18	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12										

PMIC N/A

Original date of drawing

YY MM DD

04-04-21

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TITLE
MICROCIRCUIT, DIGITAL, 8-BIT PARALLEL LOAD SHIFT REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04690
REV C		PAGE 1 OF 12

AMSC N/A

5962-V038--23

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8-bit parallel load shift register microcircuit, with an operating temperature range of -40ºC to +85ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04690	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74HC166A-EP	8-bit parallel load shift register.

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MS-012	Plastic small outline package
Y	16	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC}) ..... -0.5 V to +7.0 V
Input clamp current, (I_{IK}) ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA 2/
Output clamp current, (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA 2/
Continuous output current, (I_O) (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance (θ_{JA}): 3/
X package ..... 73°C/W
Y package ..... 108°C/W
Storage temperature range, (T_{STG}) ..... -65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output voltage ratings may exceeded if the input and output current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 4/ 5/

Supply voltage, (V_{CC}) ..... +2.0 V to +6.0 V
Minimum high level input voltage, (V_{IH}):
V_{CC} = 2.0 V ..... +1.5 V
V_{CC} = 4.5 V ..... +3.15 V
V_{CC} = 6.0 V ..... +4.2 V
Maximum low level input voltage, (V_{IL}):
V_{CC} = 2.0 V ..... +0.5 V
V_{CC} = 4.5 V ..... +1.35 V
V_{CC} = 6.0 V ..... +1.8 V
Input voltage, (V_I) ..... 0.0 V to V_{CC}
Output voltage, (V_O) ..... 0.0 V to V_{CC}
Maximum input transition rise/fall rate ($\Delta t/\Delta v$) 6/
V_{CC} = 2.0 V ..... 1000 ns
V_{CC} = 4.5 V ..... 500 ns
V_{CC} = 6.0 V ..... 400 ns
Operating free air temperature, (T_A): ..... -40°C to +85°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https:/www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Sequence waveforms. The sequence waveforms shall be as shown in figure 5.

3.5.6 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as specified in figure 6.

TABLE I. Electrical performance characteristics. 1/

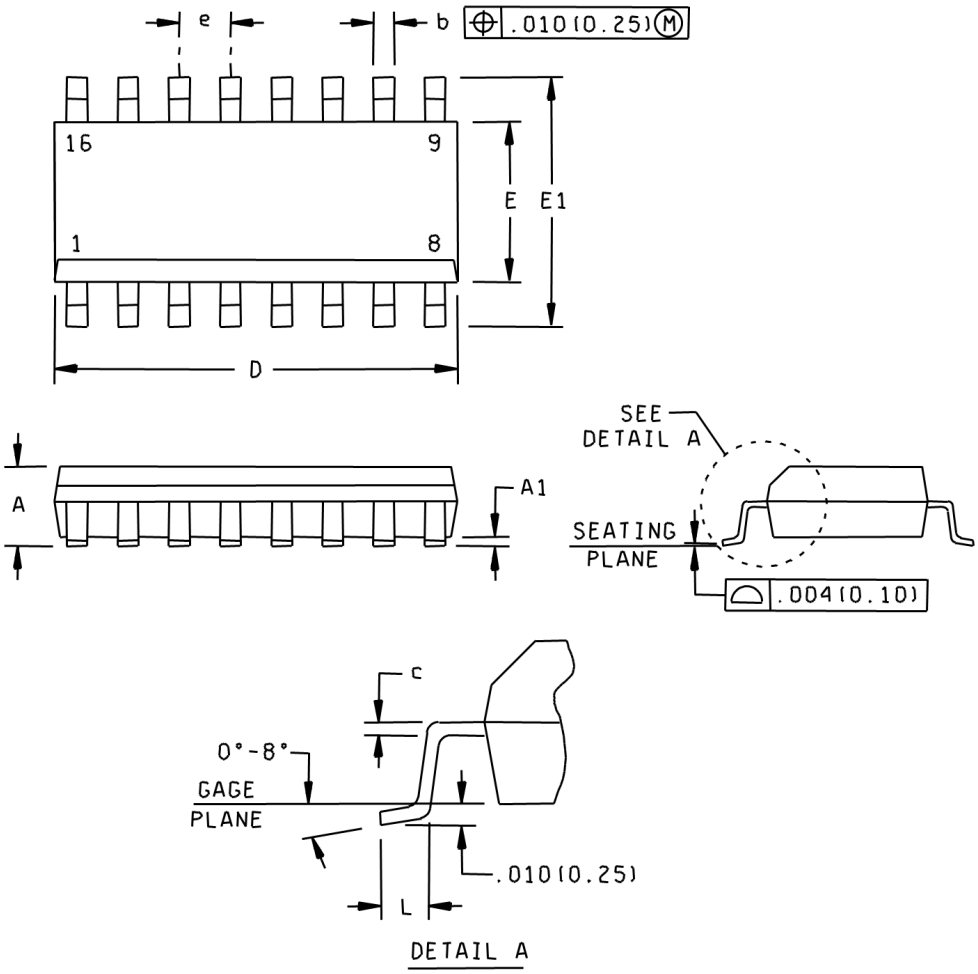
Test	Symbol	Conditions		V_{CC}	T_A = 25°C		-40°C ≤ T_A ≤+85°C		Unit
					Min	Max	Min	Max	
High level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20 μA	2.0 V	1.9		1.9		V
				4.5 V	4.4		4.4		
				6.0 V	5.9		5.9		
			I_{OH} = -4.0 mA	4.5 V	3.98		3.84		
			I_{OH} = -5.2 mA	6.0 V	5.48		5.34		
Low level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2.0 V		0.1		0.1	
				4.5 V		0.1		0.1	
				6.0 V		0.1		0.1	
			I_{OL} = 4.0 mA	4.5 V		0.26		0.33	
			I_{OL} = 5.2 mA	6.0 V		0.26		0.33	
Input current	I_I	$V_I = V_{CC}$ or 0		6.0 V		±100		±1000	nA
Quiescent supply current	I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6.0 V		8		80	μA
Input capacitance	C_I			2.0 V to 6.0 V		10		10	pF
Timing requirements									
Clock frequency	f_{clock}			2.0 V		6		5	MHz
				4.5 V		31		25	
				6.0 V		36		29	
Pulse duration	t_w	$\overline{CLR}$ low		2.0 V	100		125		ns
				4.5 V	20		25		
				6.0 V	17		21		
		CLK high or low		2.0 V	80		100		
				4.5 V	16		20		
				6.0 V	14		17		
Setup time	t_{su}	SH/$\overline{LD}$ high before CLK↑		2.0 V	145		180		
				4.5 V	29		36		
				6.0 V	25		31		
		SER before CLK↑		2.0 V	80		100		
				4.5 V	16		20		
				6.0 V	14		17		
		CLK INH low before CLK↑		2.0 V	100		125		
				4.5 V	20		25		
				6.0 V	17		21		
		Data before CLK↑		2.0 V	80		100		
				4.5 V	16		20		
				6.0 V	14		17		
		$\overline{CLR}$ inactive before CLK↑		2.0 V	40		50		
				4.5 V	8		10		
				6.0 V	7		9		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{CC}	T_A = 25°C		-40°C ≤ T_A ≤+85°C		Unit
				Min	Max	Min	Max	
Timing requirements - Continued								
Hold time	t_h	SH/$\overline{LD}$ high after CLK↑	2.0 V	0		0		ns
			4.5 V	0		0		
			6.0 V	0		0		
		SER after CLK↑	2.0 V	5		5		
			4.5 V	5		5		
			6.0 V	5		5		
		CLK INH high after CLK↑	2.0 V	0		0		
			4.5 V	0		0		
			6.0 V	0		0		
		Data after CLK↑	2.0 V	5		5		
			4.5 V	5		5		
			6.0 V	5		5		
Switching characteristics								
Maximum frequency	f_{max}		2.0 V	6		5		MHz
			4.5 V	31		25		
			6.0 V	36		29		
From input $\overline{CLR}$ to output Q_H	t_{PHL}		2.0 V		120		150	ns
			4.5 V		24		30	
			6.0 V		20		26	
From input CLK to output Q_H	t_{pd}		2.0 V		150		190	
			4.5 V		30		38	
			6.0 V		26		32	
Transition time from any input to output	t_t		2.0 V		75		95	
			4.5 V		15		19	
			6.0 V		13		16	
Power dissipation capacitance	C_{pd}	No load	2.0 V	50	Typ			pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

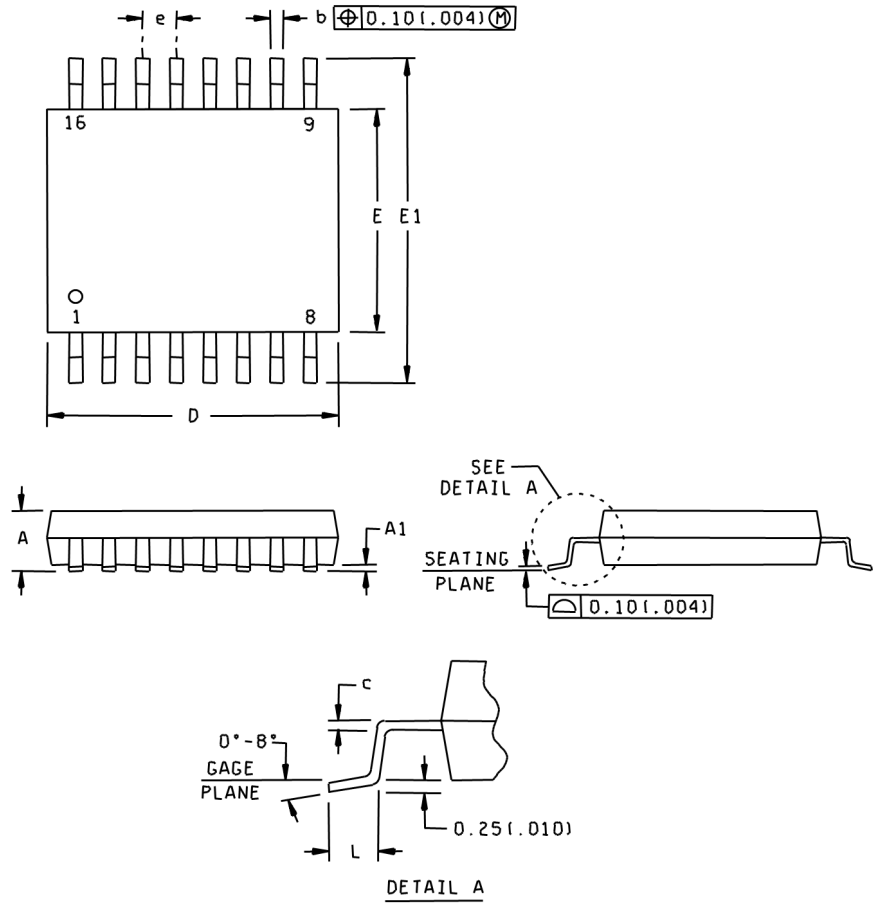


Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.069	---	1.75	E	0.150	0.157	3.81	4.00
A1	0.004	0.010	0.10	0.25	E1	0.228	0.244	5.80	6.20
b	0.014	0.020	0.35	0.51	e	0.050 BSC		1.27 BSC	
c	0.008 NOM		0.20 NOM		L	0.016	0.050	0.40	1.27
D	0.386	0.394	9.80	10.00					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 inches (0.15 mm).
4. Falls within JEDEC MS-012.

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.047	---	1.20	E	0.169	0.177	4.30	4.50
A1	0.002	0.006	0.05	0.15	E1	0.244	0.260	6.20	6.60
b	0.007	0.012	0.19	0.30	e	0.026 BSC		0.65 BSC	
c	0.006 NOM		0.15 NOM		L	0.020	0.030	0.50	0.75
D	0.193	0.200	4.90	5.10					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0.15).
4. Fall within JEDEC MO-153

FIGURE 1. Case outlines - Continued.

Case X or Y

Pin No.	Signal name	Pin No.	Signal name
1	SER	9	$\overline{CLR}$
2	A	10	E
3	B	11	F
4	C	12	G
5	D	13	Q_H
6	CLK INH	14	H
7	CLK	15	SH/$\overline{LD}$
8	GND	16	V_{CC}

FIGURE 2. Terminal connections.

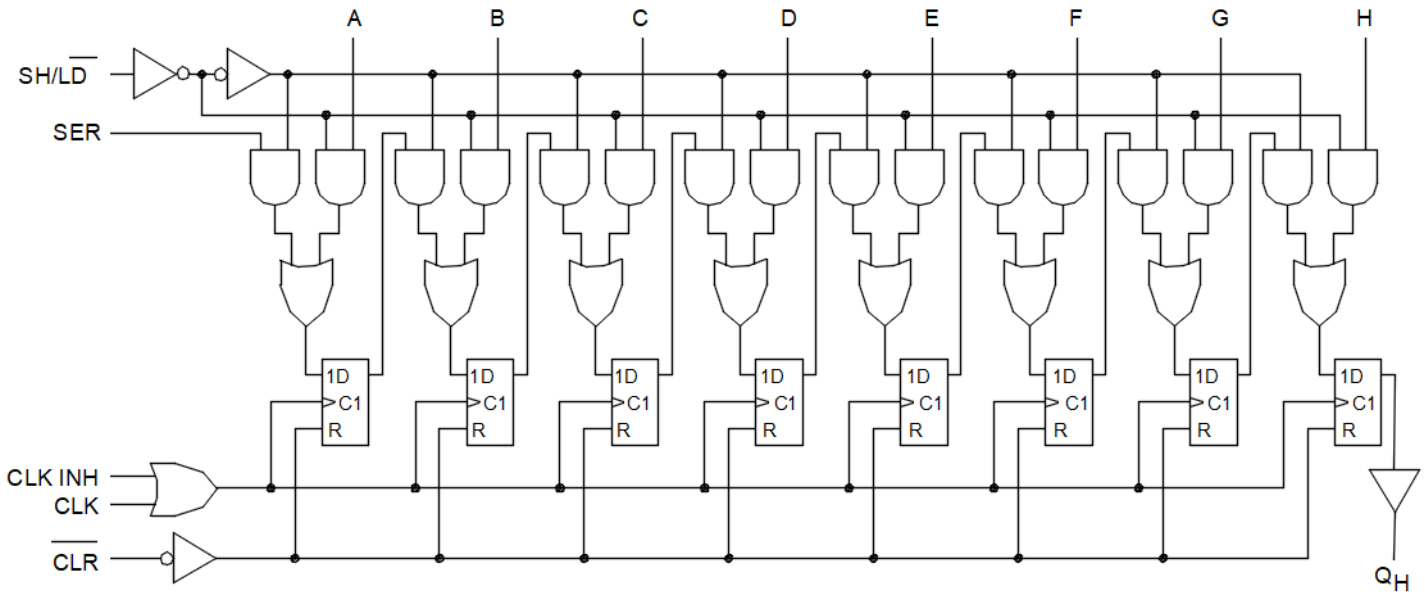


FIGURE 3. Logic diagram.

Inputs						Outputs		
						Inter nal		Q_H
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	CLK	SER	Parallel A….H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a…..h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

FIGURE 4. Function Table

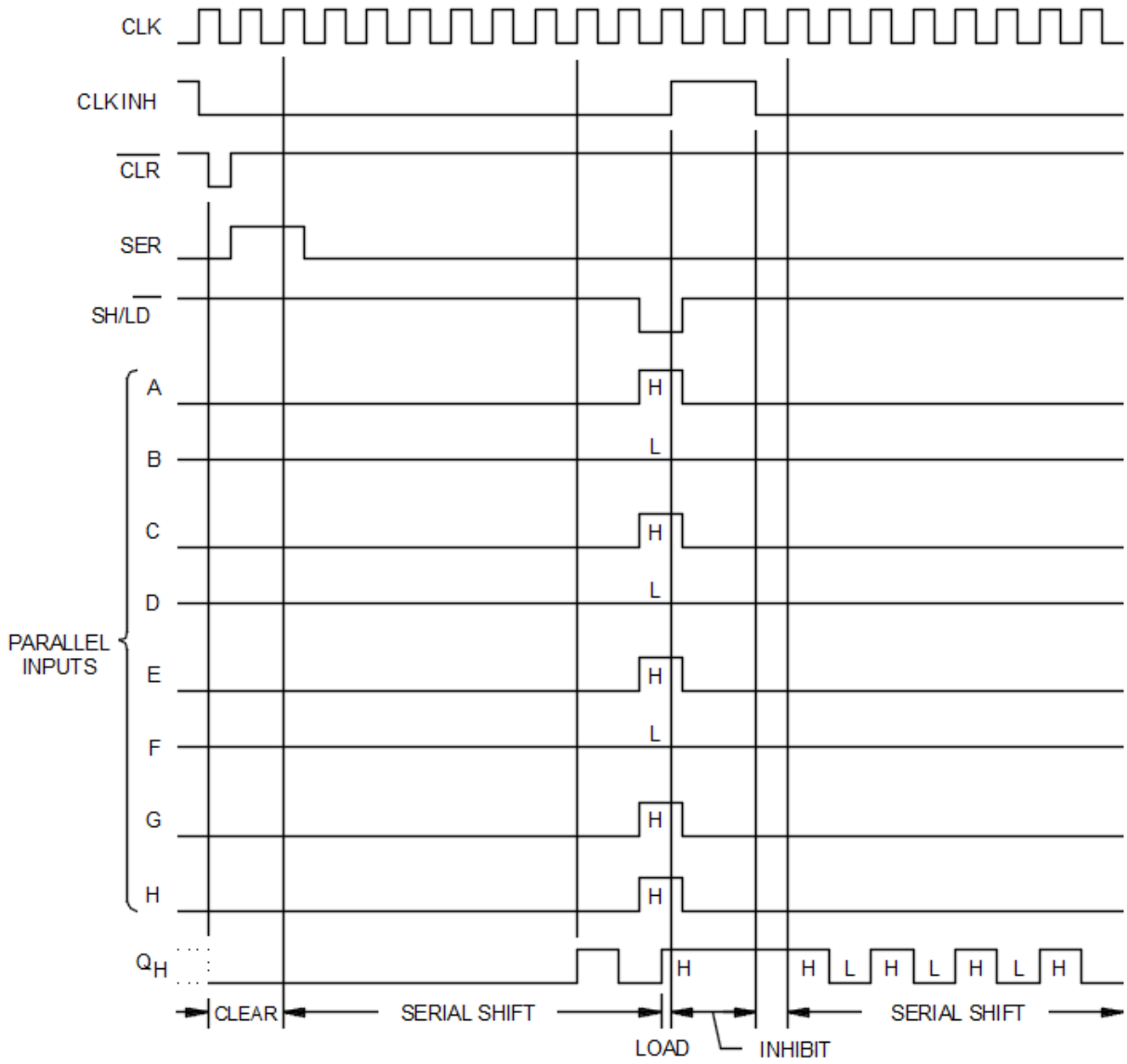
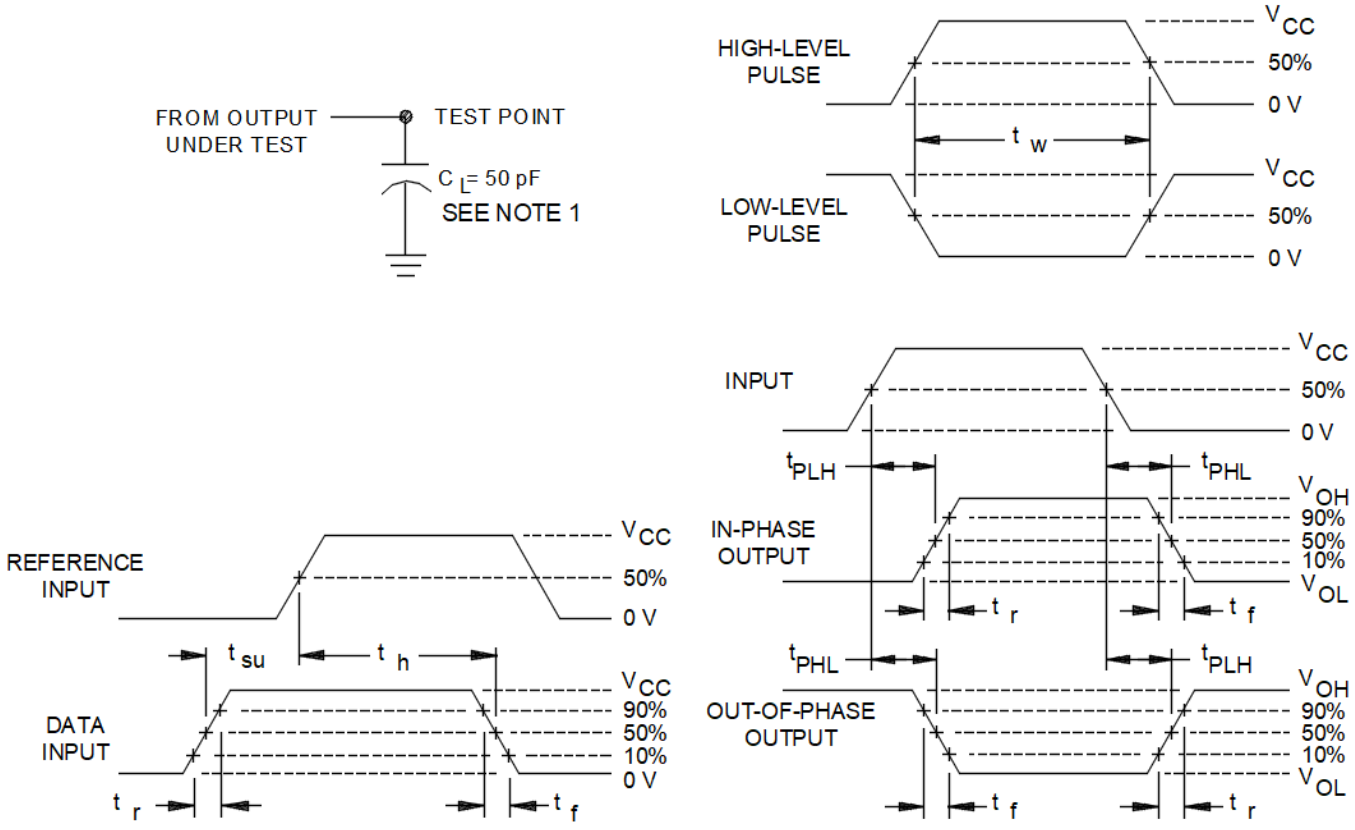


FIGURE 5. Sequence waveforms.



SETUP AND HOLD AND RISE AND FALL TIMES

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Notes:

1. C_L includes probe and test fixture capacitance.
2. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
3. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLH} and t_{PHL} are the same t_{pd}.

FIGURE 6. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04690-01XE	01295	SN74HC166AIDREP	SHC166IEP
V62/04690-01YE	01295	2/	SHC1661EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not yet available from a source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243