REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-10-19	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-04-18	Muhammad A. Akbar
C	Update boilerplate paragraphs to current VID description requirements. - PHN	22-12-15	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C												
SHEET	1	2	3	4	5	6	7	8	9	10												

PMIC N/A

Original date of drawing

YY MM DD

04-03-29

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DEFENSE SUPPLY CENTER, COLUMBUS
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

TITLE
MICROCIRCUIT, LINEAR, QUADRUPLE 2-INPUT POSITIVE NAND GATE, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04685
REV C		PAGE 1 OF 10

AMSC N/A

5962-V028-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quadruple 2-input positive NAND gate microcircuit, with an operating temperature range of -40ºC to +85ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04685	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74ALVC00-EP	Quadruple 2-input NAND gate

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MS-012	Plastic small outline package
Y	14	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC}) ..... -0.5 V to +4.6 V
Input voltage range, (V_I) ..... -0.5 V to +4.6 V 2/
Output voltage range, (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/ 3/
Input clamp current, (I_{IK}) (V_I < 0) ..... -50 mA
Output clamp current, (I_{OK}) (V_O < 0) ..... -50 mA
Continuous output current, (I_O) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Package thermal impedance (θ_{JA}): 4/
X package ..... 86°C/W
Y package ..... 113°C/W
Storage temperature range, (T_{STG})..... -65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative voltage and output voltage ratings may exceed if the input and output current ratings are observed.
3/ This value is limited to 4.6 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 5/ 6/

Supply voltage, (V_{CC})	+1.65 V to +3.6 V
Minimum high level input voltage, (V_{IH}):	
V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}
V_{CC} = 2.3 V to 2.7 V	+1.7 V
V_{CC} = 2.7 V to 3.6 V	+2.0 V
Maximum low level input voltage, (V_{IL}):	
V_{CC} = 1.65 V to 1.95 V	0.35V_{CC}
V_{CC} = 2.3 V to 2.7 V	+0.7 V
V_{CC} = 2.7 V to 3.6 V	+0.8 V
Input voltage range, (V_I)	0.0 V to +3.6 V
Output voltage range, (V_O)	0.0 V to V_{CC}
Maximum high level output current, (I_{OH}):	
V_{CC} = 1.65 V	-4.0 mA
V_{CC} = 2.3 V	-12.0 mA
V_{CC} = 2.7 V	-12.0 mA
V_{CC} = 3.0 V	-24.0 mA
Maximum low level output current, (I_{OL}):	
V_{CC} = 1.65 V	+4.0 mA
V_{CC} = 2.3 V	+12.0 mA
V_{CC} = 2.7 V	+12.0 mA
V_{CC} = 3.0 V	+24.0 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$)	5 ns/V
Operating free air temperature, (T_A)	-40°C to +85°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

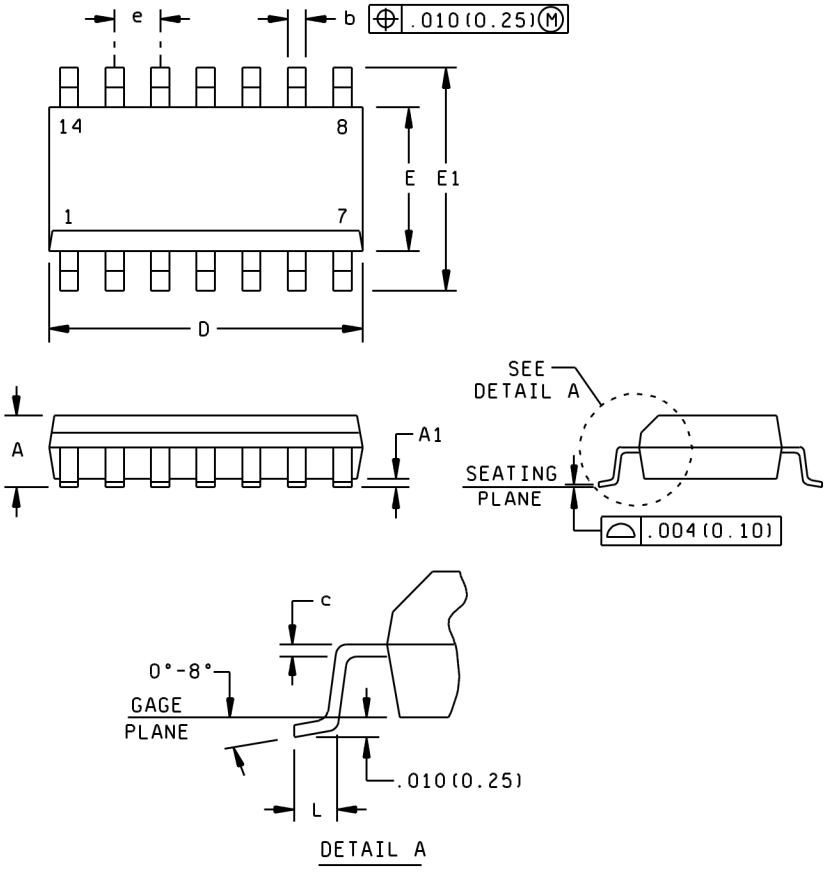
3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-40°C \le T_A \le +85°C$	V_{CC}	Limit		Unit
				Min	Max	
High level output voltage	V_{OH}	I_{OH} = -100 μA	1.65 V to 3.6 V	V_{CC}-0.2		V
		I_{OH} = -4.0 mA	1.65 V	1.2		
		I_{OH} = -6.0 mA	2.3 V	2.0		
		I_{OH} = -12.0 mA	2.3 V	1.7		
			2.7 V	2.2		
			3.0 V	2.4		
		I_{OH} = -24.0 mA	3.0 V	2.0		
Low level output voltage	V_{OL}	I_{OL} = 100 μA	1.65 V to 3.6 V		0.2	
		I_{OL} = 4.0 mA	1.65 V		0.45	
		I_{OL} = 6.0 mA	2.3 V		0.4	
		I_{OL} = 12.0 mA	2.3 V		0.7	
			2.7 V		0.4	
		I_{OL} = 24.0 mA	3.0 V		0.55	
Input current	I_I	$V_I = V_{CC}$ or GND	3.6 V		±5.0	μA
Quiescent supply current	I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0 V	3.6 V		10	
Quiescent supply current delta	ΔI_{CC}	One input at V_{CC}-0.6 V, Other inputs at V_{CC} or GND	3.0 V to 3.6 V		750	
Input capacitance	C_I	$V_I = V_{CC}$ or GND, T_A = 25°C	3.3 V	4.5 Typ		pF
Switching characteristics						
From input A or B to output Y	t_{Pd}		1.8 ±0.15 V	1	4.4	ns
			2.5 ±0.2 V	1	2.8	
			2.7 V		3.2	
			3.3 ±0.3 V	0.5	3.0	
Operating characteristics						
Power dissipation capacitance per gate	C_{Pd}	T_A = 25°C, CL = 0, f = 10 MHz	1.8 V	20 Typ		pF
			2.5 V	21 Typ		
			3.3 V	23 Typ		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

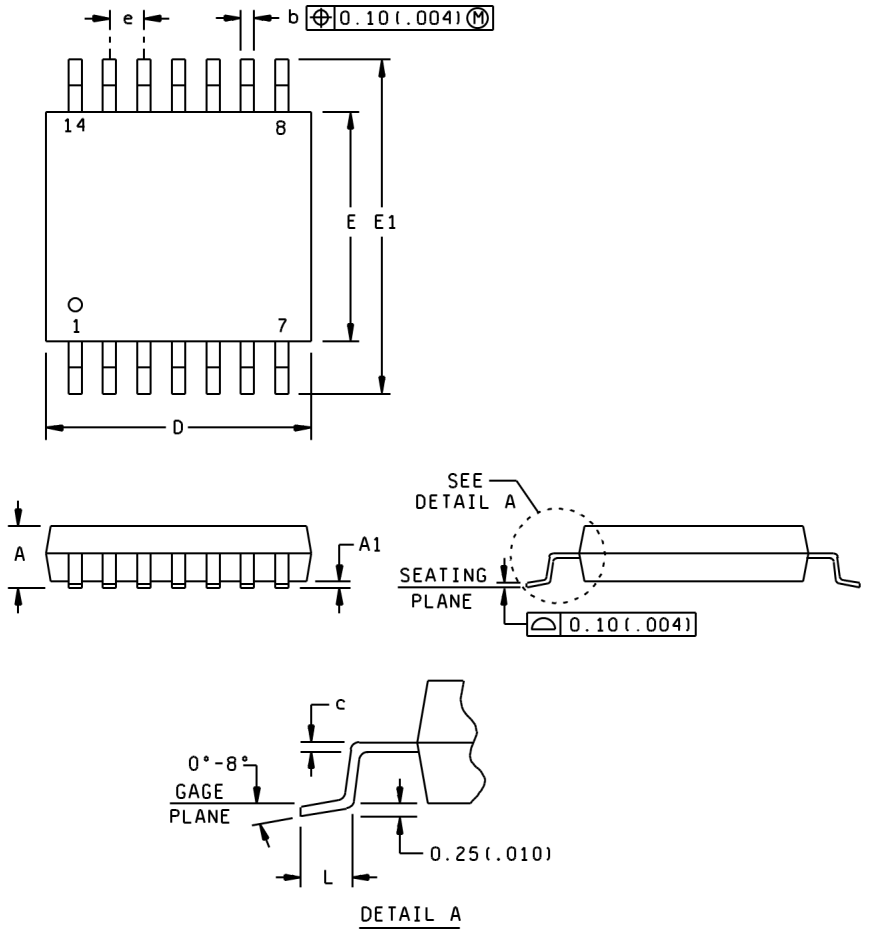


Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.069	---	1.75	E	0.150	0.157	3.81	4.00
A1	0.004	0.010	0.10	0.25	E1	0.228	0.244	5.80	6.20
b	0.014	0.020	0.35	0.51	e	0.050 BSC		1.27 BSC	
c	0.008 NOM		0.20 NOM		L	0.016	0.044	0.40	1.12
D	0.337	0.344	8.55	8.75					

Notes:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0.15).
4. Fall within JEDEC MS-012

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.047	---	1.20	E	0.169	0.177	4.30	4.50
A1	0.002	0.006	0.05	0.15	E1	0.244	0.260	6.20	6.60
b	0.007	0.012	0.19	0.30	e	0.026 BSC		0.65 BSC	
c	0.006 NOM		0.15 NOM		L	0.020	0.030	0.50	0.75
D	0.193	0.200	4.90	5.10					

Notes:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0.15).
4. Fall within JEDEC MO-153

FIGURE 1. Case outlines - Continued.

Case X or Y

Pin No.	Signal name	Pin No.	Signal name
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FIGURE 2. Terminal connections.

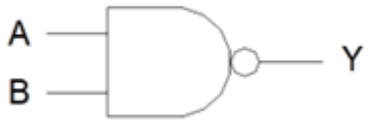
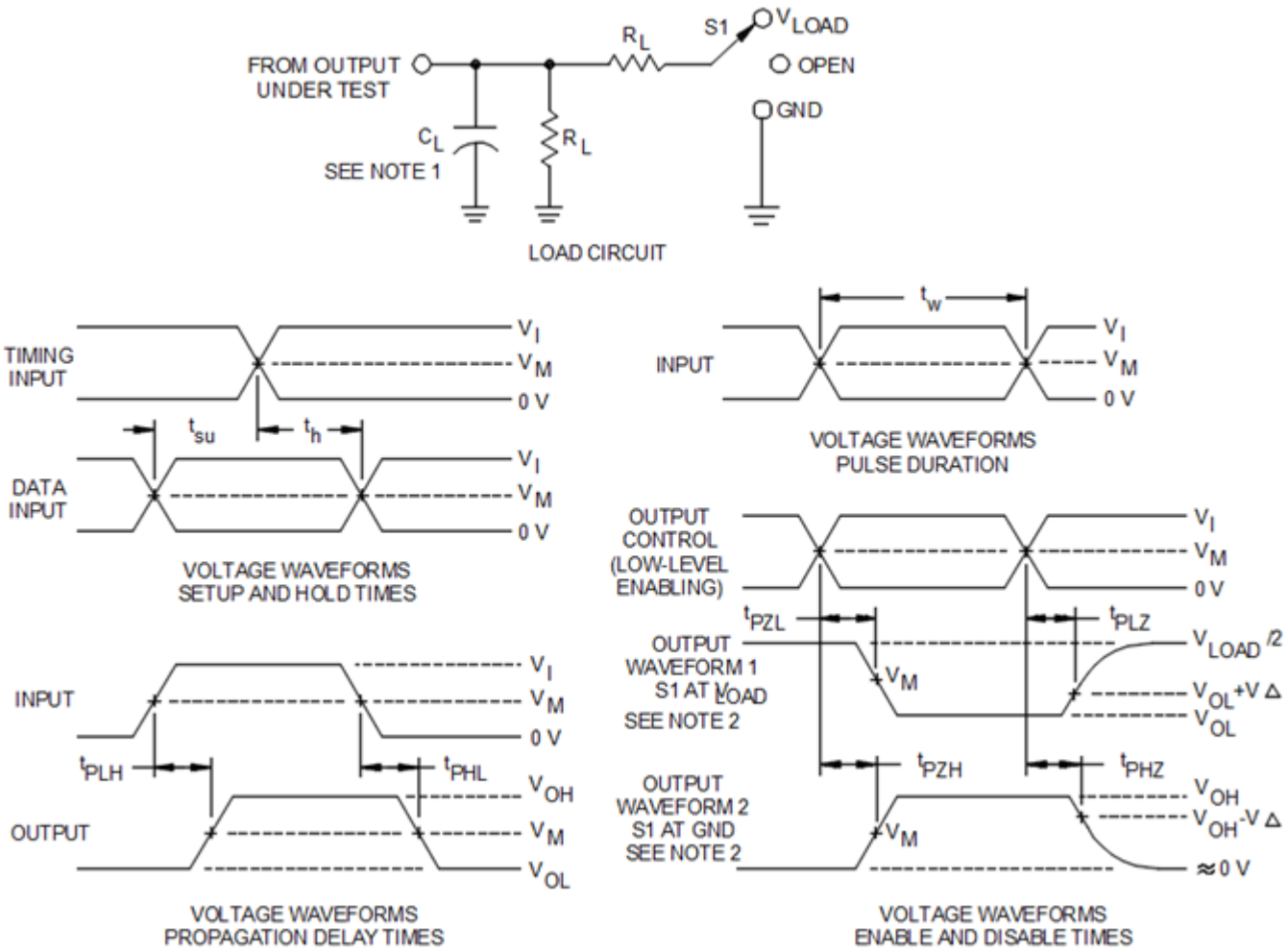


FIGURE 3. Logic diagram.

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

FIGURE 4. Function Table



V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 ±0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 ±0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	30 pF	500 Ω	0.3 V
3.3 ±0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	30 pF	500 Ω	0.3 V

Test	S1
tpd	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Notes:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis}.
6. t_{PZL} and t_{PZH} are the same t_{en}.
7. t_{PLH} and t_{PHL} are the same t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04685-01XE	01295	SN74ALVC00IDREP	ALVC00IEP
V62/04685-01YE	01295	2/	ALVC00E

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not yet available from a source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243