REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make clarification to paragraph 1.2.2 and update the boilerplate paragraphs. Add a footnote to Table I and paragraph 6.3. Make changes to the notes under figure 1. - ro	09-03-10	R. HEBER

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	A	A	A	A	A																
PAGE	18	19	20	21	22																
REV STATUS OF PAGES		REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
		PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990
Original date of drawing YY-MM-DD 04-02-12	CHECKED BY TOM HESS APPROVED BY RAYMOND MONNIN	TITLE MICROCIRCUIT, LINEAR, DUAL/QUAD, RAIL TO RAIL, LOW POWER, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	SIZE A	CODE IDENT. NO. 16236	DWG NO. **V62/04682**
	REV A	PAGE 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual / quad rail to rail, low power, operational amplifier microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04682	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TLC2252	Dual, rail to rail, low power, operational amplifier
02	TLC2252A	Dual, rail to rail, low power, operational amplifier with enhanced V_{IO}
03	TLC2254	Quad, rail to rail, low power, operational amplifier
04	TLC2254A	Quad, rail to rail, low power, operational amplifier with enhanced V_{IO}

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic surface mount
Y	14	MS-012-AB	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (+V_{DD}) .... +8 V 2/
Supply voltage range (-V_{DD}) .... -8 V 2/
Differential input voltage (V_{ID}) .... ±16 V 3/
Input voltage range (V_I) (any input) .... ±8 V 2/
Input current (I_I) (each input) .... ±5 mA
Output current (I_O) .... ±50 mA
Total current into +V_{DD} .... ±50 mA
Total current into -V_{DD} .... ±50 mA
Duration of short-circuit current (at or below) 25°C .... Unlimited 4/
Continuous total dissipation (P_D) .... See 1.5, Dissipation rating table
Operating free-air temperature range (T_A) (Q suffix) .... -40°C to +125°C
Storage temperature range (T_{STG}) .... -65°C to +150°C
Lead temperature, 1.6 mm (1/16 inch) from case for 10 seconds .... +260°C

1.4 Recommended operating conditions. 5/

Supply voltage (±V_{DD}) .... ±2.2 V minimum to ±8 V maximum
Input voltage range (V_I) .... -V_{DD} minimum to +V_{DD} –1.5 V maximum
Common mode input voltage (V_{IC}) .... -V_{DD} minimum to +V_{DD} –1.5 V maximum
Operating free-air temperature range (T_A) .... -40°C to +125°C

1.5 Dissipation rating table.

Package	$T_A \leq$ 25°C power rating	Derating factor above T_A = 25°C	T_A = 70°C power rating	T_A = 85°C power rating	T_A = 125°C power rating
X	724 mW	5.8 mW/°C	464 mW	377 mW	144 mW
Y	950 mW	7.6 mW/°C	608 mW	450 mW	190 mW

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential voltages, are with respect to +V_{DD} and –V_{DD}.

3/ Differential voltages are at the +IN with respect to the -IN. Excessive current flows when input is brought below –V_{DD} –0.3 V.

4/ The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{DD} = 5 V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$\pm V_{DD} = \pm 2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C	01		1500	µV
				02		850	
			-40°C to +125°C	01		1750	
				02		1000	
Temperature coefficient of input offset voltage	αV_{IO}	$\pm V_{DD} = \pm 2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C to +125°C	01,02	0.5 typical		µV / °C
Input offset voltage 3/ long term drift	DV_{IO}	$\pm V_{DD} = \pm 2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C	01,02	0.003 typical		µV / mo
Input offset current	I_{IO}	$\pm V_{DD} = \pm 2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C	01,02		60	pA
			-40°C to +125°C			1000	
Input bias current	I_{IB}	$\pm V_{DD} = \pm 2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C	01,02		60	pA
			-40°C to +125°C			1000	
Common mode input voltage range	V_{ICR}	$\|V_{IO}\| \leq 5$ mV, R_S = 50 Ω	25°C	01,02	0 to 4		V
			-40°C to +125°C		0 to 3.5		
High level output voltage	V_{OH}	I_{OH} = -20 µA	25°C	01,02	4.98 typical		V
		I_{OH} = -75 µA	25°C		4.9		
			-40°C to +125°C		4.8		
		I_{OH} = -150 µA	25°C		4.8		
Low level output voltage	V_{OL}	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C	01,02	0.01 typical		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C			0.15	
			-40°C to +125°C			0.15	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C			1	
			-40°C to +125°C			1.2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{DD} = 5 V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits		Unit
					Min	Max	
Large signal differential voltage amplification	A_{VD}	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 100 kΩ referenced to 2.5 V	25°C	01,02	100		V / mV
			-40°C to +125°C		10		
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ referenced to 2.5 V	25°C		1700 typical		
Differential input resistance	$r_{i(d)}$		25°C	01,02	10^{12} typical		Ω
Common mode input resistance	$r_{i(c)}$		25°C	01,02	10^{12} typical		Ω
Common mode input capacitance	$c_{i(c)}$	f = 10 kHz	25°C	01,02	8 typical		pF
Closed loop output impedance	z_o	f = 25 kHz, A_V = 10	25°C	01,02	200 typical		Ω
Common mode rejection ratio	CMRR	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	01,02	70		dB
			-40°C to +125°C		70		
Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	k_{SVR}	V_{DD} = 4.4 V to 16 V, no load, V_{IC} = V_{DD} / 2	25°C	01,02	80		dB
			-40°C to +125°C		80		
Supply current	I_{DD}	V_O = 2.5 V, no load	25°C	01,02		125	μA
			-40°C to +125°C			150	
Slew rate at unity gain	SR	V_O = 0.5 V to 3.5 V, R_L = 100 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	01,02	0.07		V / μs
			-40°C to +125°C		0.05		
Equivalent input noise voltage	V_n	f = 10 Hz	25°C	01,02	36 typical		nV / $\sqrt{Hz}$
		f = 1 kHz			19 typical		
Peak to peak equivalent input noise voltage	$V_{N(PP)}$	f = 0.1 Hz to 1 Hz	25°C	01,02	0.7 typical		μV
		f = 0.1 Hz to 10 Hz			1.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{DD} = 5 V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits		Unit
					Min	Max	
Equivalent input noise current	I_n		25°C	01,02	0.6 typical		fA / $\sqrt{Hz}$
Total harmonic distortion plus noise	THD+N	A_V = 1, V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ referenced to 2.5 V	25°C	01,02	0.2 % typical		
		A_V = 10, V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ referenced to 2.5 V			1 % typical		
Gain bandwidth product	GBWP	f = 50 kHz, R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	01,02	0.2 typical		MHz
Maximum output swing bandwidth	B_{OM}	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	01,02	30 typical		kHz
Phase margin at unity gain	ϕm	R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	01,02	63° typical		
Gain margin	Gm	R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	01,02	15 typical		dB

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Full range is –40°C to +125°C for Q suffix.

3/ Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions $\pm V_{DD} = \pm 5$ V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	01		1500	µV
				02		850	
			-40°C to +125°C	01		1750	
				02		1000	
Temperature coefficient of input offset voltage	αV_{IO}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C to +125°C	01,02	0.5 typical		µV / °C
Input offset voltage 3/ long term drift	DV_{IO}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	01,02	0.003 typical		µV / mo
Input offset current	I_{IO}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	01,02		60	pA
			-40°C to +125°C			1000	
Input bias current	I_{IB}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	01,02		60	pA
			-40°C to +125°C			1000	
Common mode input voltage range	V_{ICR}	$\|V_{IO}\| \leq 5$ mV, $R_S = 50\ \Omega$	25°C	01,02	-5 to 4		V
			-40°C to +125°C		-5 to 3.5		
Maximum positive peak output voltage	$+V_{OM}$	$I_O = -20\ \mu A$	25°C	01,02	4.98 typical		V
		$I_O = -100\ \mu A$	25°C		4.9		
			-40°C to +125°C		4.7		
		$I_O = -200\ \mu A$	25°C		4.8		
Maximum negative peak output voltage	$-V_{OM}$	$V_{IC} = 0$ V, $I_O = 50\ \mu A$	25°C	01,02	-4.99 typical		V
		$V_{IC} = 0$ V, $I_O = 500\ \mu A$	25°C		-4.85		
			-40°C to +125°C		-4.85		
		$V_{IC} = 0$ V, $I_O = 4$ mA	25°C		-4		
			-40°C to +125°C		-3.8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions $\pm V_{DD} = \pm 5$ V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits		Unit
					Min	Max	
Large signal differential voltage amplification	A_{VD}	$V_O = \pm 4$ V, $R_L = 100$ kΩ	25°C	01,02	40		V/mV
			-40°C to +125°C		10		
		$V_O = \pm 4$ V, $R_L = 1$ MΩ	25°C		3000 typical		
Differential input resistance	$r_{i(d)}$		25°C	01,02	10^{12} typical		Ω
Common mode input resistance	$r_{i(c)}$		25°C	01,02	10^{12} typical		Ω
Common mode input capacitance	$c_{i(c)}$	f = 10 kHz, X package	25°C	01,02	8 typical		pF
Closed loop output impedance	z_o	f = 25 kHz, $A_V = 10$	25°C	01,02	190 typical		Ω
Common mode rejection ratio	CMRR	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$ V, $R_S = 50$ Ω	25°C	01,02	75		dB
			-40°C to +125°C		75		
Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	k_{SVR}	$V_{DD} = \pm 2.2$ V to ± 8 V, no load, $V_{IC} = 0$	25°C	01,02	80		dB
			-40°C to +125°C		80		
Supply current	I_{DD}	$V_O = 2.5$ V, no load	25°C	01,02		125	µA
			-40°C to +125°C			150	
Slew rate at unity gain	SR	$V_O = \pm 2$ V, $R_L = 100$ kΩ, $C_L = 100$ pF	25°C	01,02	0.07		V / µs
			-40°C to +125°C		0.05		
Equivalent input noise voltage	V_n	f = 10 Hz	25°C	01,02	38 typical		nV / $\sqrt{Hz}$
		f = 1 kHz			19 typical		
Peak to peak equivalent input noise voltage	$V_{N(PP)}$	f = 0.1 Hz to 1 Hz	25°C	01,02	0.8 typical		µV
		f = 0.1 Hz to 10 Hz			1.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions $\pm V_{DD} = \pm 5$ V, unless otherwise specified	Temperature, T_A 2/	Device type	Limits Min	Limits Max	Unit
Equivalent input noise current	I_n		25°C	01,02	0.6 typical		fA / $\sqrt{Hz}$
Total harmonic distortion plus noise	THD+N	$A_V = 1$, $V_O = \pm 2.3$ V, f = 10 kHz, $R_L = 50$ kΩ	25°C	01,02	0.2 % typical		
		$A_V = 10$, $V_O = \pm 2.3$ V, f = 10 kHz, $R_L = 50$ kΩ			1 % typical		
Gain bandwidth product	GBWP	f = 10 kHz, $R_L = 50$ kΩ, $C_L = 100$ pF	25°C	01,02	0.21 typical		MHz
Maximum output swing bandwidth	B_{OM}	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 50$ kΩ, $C_L = 100$ pF	25°C	01,02	14 typical		kHz
Phase margin at unity gain	ϕm	$R_L = 50$ kΩ, $C_L = 100$ pF	25°C	01,02	63° typical		
Gain margin	Gm	$R_L = 50$ kΩ, $C_L = 100$ pF	25°C	01,02	15 typical		dB

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Full range is –40°C to +125°C for Q suffix.

3/ Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{DD} = 5 V, unless otherwise specified	Temperature, T_A 2/	Device type	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$\pm V_{DD} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03		1500	µV
				04		850	
			-40°C to +125°C	03		1750	
				04		1000	
Temperature coefficient of input offset voltage	αV_{IO}	$\pm V_{DD} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C to +125°C	03,04	0.5 typical		µV / °C
Input offset voltage long term drift 3/	DV_{IO}	$\pm V_{DD} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03,04	0.003 typical		µV / mo
Input offset current	I_{IO}	$\pm V_{DD} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03,04		60	pA
			+125°C			1000	
Input bias current	I_{IB}	$\pm V_{DD} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03,04		60	pA
			+125°C			1000	
Common mode input voltage range	V_{ICR}	$\lvert V_{IO}\rvert \leq 5$ mV, $R_S = 50\ \Omega$	25°C	03,04	0 to 4		V
			-40°C to +125°C		0 to 3.5		
High level output voltage	V_{OH}	$I_{OH} = -20\ \mu A$	25°C	03,04	4.98 typical		V
		$I_{OH} = -75\ \mu A$	25°C		4.9		
			-40°C to +125°C		4.8		
		$I_{OH} = -150\ \mu A$	25°C		4.8		
Low level output voltage	V_{OL}	$V_{IC} = 2.5$ V, $I_{OL} = 50\ \mu A$	25°C	03,04	0.01 typical		mV
		$V_{IC} = 2.5$ V, $I_{OL} = 500\ \mu A$	25°C			0.15	
			-40°C to +125°C			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 4$ mA	25°C			1	
			-40°C to +125°C			1.2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{DD} = 5 V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits		Unit
					Min	Max	
Large signal differential voltage amplification	A_{VD}	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 100 kΩ referenced to 2.5 V	25°C	03,04	100		V/mV
			-40°C to +125°C		10		
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ referenced to 2.5 V	25°C		1700 typical		
Differential input resistance	$r_{i(d)}$		25°C	03,04	10^{12} typical		Ω
Common mode input resistance	$r_{i(c)}$		25°C	03,04	10^{12} typical		Ω
Common mode input capacitance	$c_{i(c)}$	f = 10 kHz, Y package	25°C	03,04	8 typical		pF
Closed loop output impedance	z_o	f = 25 kHz, A_V = 10	25°C	03,04	200 typical		Ω
Common mode rejection ratio	CMRR	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	03,04	70		dB
			-40°C to +125°C		70		
Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	k_{SVR}	V_{DD} = 4.4 V to 16 V, no load, V_{IC} = V_{DD} / 2	25°C	03,04	80		dB
			-40°C to +125°C		80		
Supply current (four amplifiers)	I_{DD}	V_O = 2.5 V, no load	25°C	03,04		250	μA
			-40°C to +125°C			300	
Slew rate at unity gain	SR	V_O = 0.5 V to 3.5 V, R_L = 100 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	03,04	0.07		V / μs
			-40°C to +125°C		0.05		
Equivalent input noise voltage	V_n	f = 10 Hz	25°C	03,04	36 typical		nV / $\sqrt{Hz}$
		f = 1 kHz			19 typical		
Peak to peak equivalent input noise voltage	$V_{N(PP)}$	f = 0.1 Hz to 1 Hz	25°C	03,04	0.7 typical		μV
		f = 0.1 Hz to 10 Hz			1.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{DD} = 5 V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits Min	Limits Max	Unit
Equivalent input noise current	I_n		25°C	03,04	0.6 typical		fA / $\sqrt{Hz}$
Total harmonic distortion plus noise	THD+N	A_V = 1, V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ referenced to 2.5 V	25°C	03,04	0.2 % typical		
		A_V = 10, V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ referenced to 2.5 V			1 % typical		
Gain bandwidth product	GBWP	f = 50 kHz, R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	03,04	0.2 typical		MHz
Maximum output swing bandwidth	B_{OM}	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	03,04	30 typical		kHz
Phase margin at unity gain	ϕm	R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	03,04	63° typical		
Gain margin	Gm	R_L = 50 kΩ referenced to 2.5 V, C_L = 100 pF referenced to 2.5 V	25°C	03,04	15 typical		dB

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Full range is –40°C to +125°C for Q suffix.

3/ Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions $\pm V_{DD} = \pm 5$ V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03		1500	μV
				04		850	
			-40°C to +125°C	03		1750	
				04		1000	
Temperature coefficient of input offset voltage	αVIO	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C to +125°C	03,04	0.5 typical		μV / °C
Input offset voltage long term drift 3/	DV_{IO}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03,04	0.003 typical		μV / mo
Input offset current	I_{IO}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03,04		60	pA
			+125°C			1000	
Input bias current	I_{IB}	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	03,04		60	pA
			+125°C			1000	
Common mode input voltage range	V_{ICR}	$\lvert V_{IO} \rvert \leq 5$ mV, $R_S = 50\ \Omega$	25°C	03,04	-5 to 4		V
			-40°C to +125°C		-5 to 3.5		
Maximum positive peak output voltage	$+V_{OM}$	$I_O = -20\ \mu A$	25°C	03,04	4.98 typical		V
		$I_O = -100\ \mu A$	25°C		4.9		
			-40°C to +125°C		4.7		
		$I_O = -200\ \mu A$	25°C		4.8		
Maximum negative peak output voltage	$-V_{OM}$	$V_{IC} = 0$ V, $I_O = 50\ \mu A$	25°C	03,04	-4.99 typical		V
		$V_{IC} = 0$ V, $I_O = 500\ \mu A$	25°C		-4.85		
			-40°C to +125°C		-4.85		
		$V_{IC} = 0$ V, $I_O = 4$ mA	25°C		-4		
			-40°C to +125°C		-3.8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions $\pm V_{DD} = \pm 5$ V, unless otherwise specified	Temperature, 2/ T_A	Device type	Limits Min	Limits Max	Unit
Large signal differential voltage amplification	A_{VD}	$V_O = \pm 4$ V, $R_L = 100$ kΩ	25°C	03,04	40		V / mV
			-40°C to +125°C		10		
		$V_O = \pm 4$ V, $R_L = 1$ MΩ	25°C		3000 typical		
Differential input resistance	$r_{i(d)}$		25°C	03,04	10^{12} typical		Ω
Common mode input resistance	$r_{i(c)}$		25°C	03,04	10^{12} typical		Ω
Common mode input capacitance	$c_{i(c)}$	f = 10 kHz, Y package	25°C	03,04	8 typical		pF
Closed loop output impedance	z_o	f = 25 kHz, $A_V = 10$	25°C	03,04	190 typical		Ω
Common mode rejection ratio	CMRR	V_{IC} = -5 V to 2.7 V, $V_O = 0$ V, $R_S = 50$ Ω	25°C	03,04	75		dB
			-40°C to +125°C		75		
Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	k_{SVR}	$\pm V_{DD} = \pm 2.2$ V to ± 8 V, no load, $V_{IC} = V_{DD} / 2$	25°C	03,04	80		dB
			-40°C to +125°C		80		
Supply current (four amplifiers)	I_{DD}	$V_O = 0$ V, no load	25°C	03,04		250	µA
			-40°C to +125°C			300	
Slew rate at unity gain	SR	$V_O = \pm 2$ V, $R_L = 100$ kΩ, $C_L = 100$ pF	25°C	03,04	0.07		V / µs
			-40°C to +125°C		0.05		
Equivalent input noise voltage	V_n	f = 10 Hz	25°C	03,04	38 typical		nV / $\sqrt{Hz}$
		f = 1 kHz			19 typical		
Peak to peak equivalent input noise voltage	$V_{N(PP)}$	f = 0.1 Hz to 1 Hz	25°C	03,04	0.8 typical		µV
		f = 0.1 Hz to 10 Hz			1.1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions $\pm V_{DD} = \pm 5$ V, unless otherwise specified	Temperature, T_A 2/	Device type	Limits Min	Limits Max	Unit
Equivalent input noise current	I_n		25°C	03,04	0.6 typical		fA / $\sqrt{Hz}$
Total harmonic distortion plus noise	THD+N	$A_V = 1$, $V_O = \pm 2.3$ V, f = 20 kHz, $R_L = 50$ kΩ	25°C	03,04	0.2 % typical		
		$A_V = 10$, $V_O = \pm 2.3$ V, f = 20 kHz, $R_L = 50$ kΩ			1 % typical		
Gain bandwidth product	GBWP	f = 10 kHz, $R_L = 50$ kΩ, $C_L = 100$ pF	25°C	03,04	0.21 typical		MHz
Maximum output swing bandwidth	B_{OM}	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 50$ kΩ, $C_L = 100$ pF	25°C	03,04	14 typical		kHz
Phase margin at unity gain	ϕm	$R_L = 50$ kΩ, $C_L = 100$ pF	25°C	03,04	63° typical		
Gain margin	Gm	$R_L = 50$ kΩ, $C_L = 100$ pF	25°C	03,04	15 typical		dB

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Full range is –40°C to +125°C for Q suffix.

3/ Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

Case X

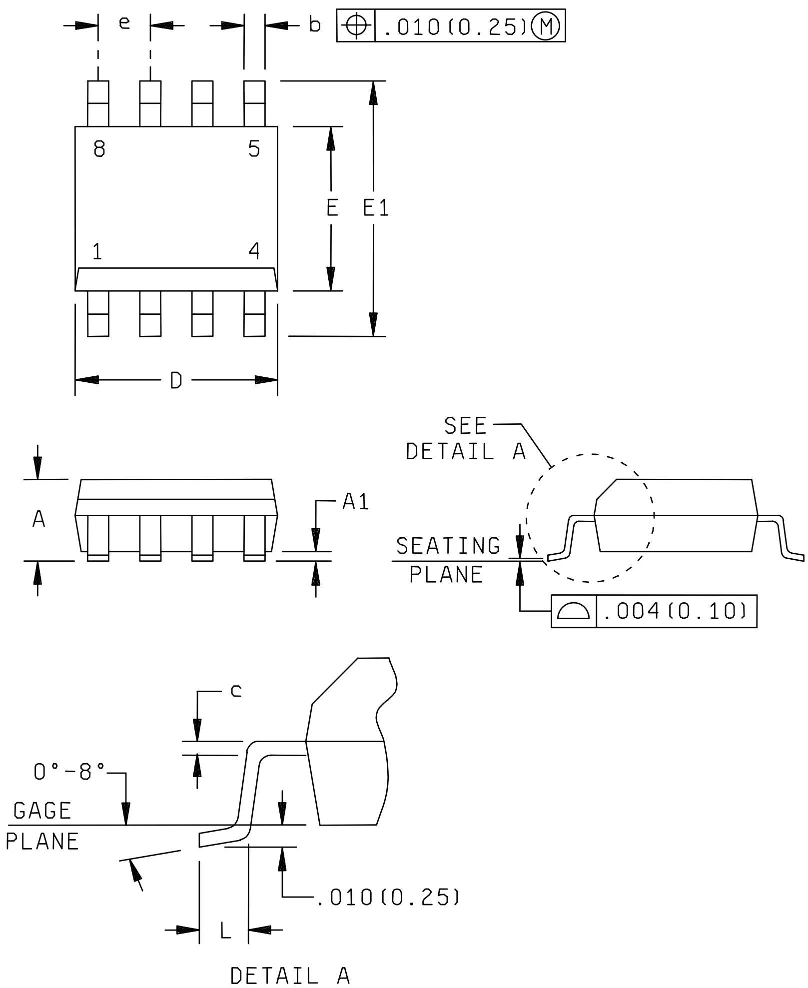

FIGURE 1. Case outlines.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE **A**	CODE IDENT NO. **16236**	DWG NO. **V62/04682**
		REV A	PAGE 17

Case X - Continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.069	---	1.75
A1	.004	.010	0.10	0.25
b	.012	.020	0.31	0.51
c	.005	.010	0.13	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.81	4.00
E1	.228	.244	5.80	6.20
e	.050 BSC		1.27 BSC	
L	.016	.050	0.40	1.27

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Fall within JEDEC MS-012 variation AA.

FIGURE 1. Case outlines - Continued.

Case Y

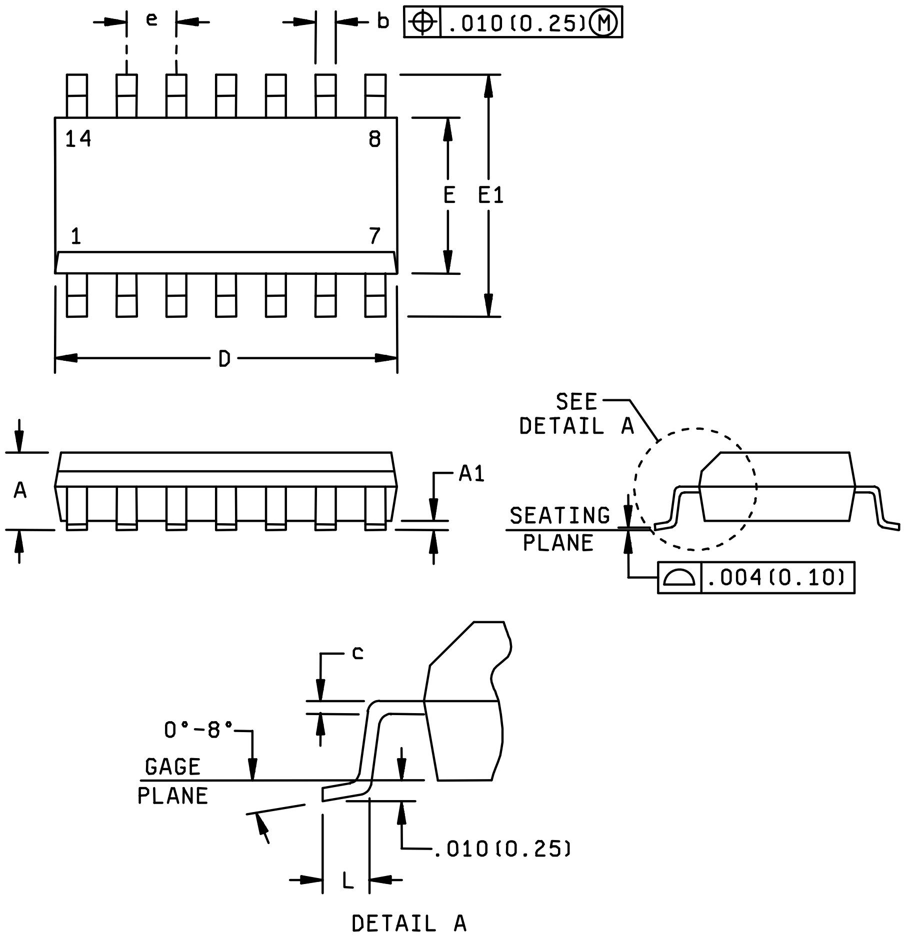

FIGURE 1. Case outlines – Continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.069	---	1.75
A1	.004	.010	0.10	0.25
b	.012	.020	0.31	0.51
c	.005	.010	0.13	0.25
D	.337	.344	8.55	8.75
E	.150	.157	3.80	4.00
E1	.228	.244	5.80	6.20
e	.050 BSC		1.27 BSC	
L	.016	.050	0.40	1.27

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Fall within JEDEC MS-012 variation AB

FIGURE 1. Case outlines - Continued.

Device types	01 and 02	03 and 04
Case outlines	X	Y
Terminal number	Terminal symbol	
1	OUT1	OUT1
2	-IN1	-IN1
3	+IN1	+IN1
4	$-V_{DD}$ / GND	$+V_{DD}$
5	+IN2	+IN2
6	-IN2	-IN2
7	OUT2	OUT2
8	$+V_{DD}$	OUT3
9	---	-IN3
10	---	+IN3
11	---	$-V_{DD}$ / GND
12	---	+IN4
13	---	-IN4
14	---	OUT4

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	V_{IO} max at 25°C	Device manufacturer CAGE code	Package 2/		Vendor part number	Top side marking
V62/04682-01XE	1550 μV	01295	SOIC (D)	Tape and reel	TLC2252QDREP	2252EP
V62/04682-02XE	850 μV	01295	SOIC (D)	Tape and reel	TLC2252AQDREP	2252AE
V62/04682-03YE	1550 μV	01295	SOIC (D)	Tape and reel	TLC2254QDREP	TLC2254EP
V62/04682-04YE	850 μV	01295	SOIC (D)	Tape and reel	TLC2254AQDREP	TLC2254AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493