REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-06-22	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-03-21	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B										
	PAGE		1	2	3	4	5	6	7	8	9	10										

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY-MM-DD 04-03-11	**CHECKED BY** Charles F. Saffle **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/04676**
	REV B	**PAGE** 1 **OF** 10

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT octal edge-triggered D-type flip-flop with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04676	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVTH374-EP	3.3-V ABT octal edge-triggered D-type flip-flop with 3-state outputs

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 4.6 V
Input voltage range (V_I) ..... -0.5 V to 7 V 2/
Voltage range applied to any output
in the high-impedance or power-off state (V_O) ..... -0.5 V to 7 V 2/
Voltage range applied to any output
in the high state (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/
Current into any output in the low state (I_O) ..... 128 mA
Current into any output in the high state (I_O) ..... 64 mA 3/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Package thermal impedance (θ_{JA}) ..... 83°C/W 4/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 5/ 6/

Supply voltage range (V_{CC}) ..... 2.7 V to 3.6 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Maximum input voltage (V_I) ..... 5.5 V
Maximum high level output current (I_{OH}) ..... -32 mA
Maximum low level output current (I_{OL}) ..... 64 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$) ..... 10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$) ..... 200 µs/V
Operating free-air temperature range (T_A) ..... -40°C to +85°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-40°C \le T_A \le 85°C$ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
Input clamp voltage	V_{IK}	I_I = -18 mA	2.7 V		-1.2	V
High level output voltage	V_{OH}	I_{OH} = -100 μA	2.7 V to 3.6 V	V_{CC} – 0.2		
		I_{OH} = -8 mA	2.7 V	2.4		
		I_{OH} = -32 mA	3.0 V	2.0		
Low level output voltage	V_{OL}	I_{OL} = 100 μA	2.7 V		0.2	
		I_{OL} = 24 mA			0.5	
		I_{OL} = 16 mA	3.0 V		0.4	
		I_{OL} = 32 mA			0.5	
		I_{OL} = 64 mA			0.55	
Input current	I_I	V_I = 5.5 V	0 V or 3.6 V		10	μA
		Control inputs, $V_I = V_{CC}$ or GND	3.6 V		±1	
		Data inputs, $V_I = V_{CC}$			1	
		Data inputs, V_I = 0 V			-5	
Input/output power-off leakage current	I_{off}	V_I or V_O = 0 to 4.5 V	0 V		±100	μA
Input current (hold)	$I_{I(hold)}$	Data inputs, V_I = 0.8 V	3 V	75		μA
		Data inputs, V_I = 2 V		-75		
		Data inputs, V_I = 0 V to 3.6 V	3.6 V 2/		+500 -750	
3-state output current high	I_{OZH}	V_O = 3 V	3.6 V		5	μA
3-state output current low	I_{OZL}	V_O = 0.5 V	3.6 V		-5	μA
3-state output current power-up	I_{OZPU}	V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care	0 V to 1.5 V		±100	μA
3-state output current power-down	I_{OZPD}	V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care	1.5 V to 0 V		±100	μA
Quiescent supply current	I_{CC}	Outputs high $V_I = V_{CC}$ or GND, I_O = 0 A	3.6 V		0.19	mA
		Outputs low. $V_I = V_{CC}$ or GND, I_O = 0 A			5	
		Outputs disabled. $V_I = V_{CC}$ or GND, I_O = 0 A			0.19	
Quiescent supply current delta	ΔI_{CC} 3/	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		0.2	mA
Input capacitance	C_i	V_I = 3 V or 0 V, T_A = 25°C	3.3 V	3 TYP		pF
Output capacitance	C_o	V_O = 3 V or 0 V, T_A = 25°C		7 TYP		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

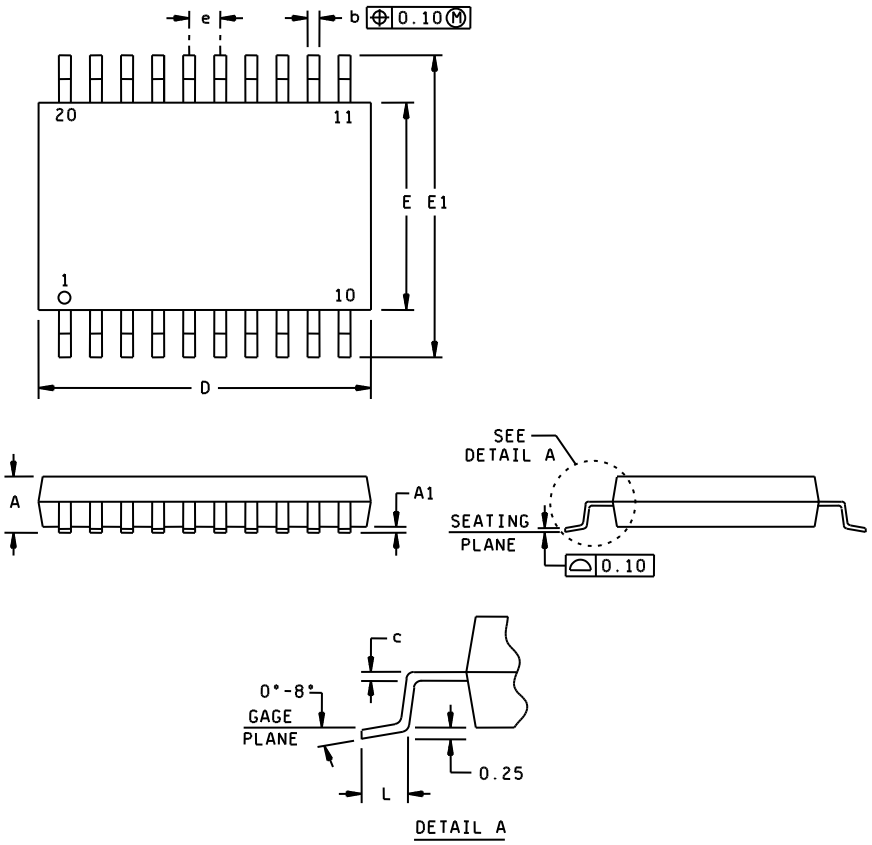
Test	Symbol	Conditions $-40°C \le T_A \le 85°C$ unless otherwise specified	V_{CC}	Limits Min	Limits Max	Unit
Clock frequency	f_{clock}		2.7 V		150	MHz
			3.3 V ±0.3 V		150	
Pulse duration, CLK high or low	t_w		2.7 V	3.3		ns
			3.3 V ±0.3 V	3.3		
Setup time, data before CLK↑	t_{su}		2.7 V	2		
			3.3 V ±0.3 V	1.5		
Hold time, data after CLK↑	t_h		2.7 V	0		
			3.3 V ±0.3 V	0.8		
Maximum clock frequency	f_{max}	See figure 5	2.7 V	150		MHz
			3.3 V ±0.3 V	150		
Propagation delay time, CLK to Q	t_{PLH}	C_L = 50 pF See figure 5.	2.7 V		5	ns
			3.3 V ±0.3 V	1.8	4.5	
	t_{PHL}		2.7 V		4.3	
			3.3 V ±0.3 V	1.8	4.2	
Propagation delay time, output enable, $\overline{OE}$ to Q	t_{PZH}		2.7 V		5.6	
			3.3 V ±0.3 V	1.3	4.7	
	t_{PZL}		2.7 V		5.2	
			3.3 V ±0.3 V	1.6	4.7	
Propagation delay time, output disable, $\overline{OE}$ to Q	t_{PHZ}		2.7 V		4.9	
			3.3 V ±0.3 V	1.9	4.6	
	t_{PLZ}		2.7 V		4.6	
			3.3 V ±0.3 V	2	4.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

3/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 BSC		0.026 BSC	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	6.40	6.60	0.252	0.260					

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline.

(each flip flop)

Inputs			Output
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Immaterial
Z = High-impedance state
Q_0 = Level of Q before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

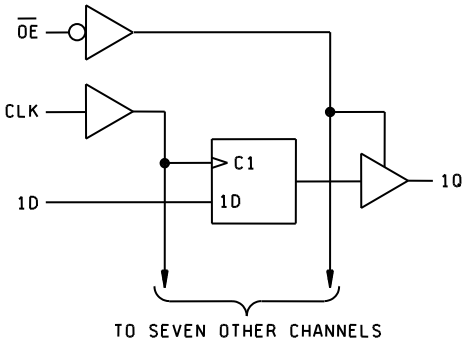
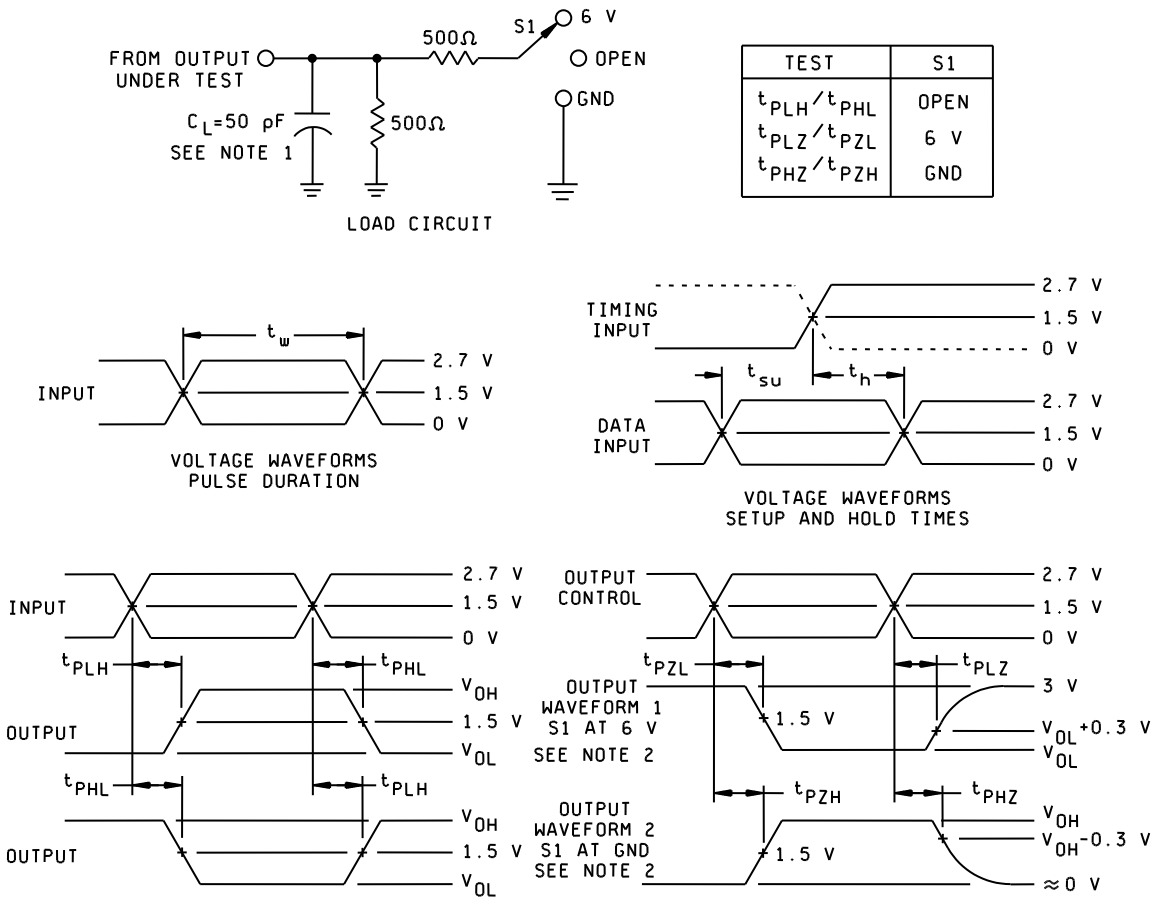


FIGURE 3. Logic diagram.

Device type 01			
Case outlines: X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{OE}$	11	CLK
2	1Q	12	5Q
3	1D	13	5D
4	2D	14	6D
5	2Q	15	6Q
6	3Q	16	7Q
7	3D	17	7D
8	4D	18	8D
9	4Q	19	8Q
10	GND	20	V_{CC}

FIGURE 4. Terminal connections.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, and t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04676-01XE	01295	SN74LVTH374IPWREP	LH374EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493