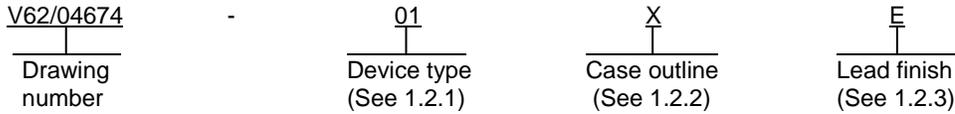




1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V ABT octal D-type flip-flop with clear microcircuit, with an operating temperature range of -40°C to +85°C and extended temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01 <u>1/</u>	SN74LVTH273-EP	3.3-V ABT octal D-type flip-flop with clear
02 <u>2/</u>	SN74LVTH273-EP	3.3-V ABT octal D-type flip-flop with clear

1.2.2 Case outline. The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MO-153	Plastic small-outline
Y	20		Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Operate at -40°C to +85°C.  
2/ Operate at -55°C to +125°C.

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1.3 Absolute maximum ratings. 3/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to 4.6 V
Input voltage range ( $V_I$ ) .....	-0.5 V to 7 V 4/
Voltage range applied to any output in the power-off state ( $V_O$ ) .....	-0.5 V to 7 V 4/
Voltage range applied to any output in the high state ( $V_O$ ) .....	-0.5 V to $V_{CC} + 0.5 V$ 4/
Current into any output in the low state ( $I_O$ ) .....	128 mA
Current into any output in the high state ( $I_O$ ) .....	64 mA 5/
Input clamp current ( $I_{IK}$ ) ( $V_I < 0$ ) .....	-50 mA
Output clamp current ( $I_{OK}$ ) ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance ( $\theta_{JA}$ ):	
Case X .....	83°C/W 6/
Case Y .....	94.4°C/W 6/
Storage temperature range ( $T_{STG}$ ) .....	-65°C to 150°C

1.4 Recommended operating conditions. 7/

Supply voltage range ( $V_{CC}$ ) .....	2.7 V to 3.6 V
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V
Maximum low level input voltage ( $V_{IL}$ ) .....	0.8 V
Maximum input voltage ( $V_I$ ) .....	5.5 V
Maximum high level output current ( $I_{OH}$ ) .....	-32 mA
Maximum low level output current ( $I_{OL}$ ) .....	64 mA
Maximum input transition rise or fall rate ( $\Delta t/\Delta v$ ) .....	10 ns/V
Operating free-air temperature range ( $T_A$ ):	
Case X .....	-40°C to +85°C
Case Y .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

- 3/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 4/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 5/ This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- 6/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 7/ All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

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### 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions -40°C ≤ T <sub>A</sub> ≤ 85°C <u>2/</u> -55°C ≤ T <sub>A</sub> ≤ 125°C <u>3/</u>		V <sub>CC</sub>	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V <sub>IK</sub>	I <sub>I</sub> = -18 mA		2.7 V	All		-1.2	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA		2.7 V to 3.6 V		V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -8 mA		2.7 V		2.4		
		I <sub>OH</sub> = -32 mA		3.0 V		2		
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		2.7 V			0.2	V
		I <sub>OL</sub> = 24 mA					0.5	
		I <sub>OL</sub> = 16 mA		3.0 V		0.4		
		I <sub>OL</sub> = 32 mA				0.5		
		I <sub>OL</sub> = 64 mA				0.55		
Input current	I <sub>I</sub>	V <sub>I</sub> = 5.5 V		0 V or 3.6 V		10	μA	
		Control inputs.	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		±1		
		Data inputs.	V <sub>I</sub> = V <sub>CC</sub>			1		
			V <sub>I</sub> = 0 V			-5		
Input/output power-off leakage current	I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V		0 V		±100	μA	
Input current (hold)	I <sub>I(hold)</sub>	Data inputs.	V <sub>I</sub> = 0.8 V	3 V	75	μA		
			V <sub>I</sub> = 2 V		-75			
			V <sub>I</sub> = 0 V to 3.6 V	3.6 V <u>4/</u>	+500 -750			
Quiescent supply current	I <sub>CC</sub>	Outputs high.	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0 A	3.6 V		0.19	mA	
		Outputs low.	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0 A			5		

See footnotes at end of table.

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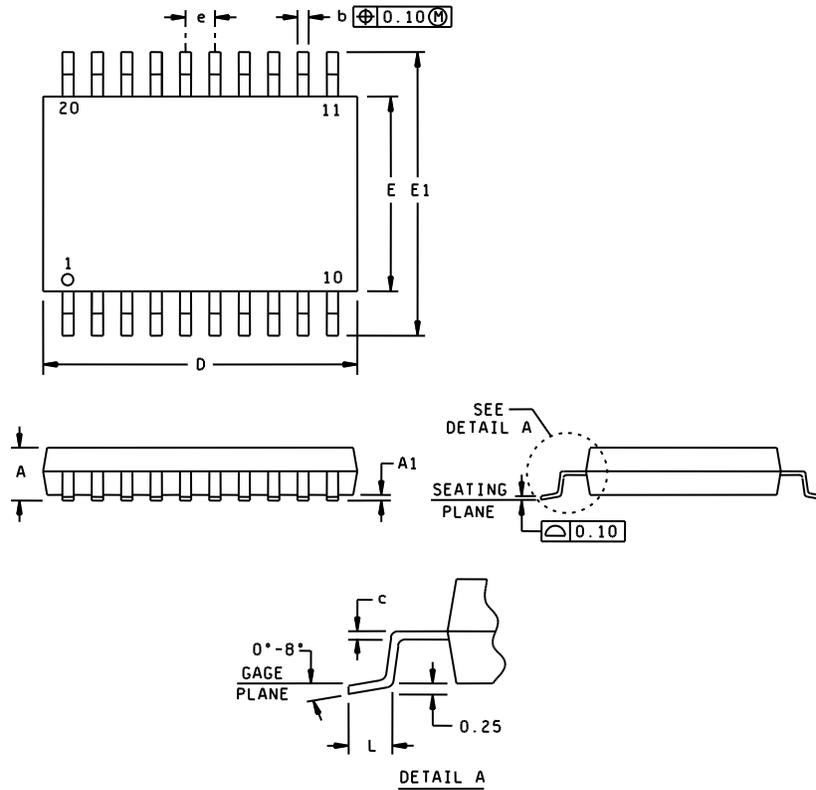
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -40°C ≤ T <sub>A</sub> ≤ 85°C <u>2/</u> -55°C ≤ T <sub>A</sub> ≤ 125°C <u>3/</u>	V <sub>CC</sub>	Device type	Limits		Unit
					Min	Max	
Quiescent supply current delta	ΔI <sub>CC</sub> <u>5/</u>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	All		0.2	mA
Input capacitance	C <sub>i</sub>	V <sub>I</sub> = 3 V or 0 V, T <sub>A</sub> = 25°C	3.3 V		4 TYP		pF
Clock frequency	f <sub>clock</sub>		3.3 V ±0.3 V			150	MHz
Pulse duration	t <sub>w</sub>	See figure 5.	2.7 V		3.3		ns
			3.3 V ±0.3 V		3.3		
Setup time	t <sub>su</sub>	Data high or low before CLK↑ See figure 5.	2.7 V		2.7		ns
			3.3 V ±0.3 V		2.3		
		CLR high before CLK↑ See figure 5.	2.7 V	2.7			
			3.3 V ±0.3 V	2.3			
Hold time	t <sub>h</sub>	Data high or low after CLK↑ See figure 5.	2.7 V	0		ns	
			3.3 V ±0.3 V	0			
Maximum clock frequency	f <sub>max</sub>		3.3 V ±0.3 V	150		MHz	
Propagation delay time, CLK to any Q	t <sub>PLH</sub>	C <sub>L</sub> = 50 pF See figure 5.	2.7 V	1	5.5	ns	
				2	7.0		
			3.3 V ±0.3 V	All	1.7		4.9
	t <sub>PHL</sub>		2.7 V	1	5.1		
				2	6.6		
			3.3 V ±0.3 V	All	1.9		4.8
Propagation delay time, CLR to any Q	t <sub>PHL</sub>	2.7 V	1	4.7	ns		
			2	7.0			
		3.3 V ±0.3 V	All	1.6		4.3	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ For device type 01.
- 3/ For device type 02.
- 4/ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
- 5/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

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Case X



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 BSC		0.026 BSC	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	6.40	6.60	0.252	0.260					

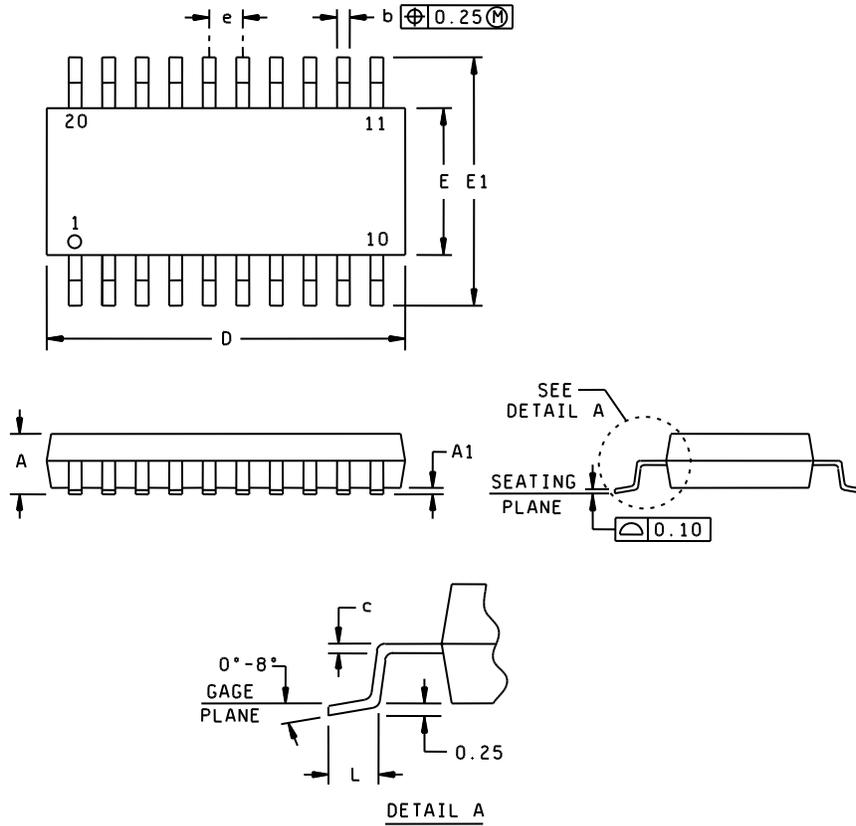
NOTES:

1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline.

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Case Y



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		2.00		.078	E	5.00	5.60	.195	.219
A1	0.05	0.15	.002	.006	E1	7.40	8.20	.289	.320
b	0.35	0.51	.014	.020	e	1.27 BSC		.050 BSC	
c	0.15 NOM		.006 NOM		L	0.55	1.05	.021	.041
D	12.30	12.90	.480	.504					

NOTES:

1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).

FIGURE 1. Case outline - Continued.

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(each flip-flop)

Inputs			Outputs
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q <sub>0</sub>

H = High voltage level

L = Low voltage level

X = Immaterial

↑ = Transition from low to high level.

Q<sub>0</sub> = Level of Q before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

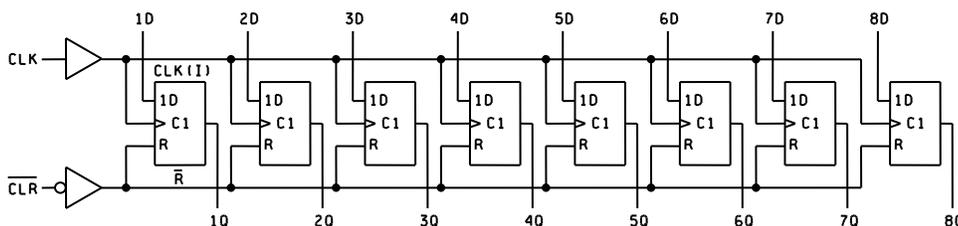
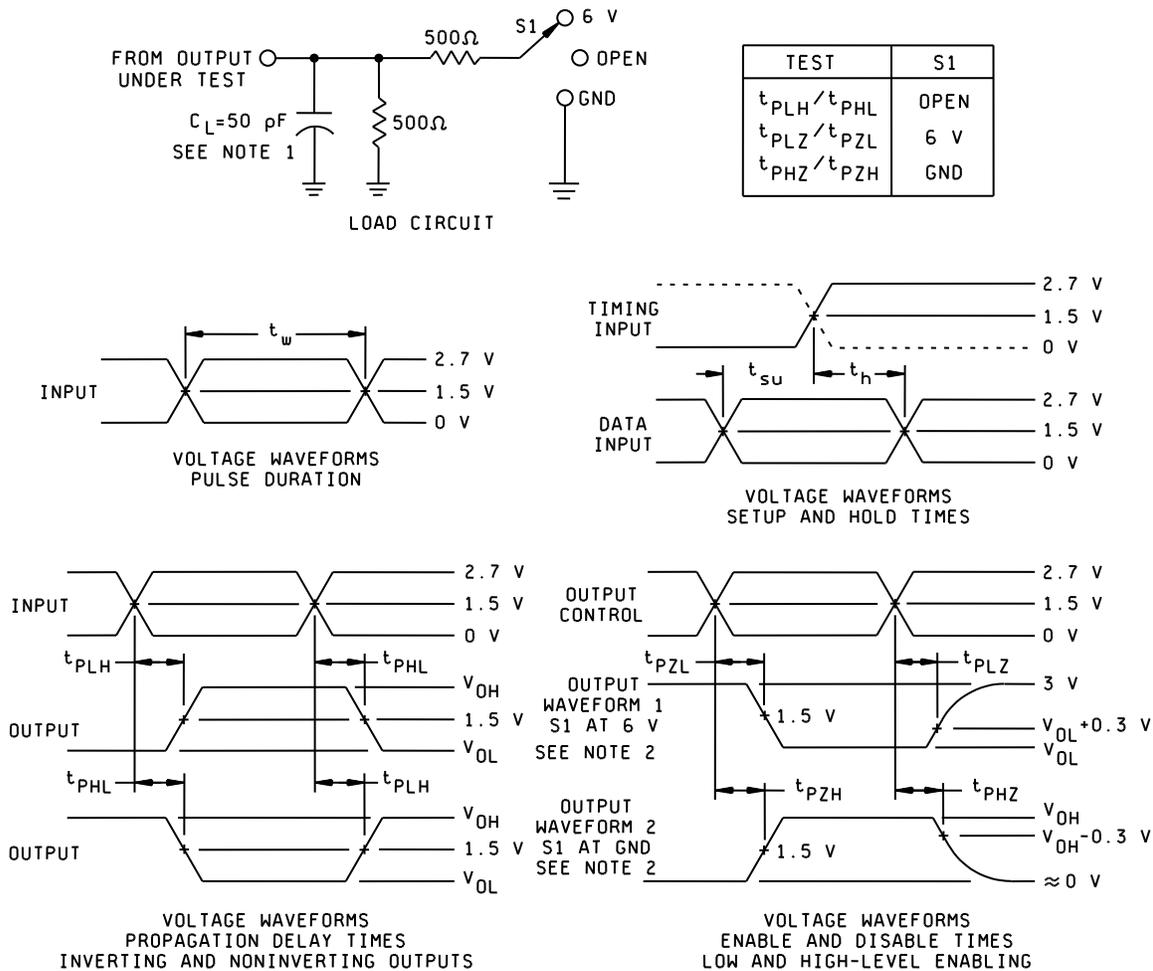


FIGURE 3. Logic diagram.

Case outline X and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{\text{CLR}}$	11	CLK
2	1Q	12	5Q
3	1D	13	5D
4	2D	14	6D
5	2Q	15	6Q
6	3Q	16	7Q
7	3D	17	7D
8	4D	18	8D
9	4Q	19	8Q
10	GND	20	V <sub>CC</sub>

FIGURE 4. Terminal connections.

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NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04674-01XE	<u>2/</u>	SN74LVTH273IPWREP	LH273EP
V62/04674-02YE	01295	SN74LVTH273MNSREP	LVTH273EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Not available from an approved source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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