REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-05-25	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-02-24	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	22-10-21	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C												
SHEET	1	2	3	4	5	6	7	8	9	10												

PMIC N/A

Original date of drawing

YY MM DD

04-03-18

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https://www.dla.mil/LandandMaritime

TITLE
MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/04668
REV C		PAGE 1 OF 10

AMSC N/A

5962-V119-22

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal edge-triggered D-type flip-flop with 3-state outputs microcircuit, with an operating temperature range of -40ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04668	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC574A-EP	Octal edge-triggered D-type flip-flop with 3-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MS-013	Plastic small-outline
Y	20	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_I)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_O)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state (V_O)	-0.5 V to V_{CC} + 0.5 V 2/ 3/
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Continuous output current (I_O)	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance (θ_{JA}): 4/	
X package	58°C/W
Y package	83°C/W
Storage temperature range (T_{STG})	-65°C to 150°C 5/

1.4 Recommended operating conditions. 6/ 7/

Supply voltage range (V_{CC}):	
Operating	2.0 V to 3.6 V
Data retention only	1.5 V minimum
Minimum high level input voltage (V_{IH}) (V_{CC} = 2.7 V to 3.6 V)	2.0 V
Maximum low level input voltage (V_{IL}) (V_{CC} = 2.7 V to 3.6 V)	0.8 V
Input voltage range (V_I)	0.0 V to 5.5 V
Output voltage range (V_O):	
High or low state	0.0 V to V_{CC}
3-state	0.0 V to 5.5 V
Maximum high level output current (I_{OH}):	
V_{CC} = 2.7 V	-12 mA
V_{CC} = 3.0 V	-24 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 2.7 V	12 mA
V_{CC} = 3.0 V	24 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$)	6 ns/V
Operating free-air temperature range (T_A)	-40°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The value of V_{CC} is provided in the recommended operating conditions table.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
6/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
7/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	-	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	-	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https:/www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

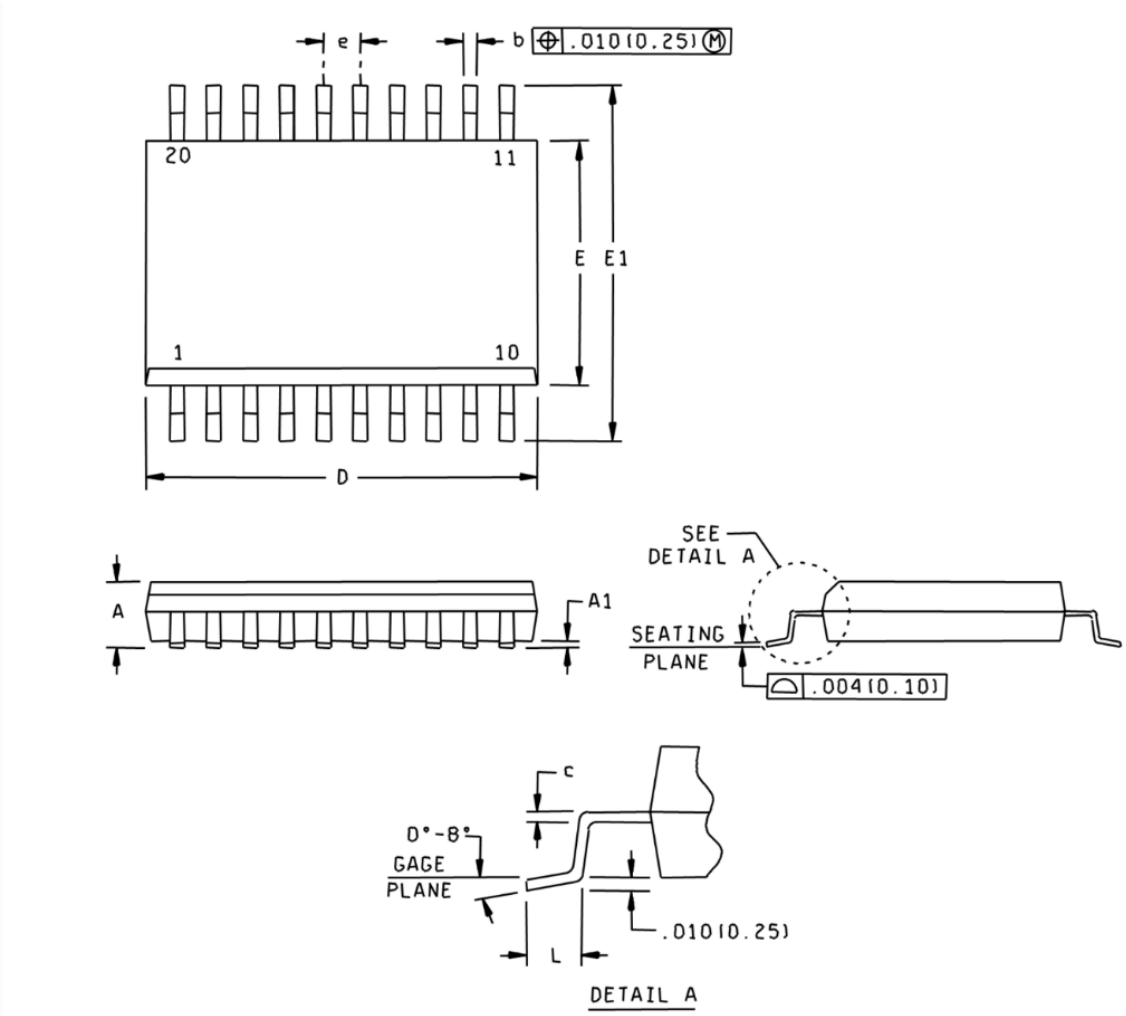
TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature T_A	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -100 μA	2.7 V to 3.6 V	25°C, -40°C to 125°C	V_{CC} – 0.2		V
		I_{OH} = -12 mA	2.7 V		2.2		
			3.0 V		2.4		
		I_{OH} = -24 mA	3.0 V		2.2		
Low level output voltage	V_{OL}	I_{OL} = 100 μA	2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA	2.7 V			0.4	
		I_{OL} = 24 mA	3.0 V			0.55	
Input current	I_I	V_I = 0 to 5.5 V	3.6 V			±5	μA
Three-state output leakage current	I_{OZ}	V_O = 0 to 5.5 V	3.6 V			±15	μA
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND, I_O = 0 A	3.6 V			10	μA
		3.6 V ≤ V_I ≤ 5.5 V 2/ I_O = 0 A				10	
Quiescent supply current delta	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
Input capacitance	C_i	V_I = V_{CC} or GND	3.3 V	25°C	4	TYP	pF
Output capacitance	C_O	V_O = V_{CC} or GND	3.3 V		5.5	TYP	pF
Power dissipation capacitance per latch	C_{pd}	Outputs enabled	2.5 V		60	TYP	pF
		f = 10 MHz	3.3 V		43	TYP	
		Outputs disabled	2.5 V		9	TYP	
		f = 10 MHz	3.3 V		15	TYP	
Maximum clock frequency	f_{max}	See figure 5	2.7 V	25°C, -40°C to 125°C	150		MHz
			3.3 V ±0.3 V		150		
Propagation delay time, CLK to Q	t_{pd}		2.7 V			8	ns
			3.3 V ±0.3 V		1	7	
Propagation delay time, output enable, $\overline{OE}$ to Q	t_{en}		2.7 V			9	
			3.3 V ±0.3 V		1	7.5	
Propagation delay time, output disable, $\overline{OE}$ to Q	t_{dis}		2.7 V			7	
			3.3 V ±0.3 V		0.5	6.4	
Clock frequency	f_{clock}		2.7 V			150	MHz
			3.3 V ±0.3 V			150	
Pulse duration, CLK high or low	t_w		2.7 V		3.3		ns
			3.3 V ±0.3 V		3.3		
Setup time, data before CLK↑	t_{su}		2.7 V		2		
			3.3 V ±0.3 V		2		
Hold time, data after CLK↑	t_h		2.7 V		2		
			3.3 V ±0.3 V		2		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This applies in the disabled state only.

Case X

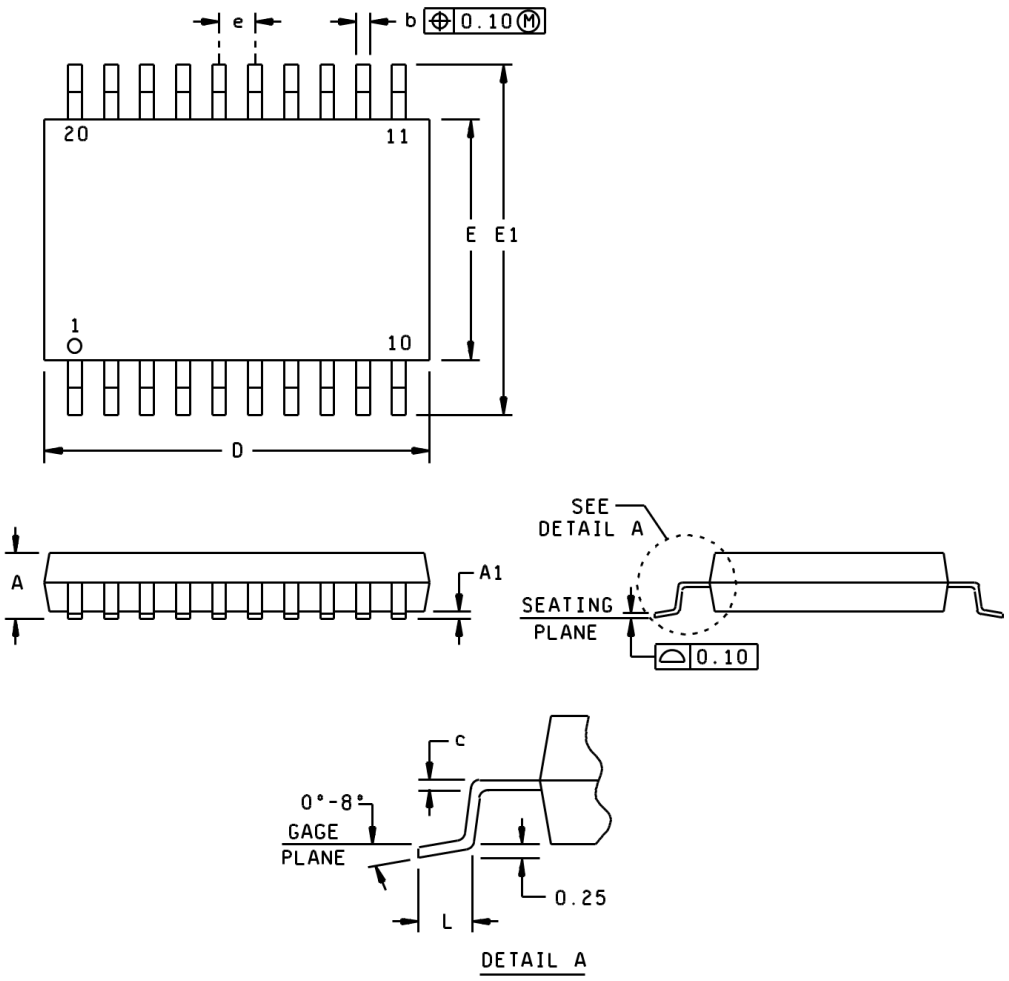


Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	.069	---	1.75	E	.150	.157	3.81	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.014	.020	0.35	0.51	e	.050 BSC		1.27 BSC	
c	.008 NOM		0.20 NOM		L	0.016	0.044	0.40	1.12
D	0.500	0.510	12.70	12.95					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 inches (0.15 mm).
4. Falls within JEDEC MS-013.

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 BSC		0.026 BSC	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	6.40	6.60	0.252	0.260					

NOTES:
1. All linear dimensions are in millimeters.
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline - Continued.

(each flip-flop)

Inputs			Output
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Immaterial
Z = High-impedance state
↑ = Transition from low to high level.
Q_0 = Level of Q before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

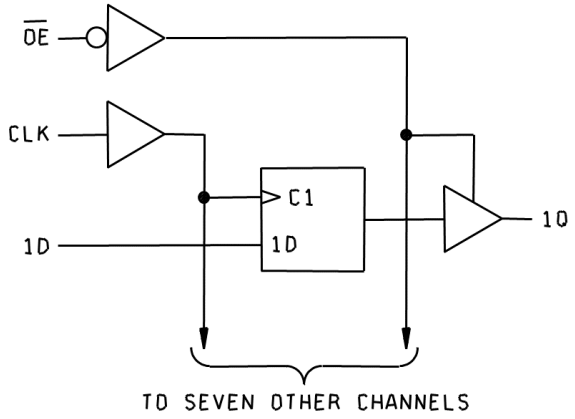
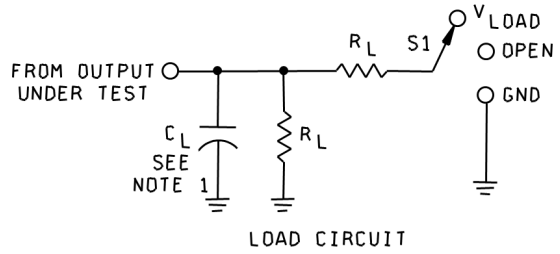


FIGURE 3. Logic diagram.

Device type 01
Case outlines: X and Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{OE}$	11	CLK
2	1D	12	8Q
3	2D	13	7Q
4	3D	14	6Q
5	4D	15	5Q
6	5D	16	4Q
7	6D	17	3Q
8	7D	18	2Q
9	8D	19	1Q
10	GND	20	V_{CC}

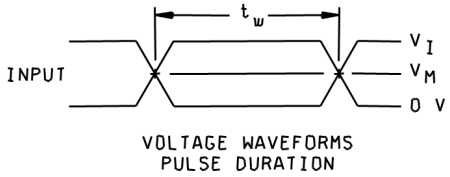
FIGURE 4. Terminal connections.



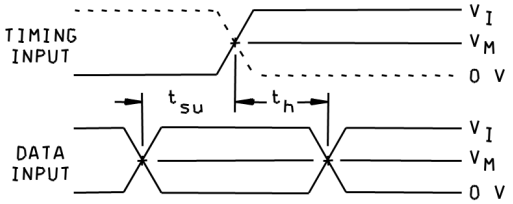
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

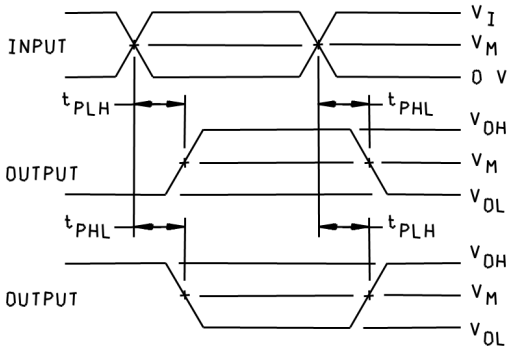
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
3.3 V ±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V

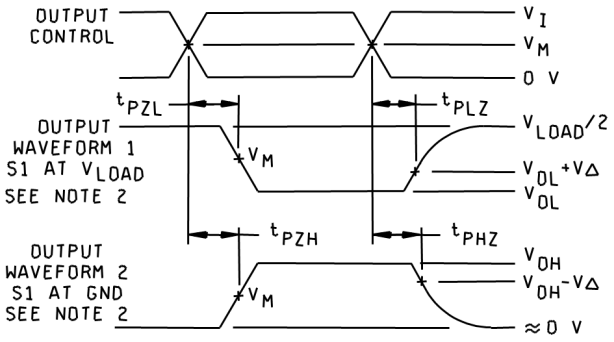


VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES





NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04668-01XE	2/	SN74LVC574AQDWREP	C574AEP
V62/04668-01YE	01295	SN74LVC574AQPWREP	C574AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not available from an approved source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243