REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-04-19	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-01-25	Muhammad Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B									
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PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY-MM-DD 04-03-11	**CHECKED BY** Charles F. Saffle **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/04664**
	REV B	**PAGE** 1 **OF** 11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal bus transceiver and 3.3-V to 5-V shifter with 3-state outputs microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04664	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC4245A-EP	Octal bus transceiver and 3.3-V to 5-V shifter with 3-state outputs

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium

1.3 Absolute maximum ratings. 1/

For V_{CCA} = 4.5 V to 5.5 V:

Supply voltage range (V_{CCA}) ..... -0.5 V to 6.5 V
Input voltage range (V_I):
A port ..... -0.5 V to V_{CCA} +0.5 V 2/
Control inputs ..... -0.5 V to 6 V
Output voltage range (V_O) (A port) ..... -0.5 V to V_{CCA} +0.5 V 2/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Continuous output current (I_O) ..... ±50 mA
Continuous current through V_{CCA} or GND ..... ±100 mA
Package thermal impedance (θ_{JA}) ..... 88°C/W 3/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

For V_{CCB} = 2.7 V to 3.6 V:

Supply voltage range (V_{CCB}) ..... -0.5 V to 4.6 V
Input voltage range (V_I) (B port) ..... -0.5 V to V_{CCB} +0.5 V 4/
Output voltage range (V_O) (B port) ..... -0.5 V to V_{CCB} +0.5 V 4/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Continuous output current (I_O) ..... ±50 mA
Continuous current through V_{CCB} or GND ..... ±100 mA
Package thermal impedance (θ_{JA}) ..... 88°C/W 3/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 5/ 6/

For V_{CCA} = 4.5 V to 5.5 V:

Supply voltage range (V_{CCA}) ..... 4.5 V to 5.5 V
Minimum high-level input voltage (V_{IH}) ..... 2.0 V
Maximum low-level input voltage (V_{IL}) ..... 0.8 V
Input voltage range (V_I) ..... 0 V to V_{CCA}
Output voltage range (V_O) ..... 0 V to V_{CCA}
Maximum high level output current (I_{OH}) ..... -24 mA
Maximum low level output current (I_{OL}) ..... 24 mA
Operating free-air temperature range (T_A) ..... -40°C to +85°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ This value is limited to 6 V maximum.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ This value is limited to 4.6 V maximum.
5/ All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.4 Recommended operating conditions – Continued.. 5/ 6/

For V_{CCB} = 2.7 V to 3.6 V:

Supply voltage range (V_{CCB})..... 2.7 V to 3.6 V
Minimum high-level input voltage (V_{IH}) (V_{CCB} = 2.7 V to 3.6 V) ..... 2.0 V
Maximum low-level input voltage (V_{IL}) (V_{CCB} = 2.7 V to 3.6 V) ..... 0.8 V
Input voltage range (V_I)..... 0 V to V_{CCB}
Output voltage range (V_O) ..... 0 V to V_{CCB}
Maximum high level output current (I_{OH}):
V_{CCB} = 2.7 V ..... -12 mA
V_{CCB} = 3 V ..... -24 mA
Maximum low level output current (I_{OL}):
V_{CCB} = 2.7 V ..... 12 mA
V_{CCB} = 3 V ..... 24 mA
Operating free-air temperature range (T_A) ..... -40°C to +85°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 - Registered and Standard Outlines for Semiconductor Devices
JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CCA} 2/	Temperature, T_A	Limits Min	Limits Max	Unit
A Port							
High level output voltage	V_{OH}	I_{OH} = -100 µA	4.5 V	25°C, -40°C to 85°C	4.3		V
			5.5 V		5.3		
		I_{OH} = -24 mA	4.5 V		3.7		
			5.5 V		4.7		
Low level output voltage	V_{OL}	I_{OL} = 100 µA	4.5 V			0.2	V
			5.5 V			0.2	
		I_{OL} = 24 mA	4.5 V			0.55	
			5.5 V			0.55	
Input current	I_I	Control inputs. $V_I = V_{CCA}$ or GND	5.5 V			±1	µA
Three-state output leakage current	I_{OZ} 3/	A port. $V_O = V_{CCA}$ or GND	5.5 V			±5	µA
Quiescent supply current	I_{CCA}	$V_I = V_{CCA}$ or GND. I_O = 0 A	5.5 V			80	µA
Quiescent supply current delta	ΔI_{CCA} 4/	One input at 3.4 V. Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
Input capacitance	C_i	Control inputs. $V_I = V_{CCA}$ or GND	Open	25°C	5 TYP		pF
Input/output capacitance	C_{io}	A port. $V_O = V_{CCA}$ or GND	5 V		11 TYP		pF
B Port							
High level output voltage	V_{OH}	I_{OH} = -100 µA	2.7 V to 3.6 V	25°C, -40°C to 85°C	V_{CC} – 0.2		V
		I_{OH} = -12 mA	2.7 V		2.2		
			3 V		2.4		
		I_{OH} = -24 mA	3 V		2		
Low level output voltage	V_{OL}	I_{OL} = 100 µA	2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA	2.7 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
Three-state output leakage current	I_{OZ} 3/	B port. $V_O = V_{CCB}$ or GND	3.6 V			±5	µA
Quiescent supply current	I_{CCB}	$V_I = V_{CCB}$ or GND. I_O = 0 A	3.6 V			50	µA
Quiescent supply current delta	ΔI_{CCB} 4/	One input at V_{CCB} – 0.6 V. Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
Input/output capacitance	C_{io}	B port. $V_O = V_{CCB}$ or GND	3.3 V	25°C	11 TYP		pF

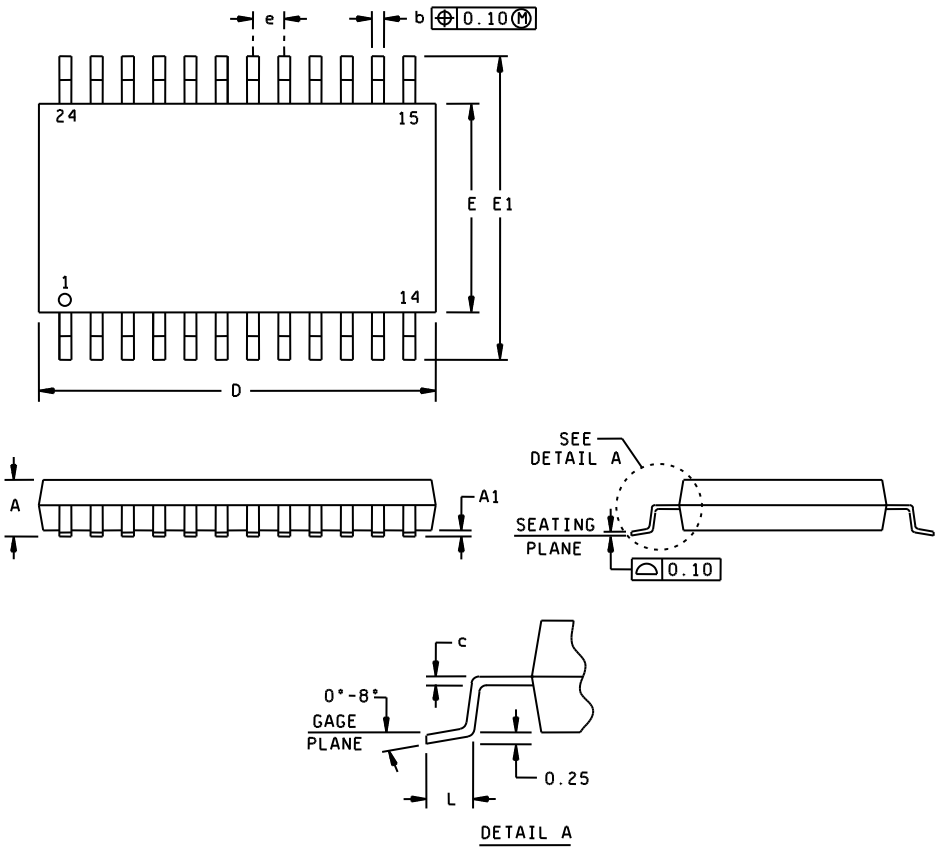
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V_{CCA} and V_{CCB}	Temperature, T_A	Limits		Unit
					Min	Max	
A and B ports							
Power dissipation capacitance per transceiver	C_{pd}	Outputs enabled. C_L = 0 f = 10 MHz	V_{CCA} = 4.5 V to 5.5 V, V_{CCB} = 2.7 V to 3.6 V	25°C	39.5 TYP		pF
		Outputs disabled. C_L = 0 f = 10 MHz			5 TYP		
Propagation delay time, A to B	t_{PHL}	C_L = 50 pF See figure 5.	V_{CCA} = 5 V ±0.5 V, V_{CCB} = 2.7 V to 3.6 V	25°C, -40°C to 85°C	1	6.3	ns
	t_{PLH}				1	6.7	
Propagation delay time, B to A	t_{PHL}				1	6.1	
	t_{PLH}				1	5	
Propagation delay time, output enable $\overline{OE}$ to A	t_{PZL}				1	9	
	t_{PZH}				1	8.1	
Propagation delay time, output enable $\overline{OE}$ to B	t_{PZL}				1	8.8	
	t_{PZH}				1	9.8	
Propagation delay time, output disable $\overline{OE}$ to A	t_{PLZ}				1	7	
	t_{PHZ}				1	5.8	
Propagation delay time, output disable $\overline{OE}$ to B	t_{PLZ}				1	7.7	
	t_{PHZ}				1	7.8	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ V_{CCB} = 2.7 V to 3.6 V.
3/ For I/O ports, the parameter I_{OZ} includes the input leakage current.
4/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.
5/ V_{CCA} = 5 V ±0.5 V.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 BSC		0.026 BSC	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	7.70	7.90	0.303	0.311					

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline.

Inputs		Operation
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage level
X = Immaterial

FIGURE 2. Truth table.

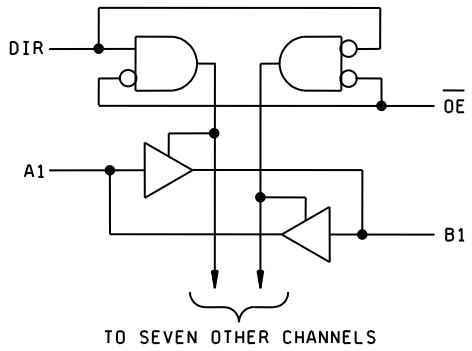
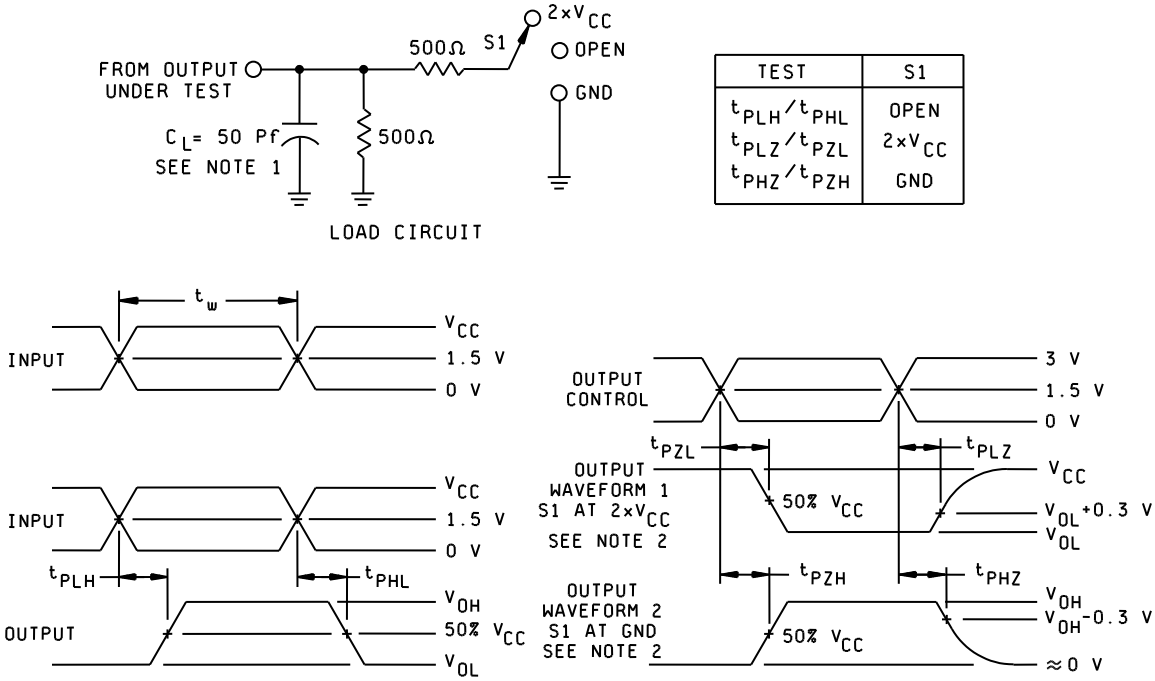


FIGURE 3. Logic diagram.

Device type 01			
Case outlines: X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	(5 V) V_{CCA}	13	GND
2	DIR	14	B8
3	A1	15	B7
4	A2	16	B6
5	A3	17	B5
6	A4	18	B4
7	A5	19	B3
8	A6	20	B2
9	A7	21	B1
10	A8	22	$\overline{OE}$
11	GND	23	V_{CCB} (3.3 V)
12	GND	24	V_{CCB} (3.3 V)

FIGURE 4. Terminal connections.

A port

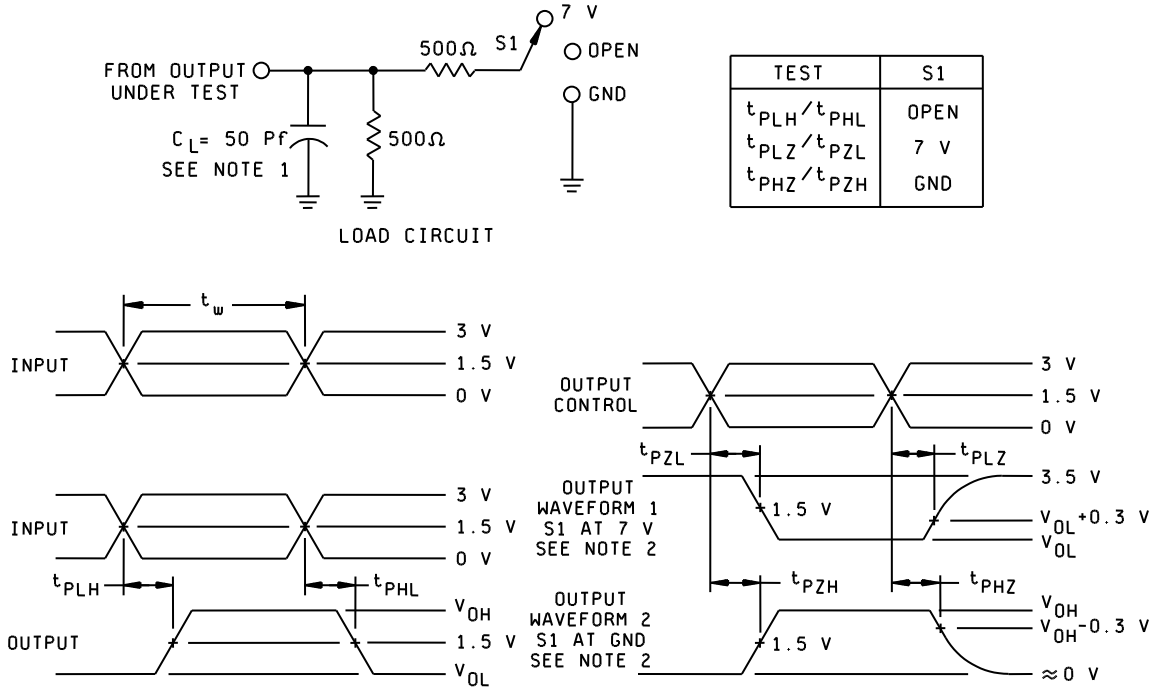


NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

B port



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 2.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04664-01XE	01295	SN74LVC4245AIPWREP	C4245AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493