REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-04-19	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-01-25	Muhammad Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B									
	PAGE			1	2	3	4	5	6	7	8	9	10									

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY-MM-DD 04-02-24	**CHECKED BY** Charles F. Saffle **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, HEX SCHMITT-TRIGGER INVERTER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/04658**
	REV B	**PAGE** 1 **OF** 10

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance hex Schmitt-trigger inverter microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04658	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC14A-EP	Hex Schmitt-trigger inverter

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	MS-012	Plastic small-outline
Y	14	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 6.5 V
Input voltage range (V_I) ..... -0.5 V to 6.5 V 2/
Output voltage range (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/ 3/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Continuous output current (I_O) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Package thermal impedance (θ_{JA}): 4/
X package ..... 86°C/W
Y package ..... 113°C/W
Storage temperature range (T_{STG}) ..... -65°C to 150°C 5/

1.4 Recommended operating conditions. 6/ 7/

Supply voltage range (V_{CC}):
Operating ..... 2.0 V to 3.6 V
Data retention only ..... 1.5 V minimum
Input voltage range (V_I) ..... 0.0 V to 5.5 V
Output voltage range (V_O) ..... 0.0 V to V_{CC}
Maximum high level output current (I_{OH}):
V_{CC} = 2.7 V ..... -12 mA
V_{CC} = 3.0 V ..... -24 mA
Maximum low level output current (I_{OL}):
V_{CC} = 2.7 V ..... 12 mA
V_{CC} = 3.0 V ..... 24 mA
Operating free-air temperature range (T_A) ..... -40°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The value of V_{CC} is provided in the recommended operating conditions table.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits
7/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	-	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	-	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

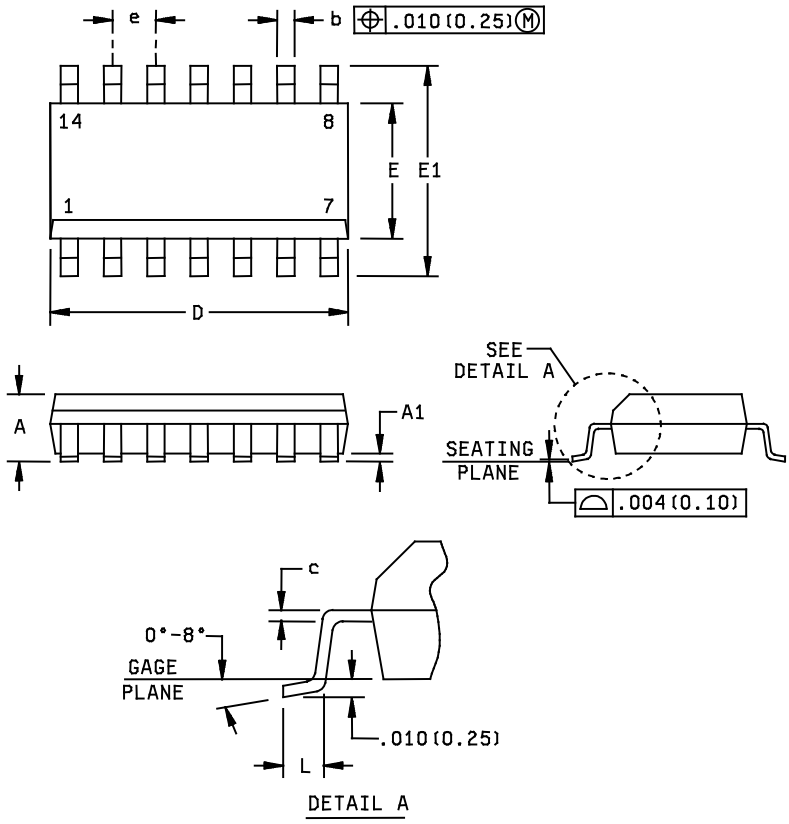
3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Limits		Units
					Min	Max	
Positive-going threshold voltage	V_{T+}		2.7 V	25°C, -40°C to 125°C	0.8	2	V
			3.0V		0.9	2	
			3.6 V		1.1	2	
Negative-going threshold voltage	V_{T-}		2.7 V		0.4	1.4	V
			3.0V		0.6	1.5	
			3.6 V		0.8	1.7	
Hysteresis voltage (V_{T+} - V_{T-})	ΔV_T		2.7 V		0.3	1.1	V
			3.0V		0.3	1.2	
			3.6 V		0.3	1.2	
High level output voltage	V_{OH}	I_{OH} = -100 μA	2.7 V to 3.6 V		V_{CC} – 0.2		V
		I_{OH} = -12 mA	2.7 V		2.2		
			3.0 V		2.4		
		I_{OH} = -24 mA	3.0 V		2.2		
Low level output voltage	V_{OL}	I_{OL} = 100 μA	2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA	2.7 V			0.4	
		I_{OL} = 24 mA	3.0 V			0.55	
Input current	I_I	V_I = 5.5 V or GND	3.6 V			±5	μA
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND I_O = 0 A	3.6 V			10	μA
Quiescent supply current delta	ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
Input capacitance	C_i	V_I = V_{CC} or GND	3.3 V	25°C	5 TYP		pF
Power dissipation capacitance per gate	C_{pd}	f = 10 MHz	2.5 V		12 TYP		
			3.3 V		15 TYP		
Propagation delay time, A to Y	t_{pd}	See figure 5.	2.7 V	25°C, -40°C to 125°C		7.5	ns
			3.3 V ±0.3 V		1	6.4	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

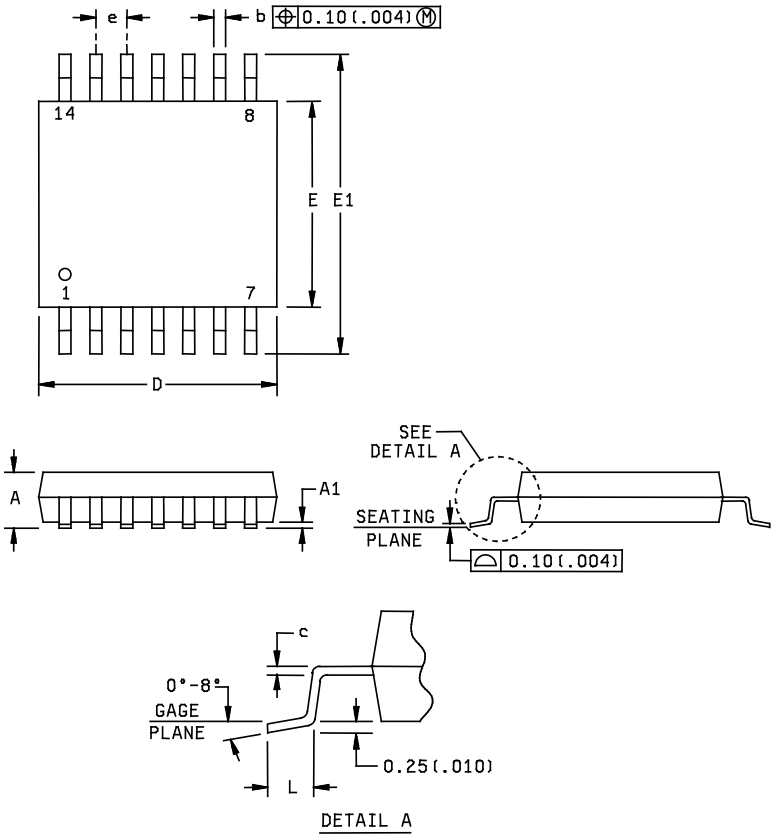


Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.069	---	1.75	E	0.150	0.157	3.81	4.00
A1	0.004	0.010	0.10	0.25	E1	0.228	0.244	5.80	6.20
b	0.014	0.020	0.35	0.51	e	0.050 BSC		1.27 BSC	
c	0.008 NOM		0.20 NOM		L	0.016	0.044	0.40	1.12
D	0.337	0.344	8.55	8.75					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 inches (0.15 mm).
4. Falls within JEDEC MS-012.

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 BSC		0.026 BSC	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	4.90	5.10	0.193	0.201					

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters (0.006 in).
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

(each inverter)

Input	Output
A	Y
H	L
L	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

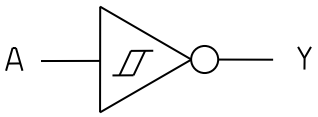
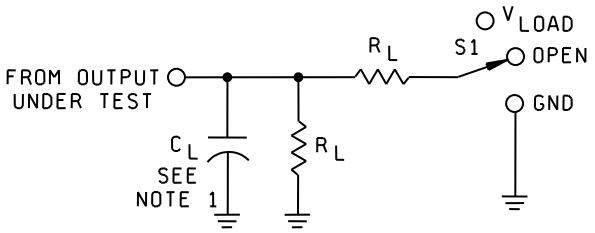


FIGURE 3. Logic diagram.

Device type 01			
Case outlines: X and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

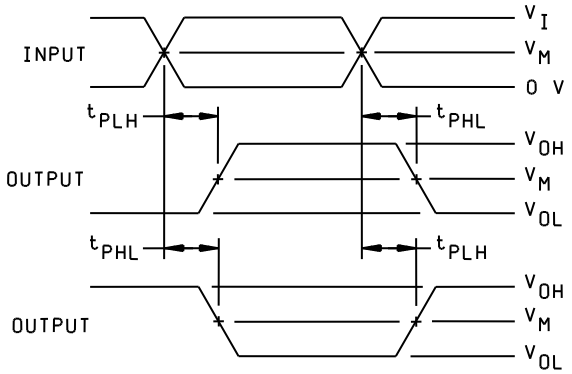
FIGURE 4. Terminal connections.



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L
	V_I	t_r/t_f				
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω
3.3 V ±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω



NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
3. t_{PLH} and t_{PHL} are the same as t_{pd}.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 2.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04658-01XE	01295	SN74LVC14AQDREP	LVC14AE
V62/04658-01YE	01295	SN74LVC14AQPWREP	LVC14AE

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493