

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. - PHN	08-11-19	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-01-27	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	22-07-14	Muhammad A. Akbar



**CURRENT DESIGN ACTIVITY CAGE CODE 16236  
HAS CHANGED NAMES TO:  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

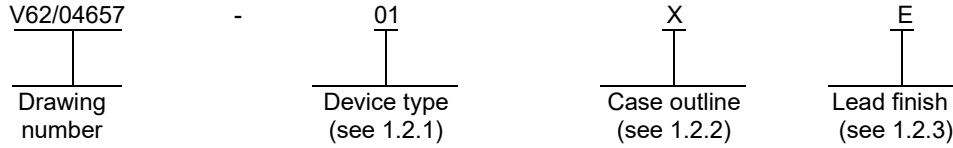
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REV	C	C	C	C	C	C	C	C	C	C	C										
SHEET	1	2	3	4	5	6	7	8	9	10	11										

<b>PMIC N/A</b>  Original date of drawing  YY MM DD  04-03-08	<b>PREPARED BY</b> Charles F. Saffle	<b>DEFENSE SUPPLY CENTER, COLUMBUS</b> COLUMBUS, OHIO 43218-3990 <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a>	
	<b>CHECKED BY</b> Charles F. Saffle	<b>TITLE</b> MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER, MONOLITHIC SILICON	
	<b>APPROVED BY</b> Thomas M. Hess	<b>DWG NO.</b> <p align="center"><b>V62/04657</b></p>	
	<b>SIZE</b> A	<b>CAGE CODE</b> <p align="center"><b>16236</b></p>	<b>PAGE</b> 1    OF    11
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3-line to 8-line decoder/demultiplexer microcircuit, with an operating temperature range of -40°C to +125°C (device type 01) and an extend with an operating temperature range of -55°C to +125°C (device type 2).

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01 <u>1/</u>	SN74LVC138A-EP	3-line to 8-line decoder/demultiplexer
02 <u>2/</u>	SN74LVC138A-EP	3-line to 8-line decoder/demultiplexer

1.2.2 Case outlines. The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MS-012	Plastic small-outline
Y	16	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1/ Device type 01 operated at -40°C to +125°C  
2/ Device type 02 operated at -55°C to +125°C

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1.3 Absolute maximum ratings. 3/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to 6.5 V
Input voltage range ( $V_i$ ) .....	-0.5 V to 6.5 V 4/
Output voltage range ( $V_o$ ) .....	-0.5 V to $V_{CC} + 0.5$ V 4/ 5/
Input clamp current ( $I_{IK}$ ) ( $V_i < 0$ ) .....	-50 mA
Output clamp current ( $I_{OK}$ ) ( $V_o < 0$ ) .....	-50 mA
Continuous output current ( $I_o$ ).....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND.....	$\pm 100$ mA
Package thermal impedance ( $\theta_{JA}$ ): 6/	
X package .....	73°C/W
Y package .....	108°C/W
Storage temperature range ( $T_{STG}$ ).....	-65°C to 150°C 7/

1.4 Recommended operating conditions. 8/

Supply voltage range ( $V_{CC}$ ):	
Operating .....	2.0 V to 3.6 V
Data retention only .....	1.5 V minimum
Minimum high level input voltage ( $V_{IH}$ ) ( $V_{CC} = 2.7$ V to 3.6 V) .....	2.0 V
Maximum low level input voltage ( $V_{IL}$ ) ( $V_{CC} = 2.7$ V to 3.6 V).....	0.8 V
Input voltage range ( $V_i$ ) .....	0.0 V to 5.5 V
Output voltage range ( $V_o$ ) .....	0.0 V to $V_{CC}$
Maximum high level output current ( $I_{OH}$ ):	
$V_{CC} = 2.7$ V .....	-12 mA
$V_{CC} = 3.0$ V .....	-24 mA
Maximum low level output current ( $I_{OL}$ ):	
$V_{CC} = 2.7$ V .....	12 mA
$V_{CC} = 3.0$ V .....	24 mA
Maximum input transition rise or fall rate ( $\Delta t/\Delta v$ ).....	10 ns/V
Operating free-air temperature range ( $T_A$ ):	
Device type 01 .....	-40°C to +125°C
Device type 02 .....	-55°C to +125°C

- 3/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 4/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 5/ The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- 6/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 7/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
- 8/ All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

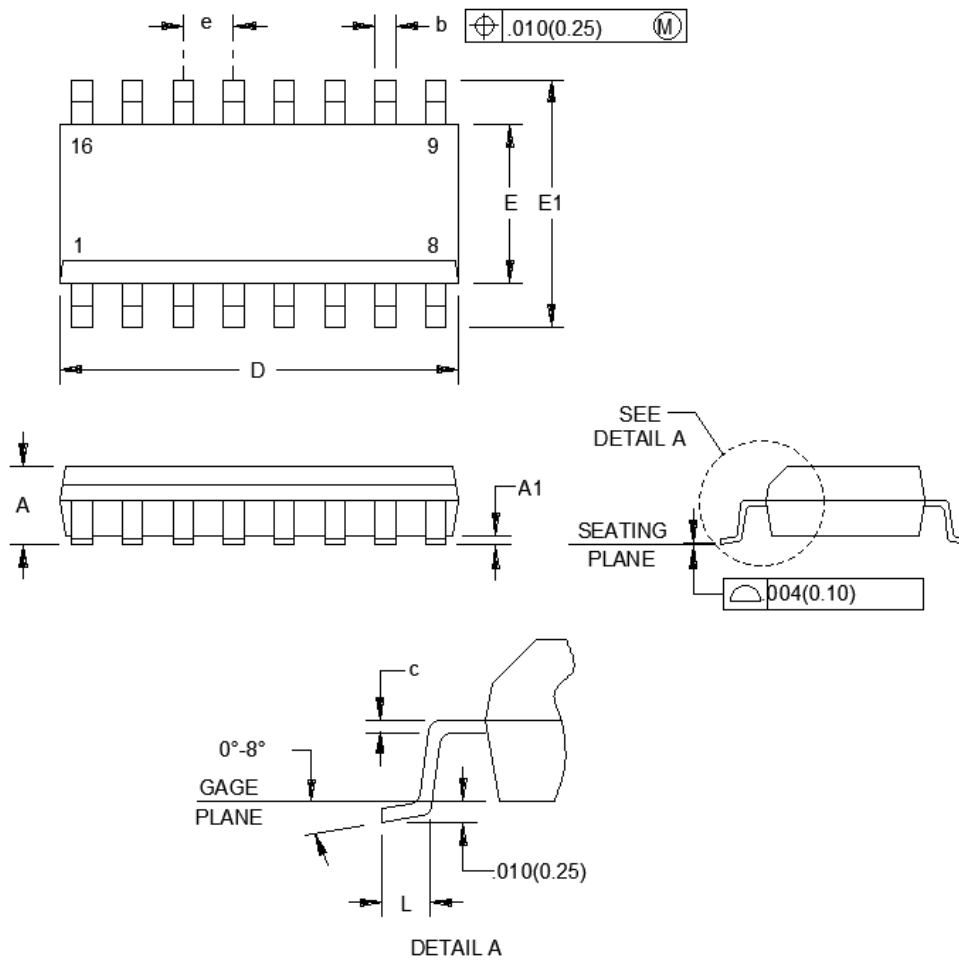
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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	V <sub>CC</sub>	Device type	Limits		Unit
					Min	Max	
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	2.7 V to 3.6 V	All	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -12 mA	2.7 V		2.2		
			3.0 V		2.4		
		I <sub>OH</sub> = -24 mA	3.0 V		2.2		
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 12 mA	2.7 V			0.4	
		I <sub>OL</sub> = 24 mA	3.0 V			0.55	
Input current	I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0 A	3.6 V			10	μA
Quiescent supply current delta	ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
Input capacitance	C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		5 TYP	pF	
Power dissipation capacitance per gate	C <sub>pd</sub>	f = 10 MHz	2.5 V		26 TYP	pF	
			3.3 V		27 TYP	pF	
Propagation delay time, A or B or C to Y	t <sub>pd</sub>	See figure 5.	2.7 V			7.9	ns
			3.3 V ±0.3 V		1	6.7	
Propagation delay time, $\overline{G2A}$ or $\overline{G2B}$ to Y			2.7 V			7.4	
			3.3 V ±0.3 V		1	6.5	
Propagation delay time, G1 to Y			2.7 V			6.4	
			3.3 V ±0.3 V		1	5.8	

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Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.75	---	.069	E	3.81	4.00	.150	.157
A1	0.10	0.25	.004	.010	E1	5.80	6.20	.228	.244
b	0.35	0.51	.014	.020	e	1.27	NOM	.050	NOM
c	0.20	NOM	.008	NOM	L	0.40	1.12	.016	.044
D	9.80	10.00	.386	.394					

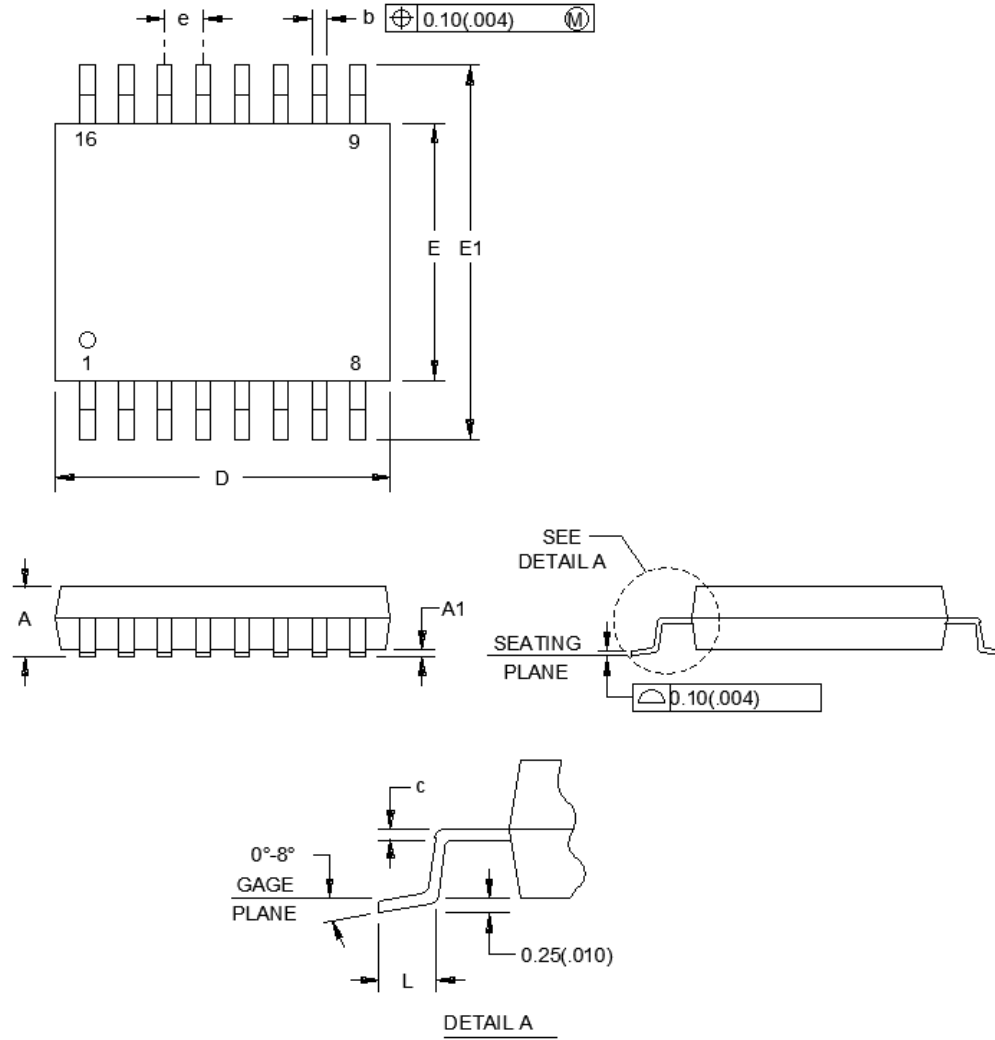
NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-012.
4. All linear dimensions are shown in inches (millimeters). Metric equivalents are given for general information only.

FIGURE 1. Case outlines.

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Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	.047	E	4.30	4.50	.169	.177
A1	0.005	0.15	.002	.006	E1	6.200	6.60	.244	.260
b	0.19	0.30	.007	.012	e	0.65	NOM	.026	NOM
c	0.15	NOM	.006	NOM	L	0.50	0.75	.020	.030
D	4.90	5.10	.193	.201					

NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

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Enable Inputs			Select Inputs			Outputs							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level  
L = Low voltage level  
X = Immaterial

FIGURE 2. Truth table.

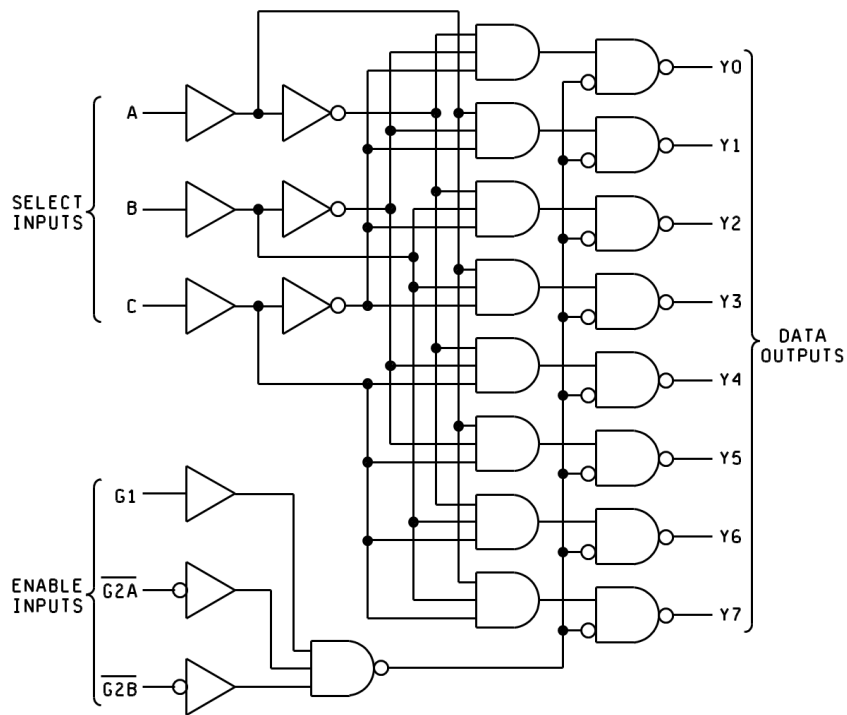


FIGURE 3. Logic diagram.

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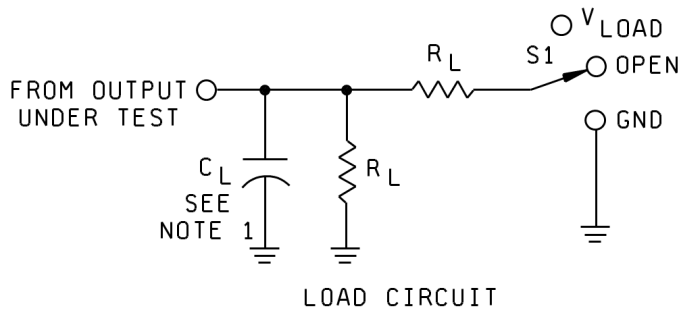


Device type 01

Case outlines	X and Y
Terminal number	Terminal symbol
1	A
2	B
3	C
4	$\overline{G2A}$
5	$\overline{G2B}$
6	G1
7	Y7
8	GND
9	Y6
10	Y5
11	Y4
12	Y3
13	Y2
14	Y1
15	Y0
16	V <sub>CC</sub>

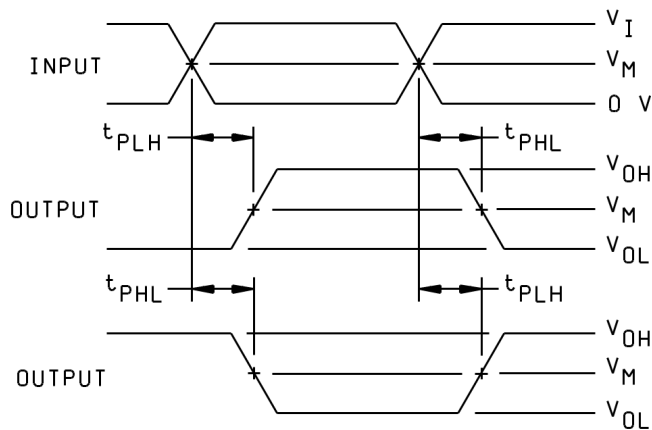
FIGURE 4. Terminal connections.

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TEST	S1
$t_{PLH}/t_{PHL}$	OPEN

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$
	$V_I$	$t_r/t_f$				
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$
3.3 V $\pm 0.3$ V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$



**NOTES:**

1.  $C_L$  includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_o = 50 \Omega$ .
3.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/04657-01XE	01295	SN74LVC138AQDREP	C138AEP
V62/04657-01YE	01295	SN74LVC138AQPWREP	C138AEP
V62/04657-02YE	01295	SN74LVC138AMPWTEP	C138AME

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

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