REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Correct the supply voltage range from: +3.0 V to +3.6 V, to: +4.5 V to +5.5 V. Update boilerplate to current requirements. - CFS	06-06-06	Thomas M. Hess
B	Make correction to symbol “c” dimensions under figure 1. Add two notes to figure 1. Update document paragraphs to current requirements. - ro	14-07-09	Charles F. Saffle
C	Update JEDEC package from MS-013-AC to MS-013. Under Table I, make correction to Zero scale error test conditions column by deleting footnote 3/ and replacing with 4/. Update document paragraphs to current requirements. - ro	22-01-06	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	C	C	C	C	C																	
PAGE	18	19	20	21	22																	

REV STATUS OF PAGES	**REV**	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 04-02-11	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 10-BIT ANALOG-TO-DIGITAL CONVERTERS, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/04647**
	REV **C**	**PAGE** 1 **OF** 22

AMSC N/A

5962-V095-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 10 bit analog to digital converters with serial control and 11 analog inputs microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04647	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function	Linearity error
01	TLC1543-EP	10 bit analog to digital converters with serial control and 11 analog inputs	±1.0 LSB

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MS-013	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +6.0 V 2/
Input voltage range (V_I)	-0.3 V to V_{CC} +0.3 V
Output voltage range (V_{OUT})	-0.3 V to V_{CC} +0.3 V
Positive reference voltage (V_{REF+})	V_{CC} +0.1 V
Negative reference voltage (V_{REF-})	-0.1 V
Peak input current range (any input)	±20 mA
Peak total input current (all inputs)	±30 mA
Operating free air temperature range (T_A)	-40°C to +125°C
Storage temperature range (T_{stg})	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from the case 10 seconds	+260°C

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{CC})	+4.5 V minimum to +5.5 V maximum
Positive reference voltage (V_{REF+})	V_{CC} nominal 4/
Negative reference voltage (V_{REF-})	0 V nominal 4/
Differential reference voltage range (V_{REF+} - V_{REF-})	2.5 V minimum to V_{CC} + 0.2 V maximum 4/
Analog input voltage range	0 V minimum to V_{CC} maximum 4/
High level control input voltage (V_{IH}) (V_{CC} = 4.5 V to 5.5 V)	2 V minimum
Low level control input voltage (V_{IL}) (V_{CC} = 4.5 V to 5.5 V)	0.8 V maximum
Setup time, address bits at data before I/O CLK ↑ ($t_{SU(A)}$)	100 ns minimum (see figure 5)
Hold time, address bits after I/O CLK ↑ ($t_{h(A)}$)	0 ns minimum (see figure 5)
Hold time, $\overline{CS}$ low after 10th I/O CLK ↓ ($t_{h(CS)}$)	0 ns minimum (see figure 5)
Setup time, $\overline{CS}$ low before clocking in first address bit ($t_{SU(CS)}$)	1.425 µs minimum (see figure 5) 5/

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise specified).

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ Analog input voltages greater than that applied to REF+ convert as all ones (11111111), while input voltages less than that applied to REF- convert as well as all zeros (00000000). The device is functional with reference voltages down to 1 V (V_{REF+} - V_{REF-}); however, the electrical specifications are no longer applicable.

5/ To minimize errors caused by noise at the chip select ($\overline{CS}$) input, the internal circuitry waits for three system clock cycles (or less) after $\overline{CS}$ ↓ falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address until the minimum $\overline{CS}$ setup time has elapsed.

1.4 Recommended operating conditions - continued. 3/

Clock frequency at I/O CLOCK	0 MHz minimum to 2.1 MHz maximum 6/
Pulse duration, I/O CLOCK high ($t_{WH(I/O)}$)	190 ns minimum
Pulse duration, I/O CLOCK low ($t_{WL(I/O)}$)	190 ns minimum
Transition time, I/O CLOCK ($t_{t(I/O)}$)	1 μs maximum (see figure 5) 7/
Transition time, ADDRESS and $\overline{CS}$ ($t_{t(CS)}$)	10 μs maximum
Operating free-air temperature range (T_A)	-40°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Test mode tables. The test mode tables shall be as shown in figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figure 5.

6/ For 11 to 16-bit transfers, after the tenth I/O CLOCK falling edge ($\leq$ 2 V) at least 1 I/O CLOCK rising edge ($\geq$ 2 V) must occur within 9.5 μs.

7/ This is the time required for the clock input signal to fall from V_{IH} minimum to V_{IL} maximum or to rise from V_{IL} maximum to V_{IH} minimum. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{CC} = V_{REF}+ = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.6 mA	-40°C to +125°C	01	2.4		V
		V_{CC} = 4.5 V to 5.5 V, I_{OH} = -20 µA			V_{CC} – 0.1		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 1.6 mA	-40°C to +125°C	01		0.4	V
		V_{CC} = 4.5 V to 5.5 V, I_{OL} = 20 µA				0.1	
Off state (high impedance state) output current	I_{OZ}	V_O = V_{CC}, $\overline{CS}$ at V_{CC}	-40°C to +125°C	01		10	µA
		V_O = 0, $\overline{CS}$ at V_{CC}				-10	
High level input current	I_{IH}	V_I = V_{CC}	-40°C to +125°C	01		2.5	µA
Low level input current	I_{IL}	V_I = 0	-40°C to +125°C	01		-2.5	µA
Operating supply current	I_{CC}	$\overline{CS}$ at 0	-40°C to +125°C	01		2.5	mA
Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V	-40°C to +125°C	01		1	µA
		Selected channel at 0 V, Unselected channel at V_{CC}				-1	
Maximum static analog reference current Into REF+		V_{REF}+ = V_{CC}, V_{REF}- = GND	-40°C to +125°C	01		10	µA
Input capacitance	C_I	Analog inputs, V_{CC} = 5 V	+25°C	01	7 typical		pF
		Control inputs, V_{CC} = 5 V			5 typical		
Linearity error 2/	E_L		-40°C to +125°C	01		±1	LSB
Zero scale error 3/	E_{ZS}	4/	-40°C to +125°C	01		±1	LSB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{CC} = V_{REF}+ = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Full scale error 3/	E_{FS}	4/	-40°C to +125°C	01		±1	LSB
Total unadjusted error 5/			-40°C to +125°C	01		±1	LSB
Self test output code		See figure 4, 6/ ADDRESS = 1011, V_{CC} = 5 V	25°C	01	512 typical		
		See figure 4, 6/ ADDRESS = 1100, V_{CC} = 5 V			0 typical		
		See figure 4, 6/ ADDRESS = 1101, V_{CC} = 5 V			1023 typical		
Conversion time	t_{conv}	See figure 5	-40°C to +125°C	01		21	µs
Total cycle time (access, sample, and conversion)	t_C	See figure 5 7/	-40°C to +125°C	01		21 +10 I/O CLOCK periods	µs
Channel acquisition time (sample)	t_{acq}	See figure 5 7/	-40°C to +125°C	01		6	I/O CLOCK periods
Valid time, DATA OUT remains valid after I/O CLOCK ↓	t_v	See figure 5	-40°C to +125°C	01	10		ns
Delay time, I/O CLOCK ↓ to DATA OUT valid	$t_{d(I/O - DATA)}$	See figure 5	-40°C to +125°C	01		240	ns
Delay time, tenth I/O CLOCK ↓ to EOC ↓	$t_{d(I/O - EOC)}$	See figure 5	-40°C to +125°C	01		240	ns
Delay time, EOC ↑ to DATA OUT (MSB)	$t_{d(EOC - DATA)}$	See figure 5	-40°C to +125°C	01		100	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{CC} = V_{REF}+ = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Enable time, $\overline{CS}$ ↓ to DATA OUT (MSB driven)	t_{PZH}, t_{PZL}	See figure 5	-40°C to +125°C	01		1.3	μs
Disable time, $\overline{CS}$ ↑ to DATA OUT (high impedance)	t_{PHZ}, t_{PLZ}	See figure 5	-40°C to +125°C	01		150	ns
Rise time, EOC	$t_{r(EOC)}$	See figure 5	-40°C to +125°C	01		300	ns
Fall time, EOC	$t_{f(EOC)}$	See figure 5	-40°C to +125°C	01		300	ns
Rise time, data bus	$t_{r(DATA)}$	See figure 5	-40°C to +125°C	01		300	ns
Fall time, data bus	$t_{f(DATA)}$	See figure 5	-40°C to +125°C	01		300	ns
Delay time, tenth I/O CLOCK ↓ to $\overline{CS}$ ↓ to abort conversion	$t_{d(I/O-CS)}$	8/	-40°C to +125°C	01		9	μs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
3/ Zero scale error is the difference between 0000000000 and the converted output for zero input voltage; full scale error is the difference between 1111111111 and the converted output for full scale input voltage.
4/ Analog input voltages greater than that applied to REF+ convert as all ones (11111111), while input voltages less than that applied to REF- convert as well as all zeros (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.
5/ Total unadjusted error comprises linearity, zero scale, and full scale errors.
6/ Both the input address and the output codes are expressed in positive logic.
7/ I/O CLOCK period = 1 / (I/O CLOCK frequency). See figure 5.
8/ Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.

Case X

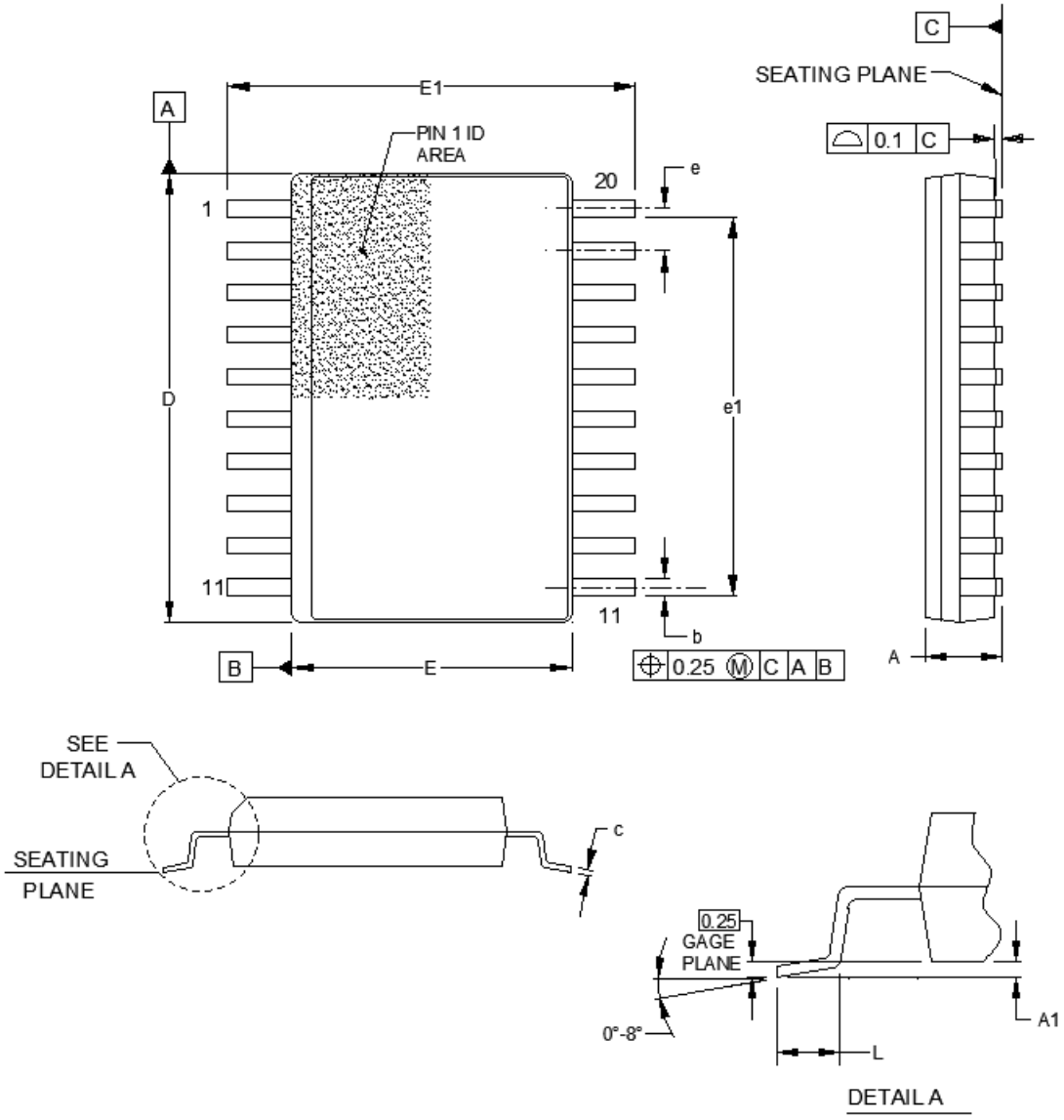


FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04647
		REV C	PAGE 8

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.104	---	2.65
A1	.004	.012	0.1	0.3
b	.012	.020	0.31	0.51
c	.004	.013	0.10	0.33
D	.496	.512	12.6	13.0
e	.050 BSC		1.27 BSC	
e1	.450 BSC		11.43 BSC	
E	.291	.299	7.4	7.6
E1	.392	.418	9.97	10.63
L	.016	.050	0.40	1.27

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Dimension D does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (.006 inch) per end.
3. Dimension E does not include interlead flash. Interlead flash shall not exceed 0.43 mm (.017 inch) per side.
4. Falls within reference to JEDEC MS-013.

FIGURE 1. Case outline. – continued.

Device type 01	
Case outline X	
Terminal number	Terminal symbol
1	A0
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	A8
10	GND
11	A9
12	A10
13	REF-
14	REF+
15	$\overline{CS}$
16	DATA OUT
17	ADDRESS
18	I/O CLOCK
19	EOC
20	V_{CC}

FIGURE 2. Terminal connections.

Terminal symbol	I/O	Description
ADDRESS	I	Serial address input. A 4 bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and shifts in on the first rising edges of I/O CLOCK. After the four address bits have been read into the address register, this input is ignored for the remainder of the current conversion period.
A0 – A10	I	Analog signal inputs. The 11 analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ.
$\overline{CS}$	I	Chip select. A high to low transition on this input resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low to high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	O	The three state serial output for the A/D conversion result. This output is in the high impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits shift out in order with LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more that ten clocks produce zeroes as the unused LSBs.
EOC	O	End of conversion. This output goes from a high to a low logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data is ready for transfer.
GND	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOCK	I	Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of the I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF- terminal.
REF-	I	The lower reference voltage value (nominally ground) is applied to this terminal.
V_{CC}	I	Positive supply voltage.

FIGURE 2. Terminal connections. – Continued.

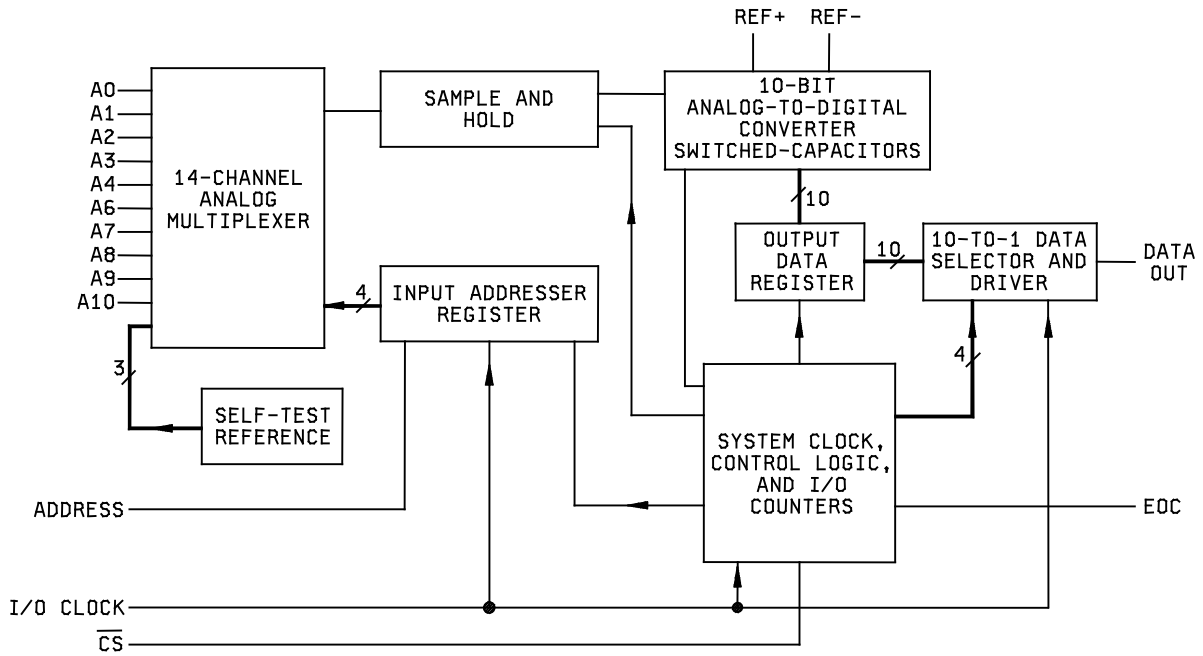


FIGURE 3. Logic diagram.

Mode operation

Modes		$\overline{CS}$	Number of I/O clocks	MSB at 1/ data out	Timing diagrams
Fast modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 5
	Mode 2	Low continuously	10	EOC rising edge	Figure 5
	Mode 3	High between conversion cycles	11 to 16 2/	$\overline{CS}$ falling edge	Figure 5
	Mode 4	Low continuously	16 2/	EOC rising edge	Figure 5
Slow modes	Mode 5	High between conversion cycles	11 to 16 2/	$\overline{CS}$ falling edge	Figure 5
	Mode 6	Low continuously	16 2/	16 th clock falling edge	Figure 5

1/ These edges also initiate serial interface communication.
2/ No more than 16 clocks should be used.

This table lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing edge which the MSB of the previous conversion appears at the output.

Fast modes.

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the tenth I/O CLOCK.

Mode 1: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 10 clock transfer.

Mode 2: fast mode $\overline{CS}$ active (low) continuously, 10 clock transfer.

Mode 3: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 11 to 16 clock transfer.

Mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16 clock transfer.

Slow modes.

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11 clock transfer into I/O CLOCK and the rising edge of the eleventh clock must occur before the conversion period is completed; otherwise, the device loses synchronization with the host serial interface and $\overline{CS}$ has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5 μs after the tenth I/O clock falling edge.

Mode 5: slow mode, $\overline{CS}$ inactive (high) between conversion cycles, 11 to 16 clock transfer.

Mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16 clock transfer.

FIGURE 4. Test mode tables.

Analog channel select address

Analog input selected	Value shifted into address input	
	Binary	Hex
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Test mode select address

Internal self-test voltage selected 1/	Value shifted into address input		Output result (Hex) 2/
	Binary	Hex	
$(V_{REF}+ - V_{REF}-) / 2$	1011	B	200
$V_{REF}-$	1100	C	000
$V_{REF}+$	1101	D	3FF

1/ $V_{REF}+$ is the voltage applied to the REF+ input, and $V_{REF}-$ is the voltage applied to the REF- input.
2/ The output results shown are the ideal values and vary with the reference stability and with internal offset.

Address bits.

The 4 bit analog channel select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one 14 inputs (11 analog inputs or three internal test inputs).

Analog inputs and test modes.

The 11 analog inputs and the three internal test inputs are selected by the 14 channel multiplexer according to the input address as shown in the tables above. The input multiplexer is a break-before make type to reduce input to input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

FIGURE 4. Test mode tables - Continued.

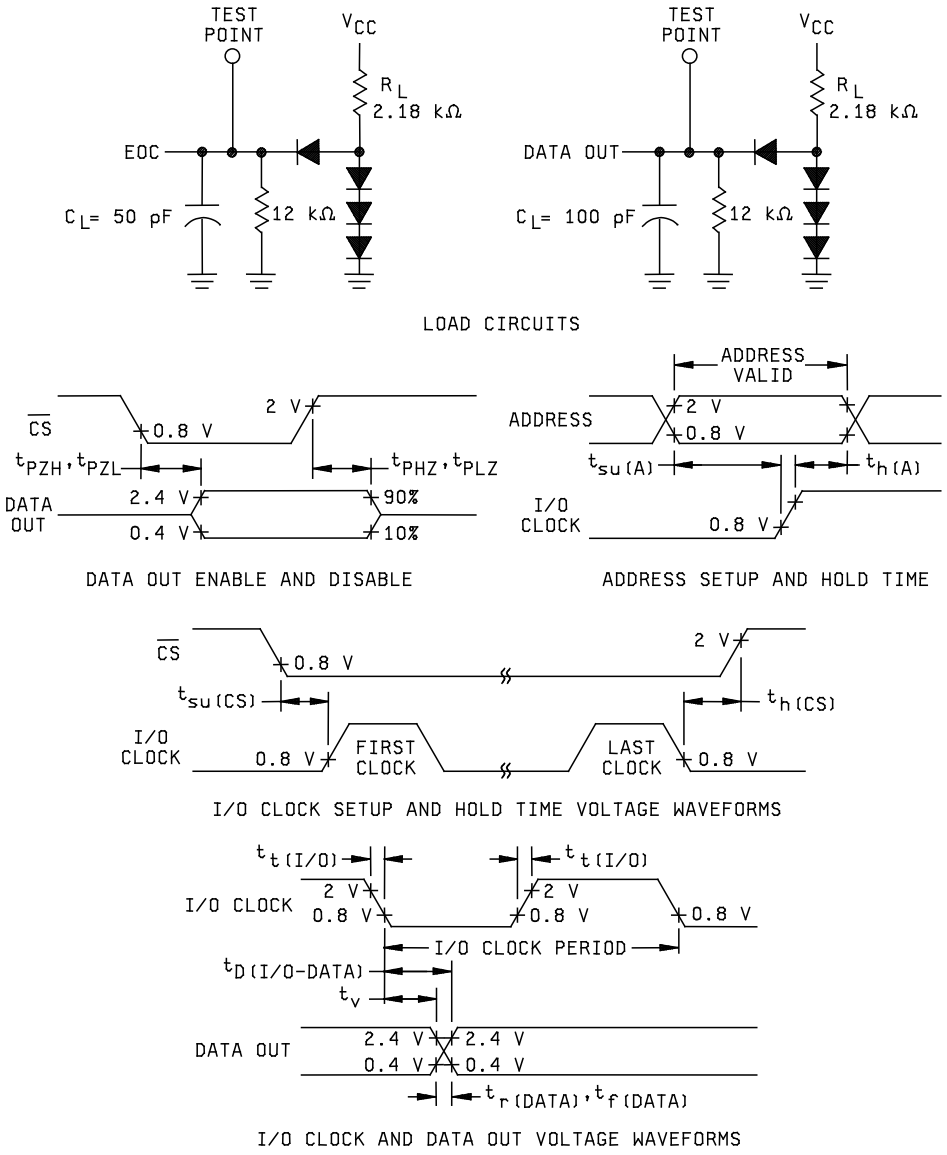
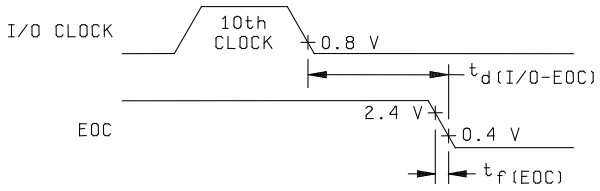
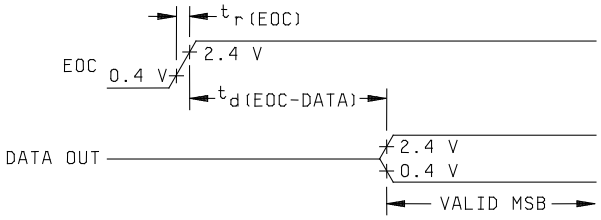


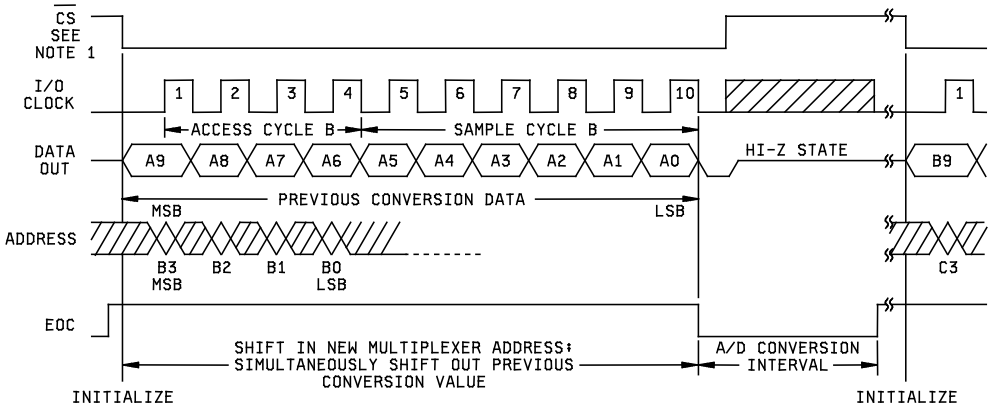
FIGURE 5. Timing waveforms and test circuit.



I/O CLOCK AND EOC VOLTAGE WAVEFORMS



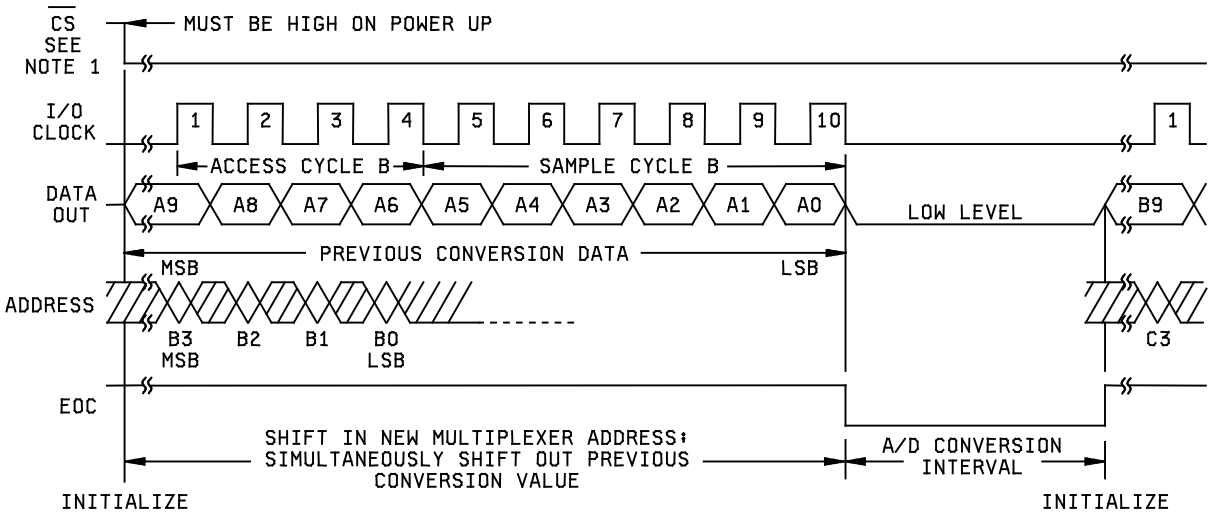
EOC AND DATA OUT VOLTAGE WAVEFORMS



TIMING FOR 10-CLOCK TRANSFER USING $\overline{CS}$

NOTE: 1. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

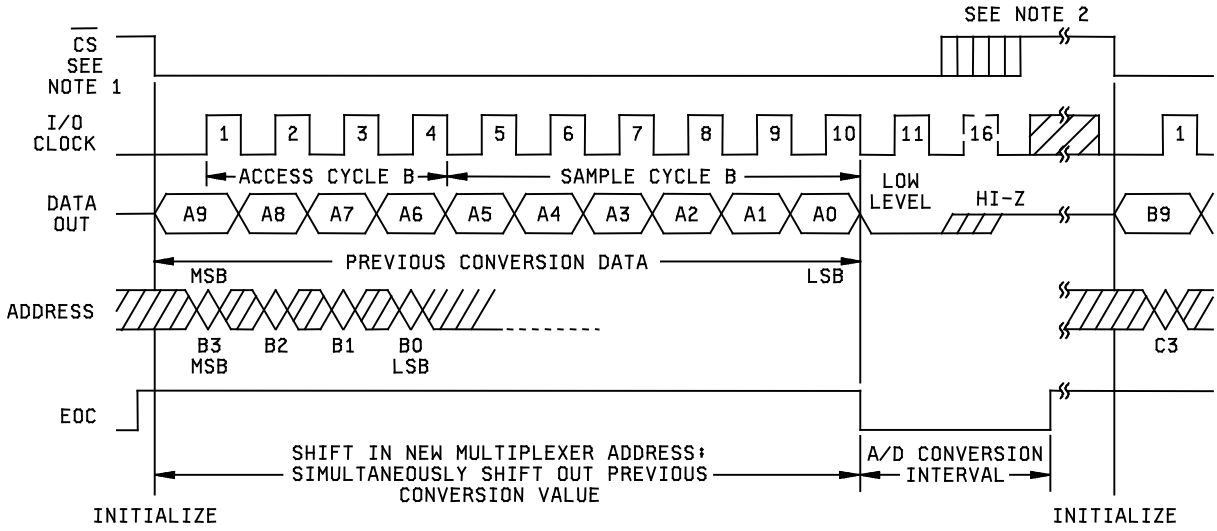
FIGURE 5. Timing waveforms and test circuit – Continued.



TIMING FOR 10-CLOCK TRANSFER NOT USING $\overline{CS}$

NOTE: 1. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 5. Timing waveforms and test circuit – Continued.

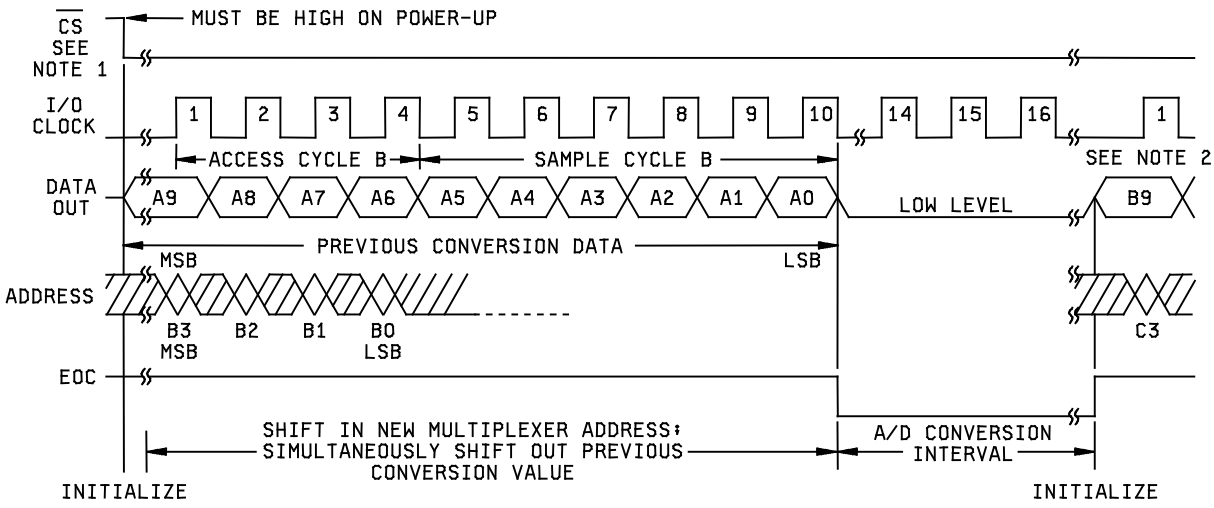


TIMING FOR 11- TO 16-CLOCK TRANSFER USING $\overline{CS}$
(SERIAL TRANSFER INTERVAL SHORTER THAN CONVERSION)

NOTES: 1. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

2. A low-to-high transition of $\overline{CS}$ disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

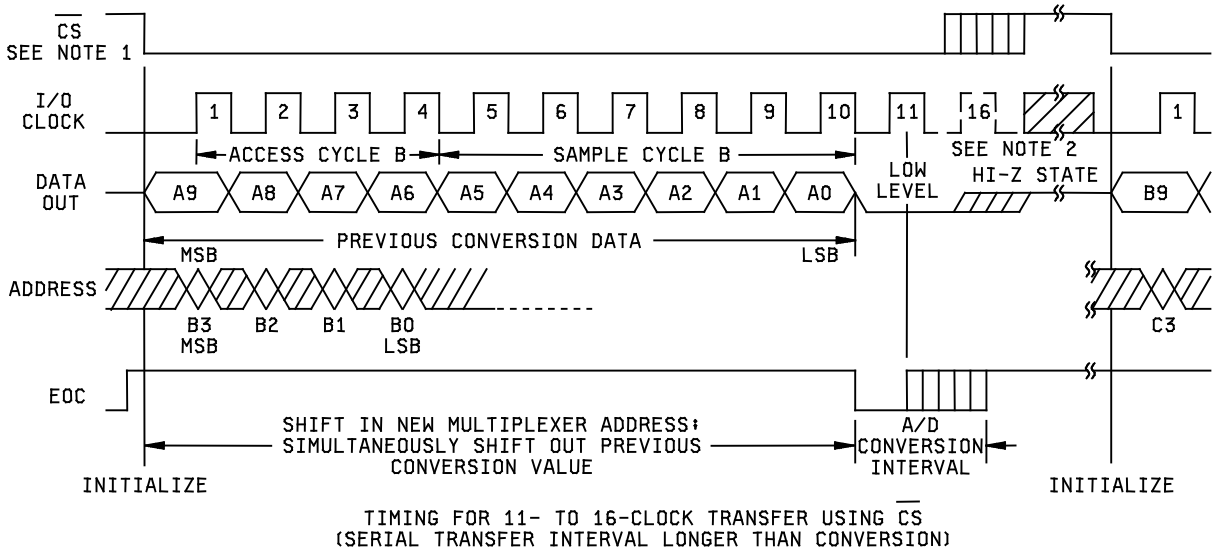
FIGURE 5. Timing waveforms and test circuit – Continued.



Timing for 16 clock transfer not using $\overline{CS}$ (serial transfer interval shorter than conversion)

NOTES:
1. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
2. The first I/O CLOCK must occur after the rising edge of EOC.

FIGURE 5. Timing waveforms and test circuit – Continued.

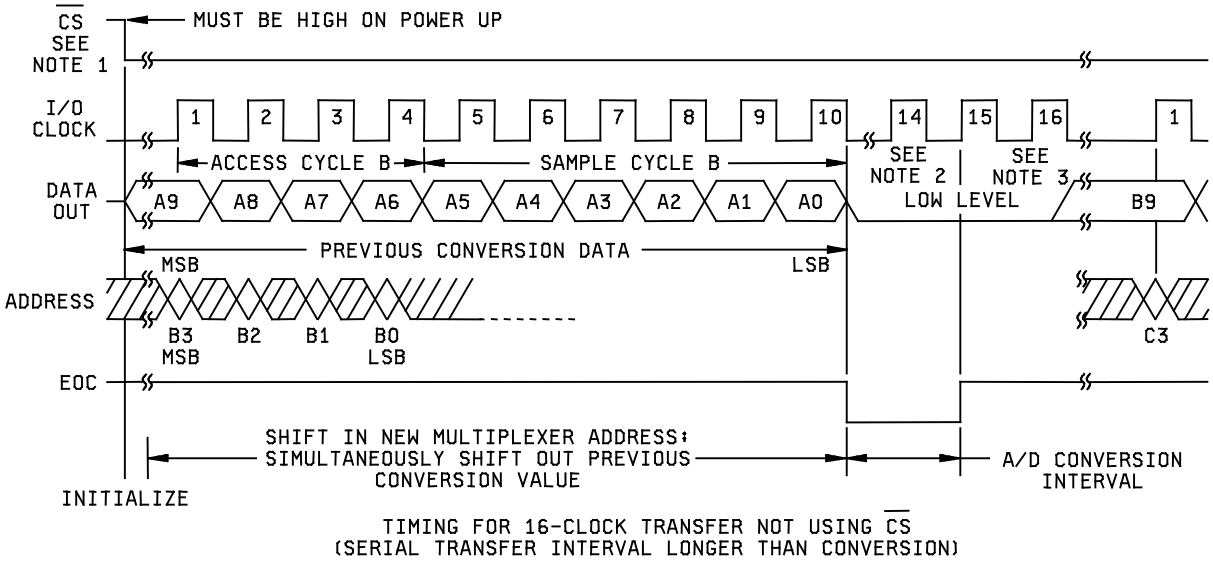


TIMING FOR 11- TO 16-CLOCK TRANSFER USING $\overline{CS}$
(SERIAL TRANSFER INTERVAL LONGER THAN CONVERSION)

NOTES: 1. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

2. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing interface synchronization.

FIGURE 5. Timing waveforms and test circuit – Continued.



TIMING FOR 16-CLOCK TRANSFER NOT USING $\overline{CS}$
(SERIAL TRANSFER INTERVAL LONGER THAN CONVERSION)

NOTES: 1. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
2. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.
3. The I/O CLOCK sequence is exactly 16 clock pulses long.

FIGURE 5. Timing waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/04647-01XE	01295	TLC1543QDWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243