REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add a footnote to Table I. Add footnotes to figure 1. Update boilerplate paragraphs to current requirements. - ro	10-10-19	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	18-01-25	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B	B	B	B	B					
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 04-02-11	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 2.7 V TO 5.5 V LOW POWER DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/04646**
	REV **B**	**PAGE** 1 **OF** 14

AMSC N/A

5962-V086-17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power dual 12-bit digital-to-analog converter (DAC) with power down microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/04646	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TLV5618A-EP	2.7 V to 5.5 V low power dual 12-bit digital-to-analog converter with power down

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD} to AGND)	7 V
Reference input voltage range	-0.3 V V_{DD} +0.3 V
Digital input voltage range	-0.3 V V_{DD} +0.3 V
Operating free-air temperature range (T_A)	-55°C to +125°C 2/
Storage temperature range	-65°C to +150°C 2/
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Package thermal impedance ($R\theta_{JA}$)	131°C/W

1.4 Recommended operating conditions. 3/

Supply voltage (V_{DD}):	
With V_{DD} = 5 V	4.5 V minimum to 5.5 V maximum
With V_{DD} = 3 V	2.7 V minimum to 3.3 V maximum
Power on reset	0.55 V minimum to 2 V maximum
High level digital input voltage (V_{IH}):	
With V_{DD} = 2.7 V	2 V minimum
With V_{DD} = 5.5 V	2.4 V minimum
Low level digital input voltage (V_{IL}):	
With V_{DD} = 2.7 V	0.6 V maximum
With V_{DD} = 5.5 V	1 V maximum
Reference voltage, V_{ref} to REF terminal:	
With V_{DD} = 5 V	AGND to V_{DD} – 1.5 V 4/
With V_{DD} = 3 V	AGND to V_{DD} – 1.5 V 4/
Load resistance (R_L)	2 kΩ minimum
Load capacitance (C_L)	100 pF maximum
Clock frequency (f_{CLK})	20 MHz maximum
Operating free air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ Due to the x2 output buffer, a reference input voltage ≥ (V_{DD} – 0.4 V) / 2 causes clipping of the transfer function.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section							
Power supply current	I_{DD}	Fast, no load, DAC latch = All ones, All inputs = AGND or V_{DD}, V_{DD} = 2.7 V to 5.5 V	-55°C to +125°C	01		2.3	mA
		Slow, no load, DAC latch = All ones, All inputs = AGND or V_{DD}, V_{DD} = 2.7 V to 5.5 V				1	
Power down supply current			-55°C to +125°C	01	1 typical		µA
Power supply rejection ration	PSRR	Zero scale 2/	-55°C to +125°C	01	-65 typical		dB
		Full scale 3/			-65 typical		
Static DAC specifications section							
Resolution			-55°C to +125°C	01	12		bits
Integral nonlinearity	INL	4/	-55°C to +125°C	01		±4	LSB
Differential nonlinearity	DNL	5/	-55°C to +125°C	01		±1	LSB
Zero scale error (offset error at zero scale)	E_{ZS}	6/	-55°C to +125°C	01		±12	mV
Zero scale error temperature coefficient	E_{ZS}(TC)	7/	-55°C to +125°C	01	3 typical		ppm / °C
Gain error	E_G	V_{DD} = 2.7 V – 5.5 V 8/	-55°C to +125°C	01		±0.6	% full scale V
Gain error temperature coefficient	E_G(TC)	9/	-55°C to +125°C	01	1 typical		ppm / °C
Output specifications section							
Output voltage range	V_O	R_L = 10 kΩ	-55°C to +125°C	01	0	V_{DD} - 0.4	V
Output load regulation accuracy		V_O = 4.096 V, 2.048 V, R_L = 2 kΩ to 10 kΩ	-55°C to +125°C	01		±0.29	% FS

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Reference input section							
Input voltage range	V_I		-55°C to +125°C	01	0	V_{DD} – 1.5	V
Input resistance	R_I		-55°C to +125°C	01	10 typical		MΩ
Input capacitance	C_I		-55°C to +125°C	01	5 typical		pF
Reference input bandwidth		Fast, REF = 0.2 V_{PP} + 1.024 V dc	-55°C to +125°C	01	1.3 typical		MHz
		Slow, REF = 0.2 V_{PP} + 1.024 V dc			525 typical		kHz
Reference feedthrough		10/ REF = 1 V_{PP} at 1 kHz + 1.024 V dc	-55°C to +125°C	01	-80 typical		dB
Digital inputs section							
High level digital input current	I_{IH}	$V_I = V_{DD}$	-55°C to +125°C	01		1	μA
Low level digital input current	I_{IL}	V_I = 0 V	-55°C to +125°C	01	-1		μA
Input capacitance	C_I		-55°C to +125°C	01	8 typical		pF
Analog output dynamic performance section							
Output settling time, full scale	$t_{s(FS)}$	Fast, R_L = 10 kΩ, C_L = 100 pF 11/	-55°C to +125°C	01		3	μs
		Slow, R_L = 10 kΩ, C_L = 100 pF 11/				10	
Output settling time, code to code	$t_{s(CC)}$	Fast, R_L = 10 kΩ, C_L = 100 pF 12/	-55°C to +125°C	01	1 typical		μs
		Slow, R_L = 10 kΩ, C_L = 100 pF 12/			2 typical		
Slew rate	SR	Fast, R_L = 10 kΩ, C_L = 100 pF 13/	-55°C to +125°C	01	3 typical		V/μs
		Slow, R_L = 10 kΩ, C_L = 100 pF 13/			0.5 typical		
Glitch energy		DIN = 0 to 1, FCLK = 100 kHz, $\overline{CS}$ = V_{DD}	-55°C to +125°C	01	5 typical		nV-s

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Analog output dynamic performance section - continued							
Signal to noise ratio	SNR	f_S = 102 kSPS, f_{out} = 1 kHz, R_L = 10 kΩ, C_L = 100 pF	-55°C to +125°C	01	76 typical		dB
Signal to noise + distortion	SINAD	f_S = 102 kSPS, f_{out} = 1 kHz, R_L = 10 kΩ, C_L = 100 pF	-55°C to +125°C	01	68 typical		dB
Total harmonic distortion	THD	f_S = 102 kSPS, f_{out} = 1 kHz, R_L = 10 kΩ, C_L = 100 pF	-55°C to +125°C	01	-68 typical		dB
Spurious free dynamic range	SFDR	f_S = 102 kSPS, f_{out} = 1 kHz, R_L = 10 kΩ, C_L = 100 pF	-55°C to +125°C	01	72 typical		dB
Digital input timing requirements section							
Setup time, $\overline{CS}$ low before first negative SCLK edge	t_{su} (CS - CK)		-55°C to +125°C	01	10		ns
Setup time, 16 th negative SCLK edge before $\overline{CS}$ rising edge	t_{su} (C16 - CS)		-55°C to +125°C	01	10		ns
SCLK pulse width high	t_{WH}		-55°C to +125°C	01	25		ns
SCLK pulse width low	t_{WL}		-55°C to +125°C	01	25		ns
Setup time, data ready before SCLK falling edge	$t_{su(D)}$		-55°C to +125°C	01	8		ns
Hold time, data held valid after SCLK falling edge	$t_{h(D)}$		-55°C to +125°C	01	10		ns
Hold time, $\overline{CS}$ high between cycles	$t_{h(CSH)}$	V_{DD} = 5 V	-55°C to +125°C	01	25		ns
		V_{DD} = 3 V			50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
$PSRR = 20 \log [E_{ZS} (V_{DD} max) – (E_{ZS} (V_{DD} min) / V_{DD} max)]$.

3/ Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
$PSRR = 20 \log [E_{G} (V_{DD} max) – (E_{G} (V_{DD} min) / V_{DD} max)]$.

4/ The relative accuracy of integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale, excluding the effects of zero code and full scale errors.

5/ The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes.

6/ Zero scale error is the deviation from zero voltage output when the digital input code is zero.

7/ Zero scale error temperature coefficient is given by:
$E_{ZS} TC = [E_{ZS} (T_{max}) – E_{ZS} (T_{min})] / 2V_{ref} \times 10^{6} / (T_{max} – T_{min})$.

8/ Gain error is the deviation from the ideal output ($2V_{ref}$ – 1 LSB) with an output load of 10 kΩ.

9/ Gain temperature coefficient is given by: $E_{G} TC = [E_{G} (T_{max}) – E_{g}(T_{min})] / 2V_{ref} \times 10^{6} / (T_{max} – T_{min})$.

10/ Reference feedthrough is measured at the DAC output with an input code = 0x000.

11/ Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively. Not tested, assured by design.

12/ Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design

13/ Slew rate determines the time it takes for a change of the DAC output from 10% to 90% of full scale voltage.

Case X

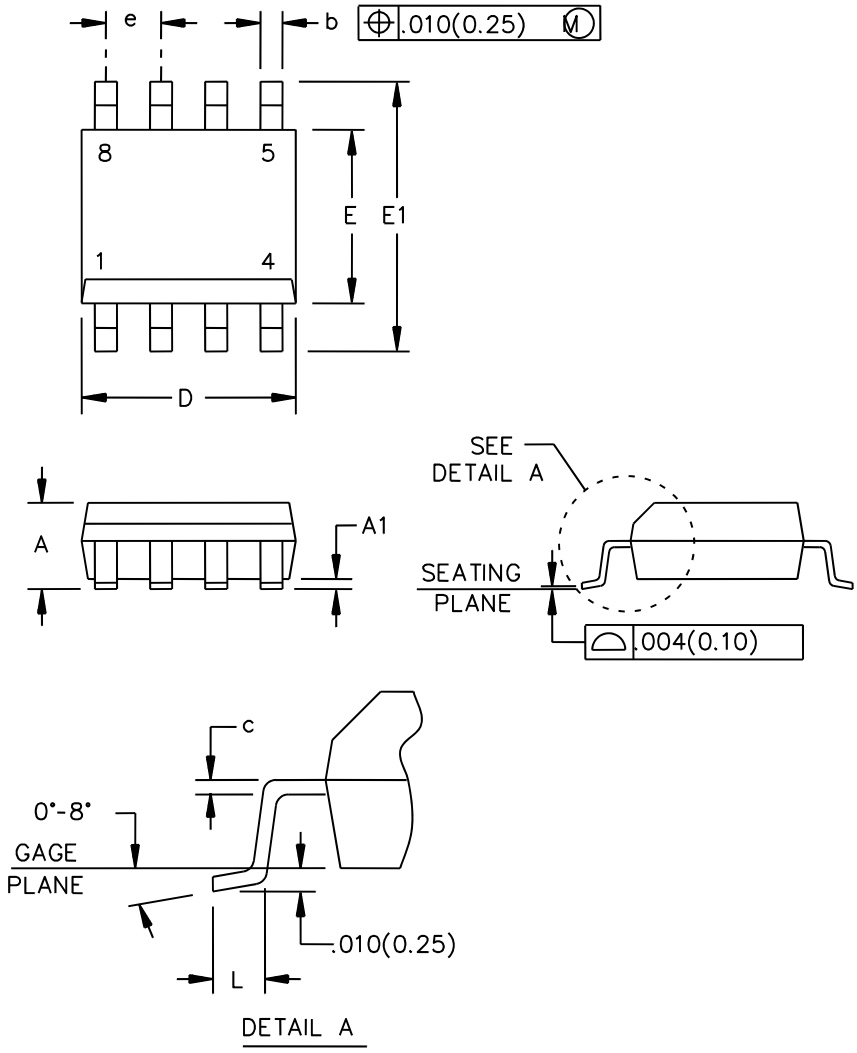

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04646
		REV B	PAGE 9

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
n	8 leads		8 leads	

NOTE:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline. – continued.

Device type 01			
Case outline X			
Terminal number	Terminal symbol	I/O/P	Description
1	DIN	I	Digital serial data input.
2	SCLK	I	Digital serial clock input.
3	$\overline{CS}$	I	Chip select. Digital input active low, used to enable/disable inputs.
4	OUTA	O	DAC A analog voltage output.
5	AGND	P	Ground.
6	REF	I	Analog reference voltage input.
7	OUTB	O	DAC B analog voltage output.
8	V_{DD}	P	Positive power supply.

FIGURE 2. Terminal connections.

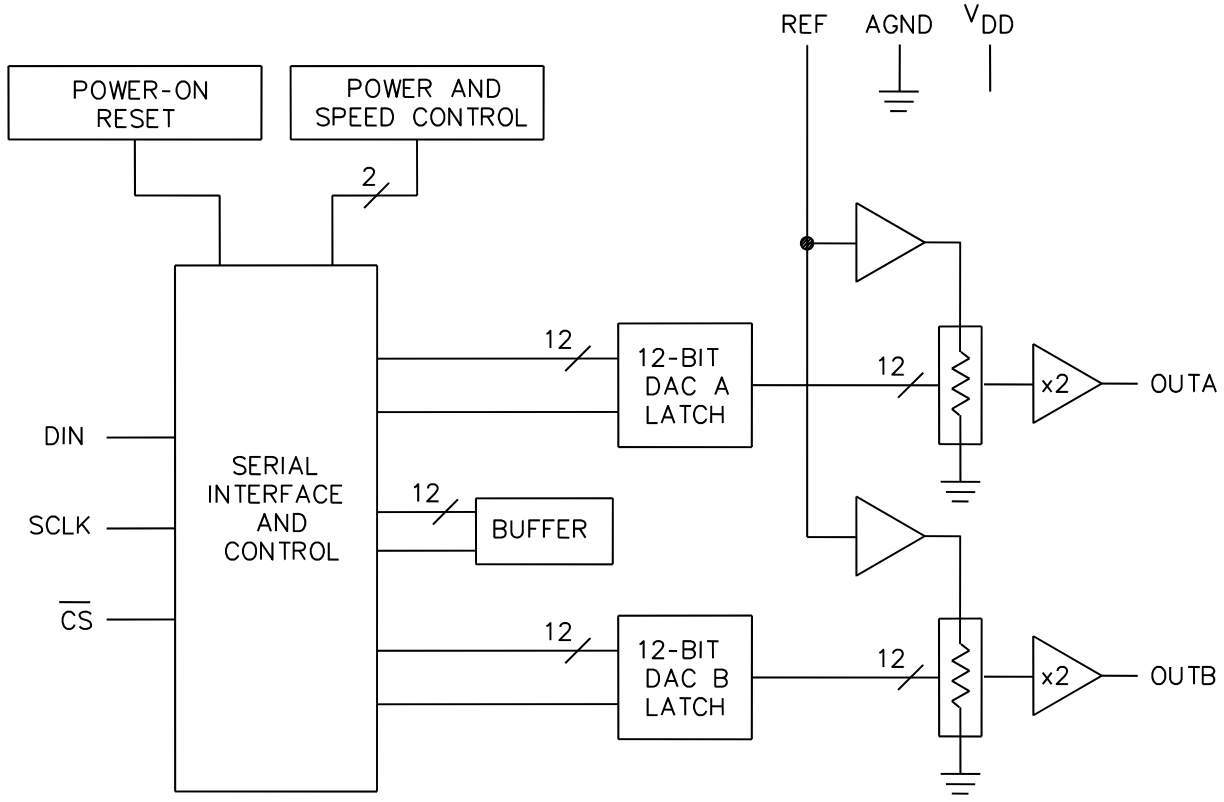

FIGURE 3. Block diagram.

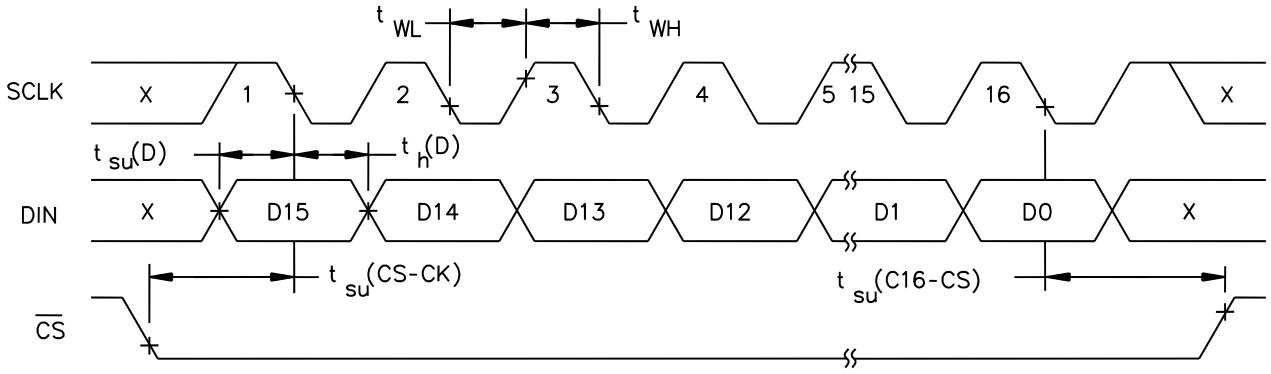

FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/		Vendor part number	Top side marking
V62/04646-01XE	01295	SOIC (D)	Tape and reel	TLV5618AMDREP	5618ME

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243