

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-04-06	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-01-25	Muhammad Akbar



CURRENT DESIGN ACTIVITY CAGE CODE 16236
 HAS CHANGED NAMES TO:
 DLA LAND AND MARITIME
 COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
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PMIC N/A	PREPARED BY Charles F. Saffle	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil	
Original date of drawing YY-MM-DD 04-01-29	CHECKED BY Charles F. Saffle	TITLE MICROCIRCUIT, DIGITAL, CMOS, 3.3-V 10-BIT ADDRESSABLE SCAN PORTS, MULTIDROP-ADDRESSABLE IEEE STD 1149.1 (JTAG) TAP TRANSCEIVERS, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/04644
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-V 10-bit addressable scan ports, multidrop-addressable IEEE Std 1149.1 (JTAG) TAP transceivers microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/04644</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVT8996-EP	3.3-V 10-bit addressable scan ports, multidrop-addressable IEEE Std 1149.1 (JTAG) TAP transceivers

1.2.2 Case outline. The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	24	JEDEC MS-013	Plastic small-outline
Y	24	JEDEC MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +4.6 V
Input voltage range (V_I)	-0.5 V to 7.0 V 2/
Voltage range applied to any output in the high or power-off state (V_O)	-0.5 V to 7.0 V 2/
Current into any output in the low state (I_{OL})	128 mA
Current into any output in the high state (I_{OH})	64 mA 3/
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA
Package thermal impedance (θ_{JA}): 4/	
Case X	46°C/W
Case Y	88°C/W
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	+2.7 V to +3.6 V
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum low level input voltage (V_{IL})	+0.8 V
Input voltage range (V_I)	0.0 V to +5.5 V
Maximum high level output current (I_{OH})	-32 mA
Maximum low level output current (I_{OL})	64 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$)	10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$)	200 μ s/V
Operating free-air temperature range (T_A)	-40°C to +85°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
- 3/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

- IEEE Standard 1149.1-1990 - Standard Test Access Port and Boundary Scan Architecture

(Copies of these documents are available online at <http://www.ieee.org> or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions -40°C ≤ T _A ≤ +85°C Device type: All unless otherwise specified		V _{CC}	Limits		Unit	
					Min	Max		
Input clamp voltage	V _{IK}	I _I = -18 mA		2.7 V		-1.2	V	
High level output voltage	V _{OH}	I _{OH} = -100 μA		2.7 V and 3.6 V	V _{CC} - 0.2		V	
		I _{OH} = -8 mA		2.7 V	2.4			
		I _{OH} = -32 mA		3.0 V	2.0			
Low level output voltage	V _{OL}	I _{OL} = 100 μA		2.7 V		0.2	V	
		I _{OL} = 24 mA				0.5		
		I _{OL} = 16 mA		3.0 V		0.4		
		I _{OL} = 32 mA				0.5		
		I _{OL} = 64 mA				0.55		
Input current	I _I	V _I = 5.5 V		0.0 V and 3.6 V		10	μA	
		PTCK V _I = V _{CC} or GND		3.6 V		±1.0		
High level input current	I _{IH}	PTDI, PTMS, PTRST V _I = V _{CC}		3.6 V		1.0	μA	
		A9 - A0, BYP, STDI V _I = V _{CC}		3.6 V		1.0		
Low level input current	I _{IL}	PTDI, PTMS, PTRST V _I = GND		3.6 V	-8.0	-30	μA	
		A9 - A0, BYP, STDI V _I = GND		3.6 V	-25	-100		
Input/output power-off leakage current	I _{off}	V _I or V _O = 0.0 V to 4.5 V		0.0 V		±100	μA	
Three-state output leakage current high	I _{OZH}	PTDO, STDO	V _O = 3.0 V	3.6 V		5.0	μA	
Three-state output leakage current low	I _{OZL}	PTDO, STDO	V _O = 0.5 V	3.6 V		-5.0	μA	
Three-state output leakage current power-up	I _{OZPU}	V _O = 0.5 V to 3.0 V		0.0 V to 1.5 V		±100	μA	
Three-state output leakage current power-down	I _{OZPD}	V _O = 0.5 V to 3.0 V		0.0 V to 1.5 V		±100	μA	
Quiescent supply current	I _{CC}	Off, STCK = H, STMS = H		I _O = 0.0 A V _I = V _{CC} or GND	3.6 V		2.0	
		On, PTDO = L, STCK = L, STDO = L, STMS = L					20	
		On, PTDO = H, STCK = H, STDO = H, STMS = H					7.0	
		TRST, STCK = L					10	
Quiescent supply current delta, TTL input levels	ΔI _{CC} 2/	One input at V _{CC} - 0.6 V. Other inputs at V _{CC} or GND.		3.0 V and 3.6 V		0.2	mA	
Input capacitance	C _I	V _I = 3.0 V or 0.0 V, T _A = 25°C		3.3 V	3.5 TYP		pF	
Output capacitance	C _O	V _O = 3.0 V or 0.0 V, , T _A = 25°C		3.3 V	6.5 TYP			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions -40°C ≤ T _A ≤ +85°C Device type: All unless otherwise specified	V _{CC}	Limits		Unit		
				Min	Max			
Clock frequency	f _{clock}	PTCK	See figure 4	2.7 V		20	MHz	
				3.0 V and 3.6 V		25		
Pulse duration	t _w	$\overline{\text{BYP}}$ low 3/	2.7 V and 3.6 V		8.0		ns	
		PTCK high			20			
		PTCK low			12			
		$\overline{\text{PTRST}}$ low			9.0			
Setup time	t _{su}	A9 – A0 before PTCK↓ 4/	2.7 V and 3.6 V		10.2			
		PTDI before PTCK↑			10.1			
		PTMS before $\overline{\text{BYP}}$ ↑ 3/			4.0			
		PTMS before PTCK↑			10			
Hold time	t _h	A9 – A0 after PTCK↓ 4/	2.7 V and 3.6 V		4.0			
		PTDI after PTCK↑			4.0			
		PTMS after $\overline{\text{BYP}}$ ↑ 3/			4.0			
		PTMS after PTCK↑			4.0			
Maximum clock frequency, from PTCK	f _{max}	See figure 4			2.7 V	20		MHz
					3.0 V and 3.6 V	25		
Propagation delay time, $\overline{\text{BYP}}$ ↑ to $\overline{\text{CON}}$	t _{PLH}				2.7 V	1.0	9.4	ns
					3.0 V and 3.6 V	1.0	8.2	
Propagation delay time, $\overline{\text{BYP}}$ ↓ to $\overline{\text{CON}}$	t _{PHL}				2.7 V	1.0	11.4	
					3.0 V and 3.6 V	1.0	9.8	
Propagation delay time, $\overline{\text{BYP}}$ ↓ to STMS	t _{PLH}				2.7 V	2.5	14.7	
	t _{PHL}				3.0 V and 3.6 V	2.5	12	
Propagation delay time, PTCK to STCK	t _{PLH}				2.7 V	2.5	13.4	
	t _{PHL}				3.0 V and 3.6 V	2.5	11.7	
Propagation delay time, PTCK to STCK	t _{PLH}				2.7 V	1.0	11.2	
	t _{PHL}				3.0 V and 3.6 V	1.0	9.6	
Propagation delay time, PTCK↓ to $\overline{\text{CON}}$	t _{PLH}				2.7 V	1.0	11.8	
	t _{PHL}				3.0 V and 3.6 V	1.0	10	
Propagation delay time, PTCK↓ to $\overline{\text{CON}}$	t _{PLH}				2.7 V	3.5	24.8	
	t _{PHL}				3.0 V and 3.6 V	3.5	20.6	
Propagation delay time, PTCK↓ (shadow-protocol acknowledge) to PTDO	t _{PLH}				2.7 V	3.5	27.4	
	t _{PHL}				3.0 V and 3.6 V	3.5	23	
Propagation delay time, PTCK↓ (connect) to STMS	t _{PLH}				2.7 V	3.0	17.4	
	t _{PHL}				3.0 V and 3.6 V	3.0	14.7	
Propagation delay time, PTCK↓ (connect) to STMS	t _{PLH}				2.7 V	3.0	17.7	
	t _{PHL}				3.0 V and 3.6 V	3.0	15	
Propagation delay time, PTCK↓ (connect) to STMS	t _{PLH}				2.7 V	5.5	23.9	
	t _{PHL}				3.0 V and 3.6 V	5.5	19.9	
					2.7 V	5.5	22.9	
					3.0 V and 3.6 V	5.5	19.1	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions -40°C ≤ T _A ≤ +85°C Device type: All unless otherwise specified	V _{CC}	Limits		Unit
				Min	Max	
Propagation delay time, PTDI to STDO	t _{PLH}	See figure 4	2.7 V	1.0	9.9	ns
	t _{PHL}		3.0 V and 3.6 V	1.0	8.3	
			2.7 V	1.0	10.2	
	t _{PHL}		3.0 V and 3.6 V	1.0	8.6	
2.7 V			1.0	9.8		
Propagation delay time, PTMS to STMS	t _{PLH}		3.0 V and 3.6 V	1.0	8.5	
	t _{PHL}		2.7 V	1.0	10.3	
			3.0 V and 3.6 V	1.0	8.8	
	2.7 V		1.0	10		
Propagation delay time, PTRST to STRST	t _{PLH}		3.0 V and 3.6 V	1.0	8.4	
	t _{PHL}		2.7 V	1.0	10.5	
			3.0 V and 3.6 V	1.0	9.0	
	2.7 V		3.5	29		
Propagation delay time, PTRST↓ to CON	t _{PLH}		3.0 V and 3.6 V	3.5	23.9	
	2.7 V		2.5	15.7		
Propagation delay time, PTRST↓ to STMS	t _{PLH}		3.0 V and 3.6 V	2.5	13.2	
	2.7 V	1.0	8.2			
Propagation delay time, STDI to PTDO	t _{PLH}	3.0 V and 3.6 V	1.0	6.8		
	t _{PHL}	2.7 V	1.0	9.0		
		3.0 V and 3.6 V	1.0	7.6		
	2.7 V	1.5	10.6			
Propagation delay time, BYP ↓ to PTDO	t _{PZH} 6/	3.0 V and 3.6 V	1.5	9.0		
	t _{PZL}	2.7 V	1.5	11.9		
		3.0 V and 3.6 V	1.5	10.1		
	2.7 V	1.5	9.3			
Propagation delay time, BYP↓ to STDO	t _{PZH} 7/	3.0 V and 3.6 V	1.5	8.1		
	t _{PZL}	2.7 V	1.5	10.7		
		3.0 V and 3.6 V	1.5	9.2		
	2.7 V	4.0	16.8			
Propagation delay time, PTCK↓ to PTDO	t _{PZH} 6/	3.0 V and 3.6 V	4.0	14.5		
	2.7 V	4.0	18.4			
Propagation delay time, PTCK↓ to STDO	t _{PZH} 7/	3.0 V and 3.6 V	4.0	15.8		
	t _{PZL}	2.7 V	4.0	19.1		
		3.0 V and 3.6 V	4.0	16.4		
	2.7 V	1.5	9.3			
Propagation delay time, BYP↑ to PTDO	t _{PHZ} 6/	3.0 V and 3.6 V	1.5	8.3		
	t _{PLZ}	2.7 V	1.5	8.3		
		3.0 V and 3.6 V	1.5	7.7		
	2.7 V	1.5	7.7			

See footnotes at end of table.

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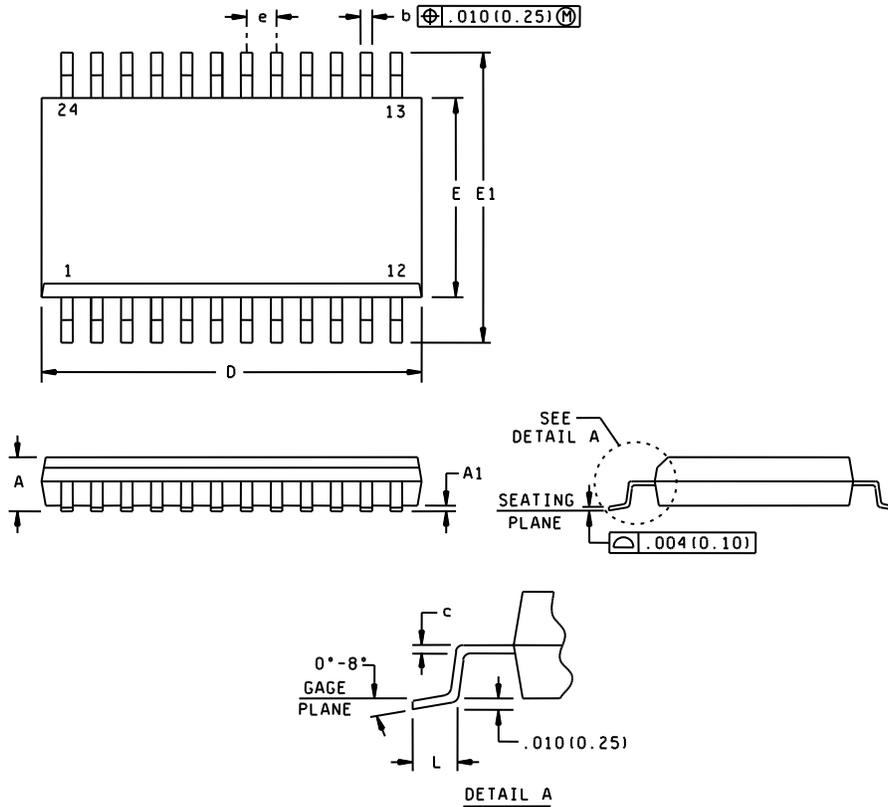
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions -40°C ≤ T _A ≤ +85°C Device type: All unless otherwise specified	V _{CC}	Limits		Unit
				Min	Max	
Propagation delay time, $\overline{BYP}\uparrow$ to STDO	t _{PHZ} 7/	See figure 4	2.7 V	1.5	8.5	ns
			3.0 V and 3.6 V	1.5	7.3	
	t _{PLZ}		2.7 V	1.5	7.1	
			3.0 V and 3.6 V	1.5	7.4	
Propagation delay time, PTCK↓ to PTDO	t _{PHZ} 6/		2.7 V	3.0	16.6	
			3.0 V and 3.6 V	3.0	14	
	t _{PLZ}		2.7 V	3.0	15.5	
			3.0 V and 3.6 V	3.0	13.9	
Propagation delay time, PTCK↓ to STDO	t _{PHZ} 7/	2.7 V	3.5	18.3		
		3.0 V and 3.6 V	3.5	16.9		
	t _{PLZ} 8/	2.7 V	3.5	15.1		
		3.0 V and 3.6 V	3.5	13		
Propagation delay time, $\overline{PTRST}\downarrow$ to PTDO	t _{PHZ} 5/	2.7 V	3.5	21.6		
		3.0 V and 3.6 V	3.5	18.3		
	t _{PLZ}	2.7 V	3.5	19.6		
		3.0 V and 3.6 V	3.5	19.3		
Propagation delay time, $\overline{PTRST}\downarrow$ to STDO	t _{PHZ} 6/	2.7 V	4.5	21.4		
		3.0 V and 3.6 V	4.5	18.2		
	t _{PLZ}	2.7 V	4.5	23.4		
		3.0 V and 3.6 V	4.5	20.6		

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
- 3/ In normal application of the ASP, such timing requirements with respect to BYP are met implicitly and, therefore, need not be considered.
- 4/ These requirements apply only in the case in which the address inputs are changed during a shadow protocol. For normal application of the ASP, it is recommended that the address inputs remain static throughout any shadow protocols. In such cases, the timing of address inputs relative to PTCK need not be considered.
- 5/ The transitions at STMS are possible only when a shadow-protocol select is issued while STMS is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended since state synchronization of the primary TAP to secondary TAP cannot be ensured.
- 6/ In most applications, the node to which PTDO is connected has a pullup resistor. In such cases, this parameter is not significant.
- 7/ In most applications, the node to which STDO is connected has a pullup resistor. In such cases, this parameter is not significant.
- 8/ This parameter applies only in case of protocol result HARD ERROR.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		0.104		2.65	E	0.291	0.299	7.39	7.59
A1	0.004	0.012	0.10	0.30	E1	0.400	0.419	10.15	10.65
b	0.014	0.020	0.35	0.51	e	0.050 NOM		1.27 NOM	
c	0.010 NOM		0.25 NOM		L	0.016	0.050	0.40	1.27
D	0.600	0.610	15.24	15.49					

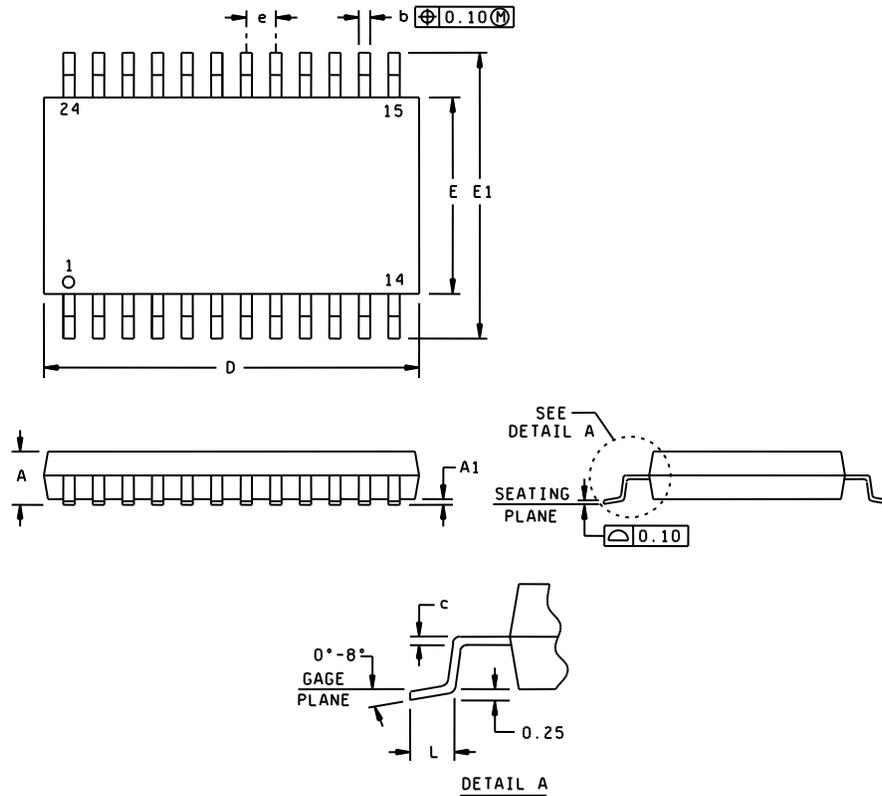
NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-013.
4. All linear dimensions are shown in inches (millimeters). Metric equivalents are given for general information only.

FIGURE 1. Case outline.

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Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		1.20		0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 NOM		0.026 NOM	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	7.70	7.90	0.303	0.311					

NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches).
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outline - Continued.

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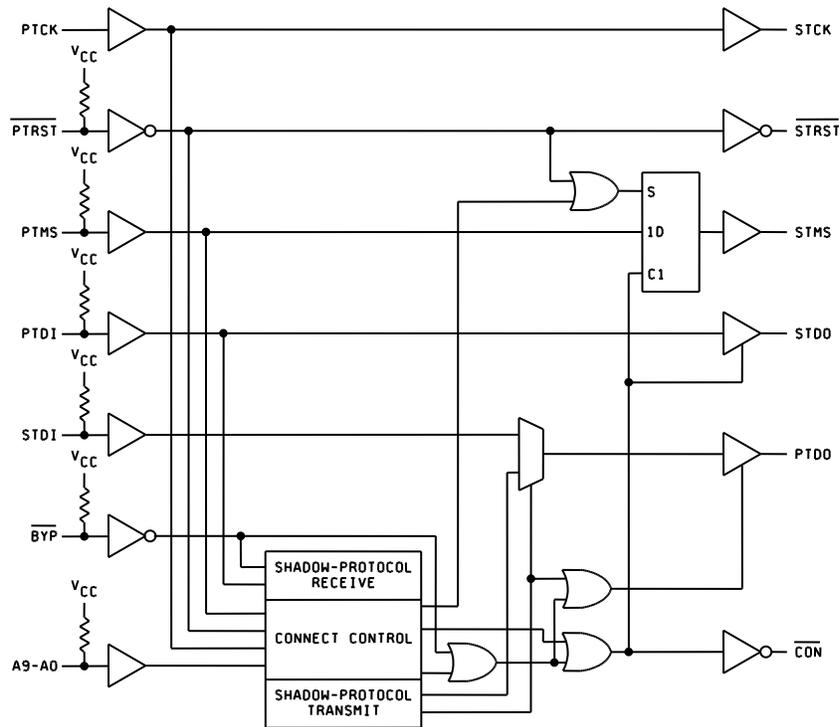
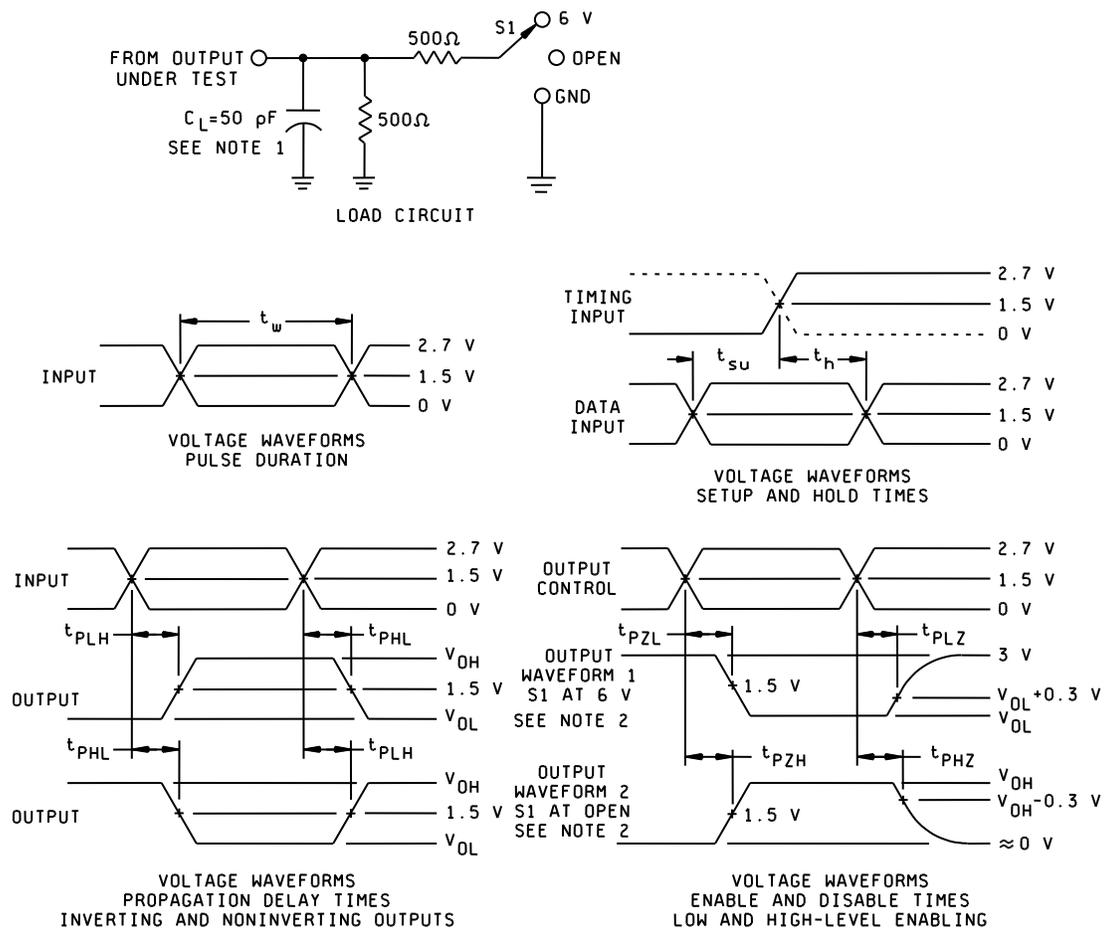


FIGURE 2. Block diagram.

Device type 01			
Case outlines: X and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A4	13	$\overline{\text{STRST}}$
2	A3	14	STDO
3	A2	15	STMS
4	A1	16	STCK
5	A0	17	STDI
6	$\overline{\text{BYP}}$	18	$\overline{\text{CON}}$
7	GND	19	V _{CC}
8	PTDO	20	A9
9	PTCK	21	A8
10	PTMS	22	A7
11	PTDI	23	A6
12	$\overline{\text{PTRST}}$	24	A5

FIGURE 3. Terminal connections.

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- NOTES:
1. C_L includes probe and jig capacitance.
 2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 4. The outputs are measured one at a time with one transition per measurement.
 5. For 3-state outputs tests:

t _{PLH} /t _{PHL}	S1 = Open
t _{PLZ} /t _{PZL}	S1 = 6 V
t _{PHZ} /t _{PZH}	S1 = GND

FIGURE 4. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 2.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04644-01XE	<u>2/</u>	SN74LVT8996IDWREP	LVT8996EP
V62/04644-01YE	01295	SN74LVT8996IPWREP	LVT8996EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ This part is not available as of the release date of this drawing.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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