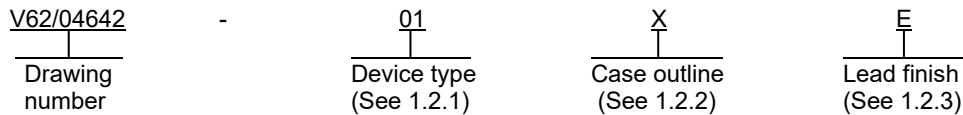




1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power current mode push-pull pulse width modulator microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>	<u>UVLO option</u>
01	UCC2808A-1EP	Pulse width modulator	12.5 V / 8.3 V
02	UCC2808A-2EP	Pulse width modulator	4.3 V / 4.1 V

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage (IDD ≤ 10 mA) .....	15 V
Supply current .....	20 mA
OUTA/OUTB source current (peak) .....	-0.5 A
OUTA/OUTB sink current (peak) .....	1.0 A
Analog inputs (FB, CS) .....	-0.3 V to VDD 0.3 V, not to exceed 6 V
Power dissipation at TA = 25°C (D package) .....	650 mW
Storage temperature range (TSTG) .....	-65°C to 150°C 3/
Junction temperature (TJ) .....	-55°C to +150°C
Lead temperature (soldering, 10 seconds) .....	300°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Currents are positive into, negative out of the specified terminal.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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1.4 Recommended operating conditions. 4/

Supply voltage range (VDD) ..... 10 V  
Operating free-air temperature range (TA) ..... -40°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Oscillator section							
Oscillator frequency			-40°C to +125°C	All	175	213	kHz
Oscillator amplitude / V <sub>DD</sub>		3/	-40°C to +125°C	All	0.44	0.56	V/V
Error amplitude section							
Input voltage		COMP = 2 V	-40°C to +125°C	All	1.95	2.05	V
Input bias current			-40°C to +125°C	All	-1	1	μA
Open loop voltage gain			-40°C to +125°C	All	60		dB
COMP sink current		FB = 2.2 V, COMP = 1 V	-40°C to +125°C	All	0.3		mA
COMP source current		FB = 1.3 V, COMP = 3.5 V	-40°C to +125°C	All	-0.2		mA
PWM section							
Maximum duty cycle		Measured at O <sub>UTA</sub> or O <sub>UTB</sub>	-40°C to +125°C	All	48	50	%
Minimum duty cycle		COMP = 0 V	-40°C to +125°C	All		0	%
Current sense section							
Gain		4/	-40°C to +125°C	All	1.9	2.5	V/V
Maximum input signal		COMP = 5 V 5/	-40°C to +125°C	All	0.45	0.55	V
CS to output delay		COMP = 3.5 V, CS from 0 mV to 600 mV	-40°C to +125°C	All		200	ns
CS source current			-40°C to +125°C	All	-200		nA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Current sense section - continued.							
CS sink current		CS = 0.5 V, RC = 5.5 <u>6/</u>	-40°C to +125°C	All	4		mA
Over current threshold			-40°C to +125°C	All	0.65	0.85	V
COMP to CS offset		CS = 0 V	-40°C to +125°C	All	0.35	1.2	V
Output section							
OUT low level		I = 100 mA	-40°C to +125°C	All		1.1	V
OUT high level		I = -50 mA, VDD - OUT	-40°C to +125°C	All		1	V
Rise time		CL = 1 nF	-40°C to +125°C	All		60	ns
Fall time		CL = 1 nF	-40°C to +125°C	All		60	ns
Undervoltage lockout section							
Start threshold		<u>7/</u>	-40°C to +125°C	01	11.5	13.5	V
				02	4.1	4.5	
Minimum operating voltage after start			-40°C to +125°C	01	7.6	9	V
				02	3.9	4.3	
Hysteresis			-40°C to +125°C	01	3.5	5.1	V
				02	0.1	0.3	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Soft start section							
COMP rise time		FB = 1.8 V, rise from 0.5 V to 4 V	-40°C to +125°C	All		20	ms
Overall section							
Standup current		VDD < start threshold	-40°C to +125°C	All		260	μA
Operating supply current		FB = 0 V, CS = 0 V <u>7/ 8/</u>	-40°C to +125°C	All		2	mA
VDD zener shunt voltage		I <sub>DD</sub> = 10 mA <u>9/</u>	-40°C to +125°C	All	13	15	V

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise noted, V<sub>DD</sub> = 10 V, 1 μF capacitor from V<sub>DD</sub> to GND, R = 22 kΩ, C = 330 pF, and T<sub>A</sub> = T<sub>J</sub>.

3/ Measured at RC. Signal amplitude tracks V<sub>DD</sub>.

4/ Gain is defined by:  $A = \Delta V_{COMP} / \Delta V_{CS}$ ,  $0 \leq V_{CS} \leq 0.4$  V.

5/ Parameter measured at trip point of latch with FB at 0 V.

6/ The internal current sink on the CS pin is designed to discharge an external filter capacitor. It is not intended to be a dc sink path.

7/ For device type 01, set V<sub>DD</sub> above the start threshold before setting at 10 V.

8/ Does not include current in the external oscillator network.

9/ Start threshold and zener shunt threshold trade one another.

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Case X

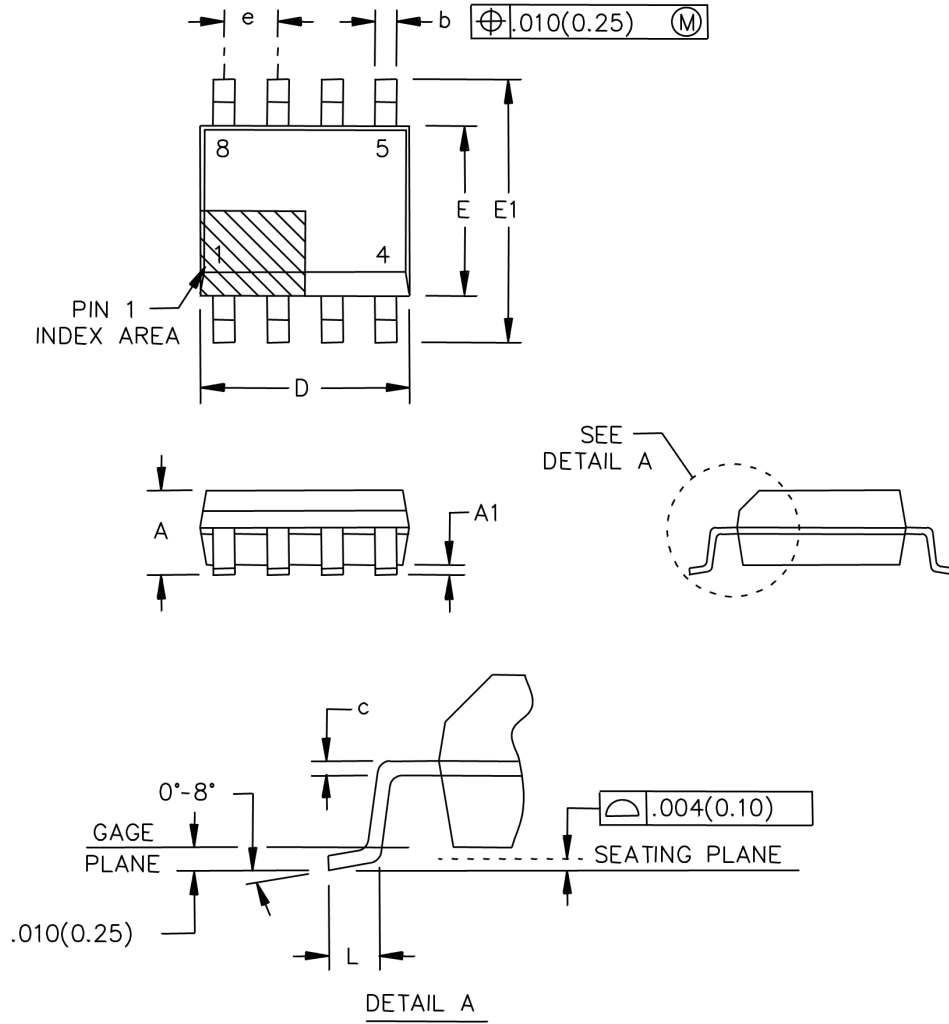


FIGURE 1. Case outline.

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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.014	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
n	8 leads		8 leads	

NOTE:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline. – continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	COMP	COMP is the output of the error amplifier and the input of the PWM comparator.
2	FB	FB is the inverting input of the error amplifier.
3	CS	CS is the input to the pulse width modulator, peak current, and over current comparators.
4	RC	RC is the oscillator programming pin.
5	GND	GND is reference ground and power ground for all functions.
6	OUTB	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500 mA peak-source current, and 1 A peak-sink current.
7	OUTA	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500 mA peak-source current, and 1 A peak-sink current.
8	VDD	VDD is the power input connection for this device.

FIGURE 2. Terminal connections.

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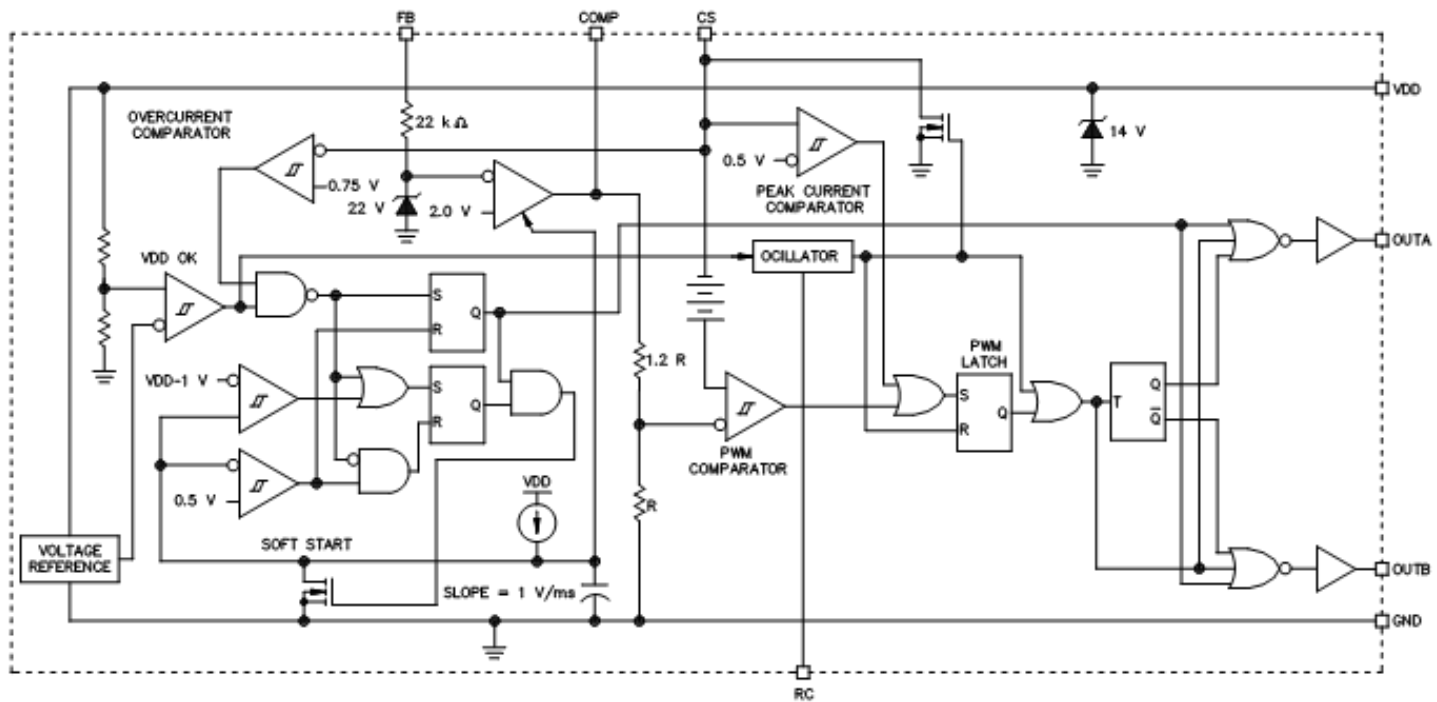


FIGURE 3. Logic diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/ 2/</u>	Device manufacturer CAGE code	Package	Top side marking	Vendor part number
V62/04642-01XE	01295	Tape and reel	UCC2808AQD-1EP	UCC2808AQDR-1EP
V62/04642-02XE	01295	Tape and reel	UCC2808AQD-2EP	UCC2808AQDR-2EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

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