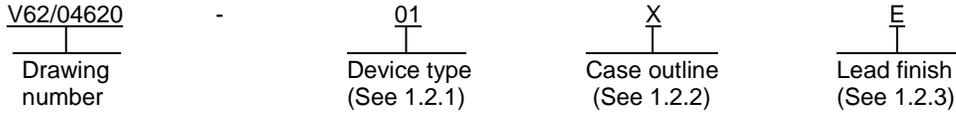




1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal buffer/driver with TTL compatible inputs and 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C for device type 01, and an operating temperature range of -40°C to +85°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74ACT244-EP	Octal buffer/driver with TTL compatible inputs and 3-state outputs
02	SN74ACT244-EP	Octal buffer/driver with TTL compatible inputs and 3-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	JEDEC MS-013	Plastic small-outline
Y	20		Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to +7.0 V
Input voltage range ( $V_i$ ) .....	-0.5 V to $V_{CC} + 0.5$ V 2/
Output voltage range ( $V_o$ ) .....	-0.5 V to $V_{CC} + 0.5$ V 2/
Input clamp current ( $I_{IK}$ ) ( $V_i < 0$ or $V_i > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current ( $I_{OK}$ ) ( $V_o < 0$ or $V_o > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current ( $I_o$ ) ( $V_o = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Package thermal impedance ( $\theta_{JA}$ ) .....	58°C/W 3/
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C 4/

1.4 Recommended operating conditions. 5/

Supply voltage range ( $V_{CC}$ ) .....	4.5 V to 5.5 V
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V
Maximum low level input voltage ( $V_{IL}$ ) .....	0.8 V
Input voltage range ( $V_i$ ) .....	0.0 V to $V_{CC}$
Output voltage range ( $V_o$ ) .....	0.0 V to $V_{CC}$
Maximum high level output current ( $I_{OH}$ ) .....	-24 mA
Maximum low level output current ( $I_{OL}$ ) .....	24 mA
Maximum input transition rise or fall rate ( $\Delta t/\Delta v$ ) .....	8 ns/V
Operating free-air temperature range ( $T_A$ ):	
Device type 01 .....	-55°C to +125°C
Device type 02 .....	-40°C to +85°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 3/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 4/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
- 5/ All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

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### 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Device type	Limits		Unit
					Min	Max	
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	All	4.4		V
			5.5 V		5.4		
		I <sub>OH</sub> = -24 mA, T <sub>A</sub> = 25°C	4.5 V	All	3.86		
				01	3.7		
		I <sub>OH</sub> = -24 mA	4.5 V	02	3.76		
				01	4.7		
		I <sub>OH</sub> = -24 mA, T <sub>A</sub> = 25°C	5.5 V	All	4.86		
02	4.76						
I <sub>OH</sub> = -75 mA 3/	5.5 V	02	3.85				
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V	All		0.1	V
			5.5 V			0.1	
		I <sub>OL</sub> = 24 mA, T <sub>A</sub> = 25°C	4.5 V	All		0.36	
				01		0.5	
		I <sub>OL</sub> = 24 mA	4.5 V	02		0.44	
				All		0.36	
		I <sub>OL</sub> = 24 mA, T <sub>A</sub> = 25°C	5.5 V	01		0.5	
02				0.44			
I <sub>OL</sub> = 75 mA 3/	5.5 V	02		1.65			
Off-state output current	I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, T <sub>A</sub> = 25°C	5.5 V	All		±0.25	μA
				01		±5	
				02		±2.5	
Input current	I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, T <sub>A</sub> = 25°C	5.5 V	All		±0.1	μA
				All		±1	
Quiescent supply current	I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, T <sub>A</sub> = 25°C I <sub>O</sub> = 0 A	5.5 V	All		4	μA
				01		80	
				02		40	
Quiescent supply current delta	ΔI <sub>CC</sub> 4/	T <sub>A</sub> = 25°C One input at 3.4 V, other inputs at GND or V <sub>CC</sub> One input at 3.4 V. Other inputs at GND or V <sub>CC</sub>	5.5 V	All	0.6 TYP		mA
				01		1.6	
				02		1.5	
Input capacitance	C <sub>I</sub>	T <sub>A</sub> = 25°C V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	All	2.5 TYP		pF
Output capacitance	C <sub>O</sub>	T <sub>A</sub> = 25°C V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	All	8 TYP		pF
Power dissipation capacitance per buffer/driver	C <sub>pd</sub>	T <sub>A</sub> = 25°C C <sub>L</sub> = 50 pF f = 1 MHz	5 V	All	45 TYP		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	V <sub>CC</sub>	Device type	Limits		Unit
					Min	Max	
Propagation delay time, A to Y	t <sub>PLH</sub>	T <sub>A</sub> = 25°C See figure 5	4.5 V and 5.5 V	All	2	9	ns
		See figure 5		01	1	10	
				02	1.5	10	
	t <sub>PHL</sub>	T <sub>A</sub> = 25°C See figure 5	4.5 V and 5.5 V	All	2	9	
		See figure 5		01	1	10	
				02	1.5	10	
Output enable time, $\overline{\text{OE}}$ to Y	t <sub>PZH</sub>	T <sub>A</sub> = 25°C See figure 5	4.5 V and 5.5 V	All	1.5	8.5	ns
		See figure 5		01	1	9.5	
				02	1	9.5	
	t <sub>PZL</sub>	T <sub>A</sub> = 25°C See figure 5	4.5 V and 5.5 V	All	2	9.5	
		See figure 5		01	1	11	
				02	1.5	10.5	
Output disable time, $\overline{\text{OE}}$ to Y	t <sub>PHZ</sub>	T <sub>A</sub> = 25°C See figure 5	4.5 V and 5.5 V	All	2	9.5	ns
		See figure 5		01	1	11	
				02	1.5	10.5	
	t <sub>PLZ</sub>	T <sub>A</sub> = 25°C See figure 5	4.5 V and 5.5 V	All	2.5	10	
		See figure 5		01	1	11.5	
				02	2	10.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

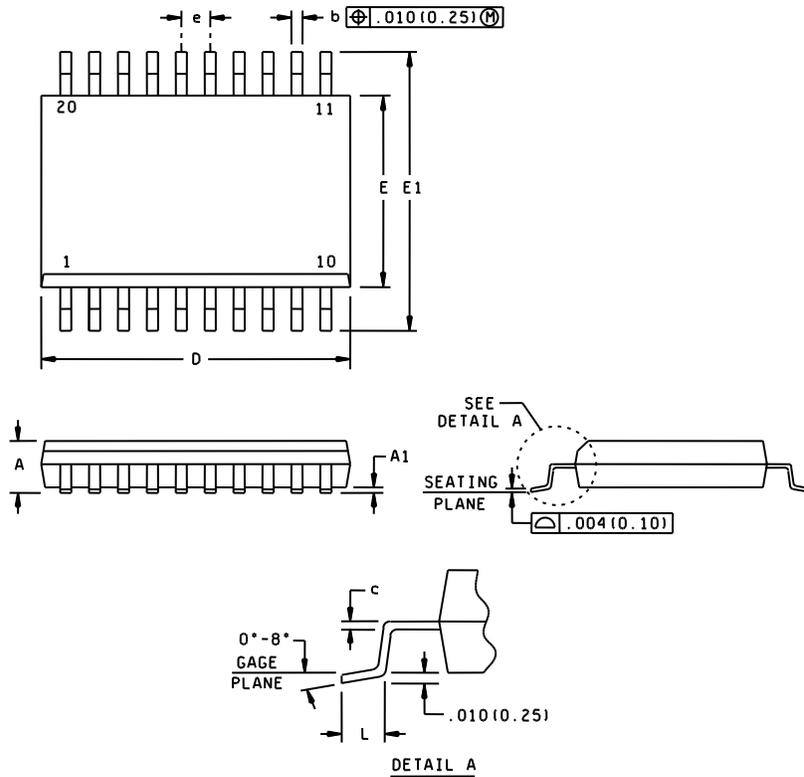
2/ Unless otherwise stated, the operating free-air temperature (T<sub>A</sub>) range for device type 01 is from -55°C to +125°C, and the operating free-air temperature (T<sub>A</sub>) range for device type 02 is from -40°C to +85°C.

3/ Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

4/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

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Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	2.65	---	0.104	E	7.40	7.60	0.291	0.299
A1	0.10	0.30	0.004	0.012	E1	9.97	10.63	0.393	0.419
b	0.31	0.51	0.012	0.020	e	1.27 NOM		0.050 NOM	
c	0.20	0.33	0.008	0.013	L	0.40	1.27	0.016	0.050
D	12.60	13.00	0.496	0.512					

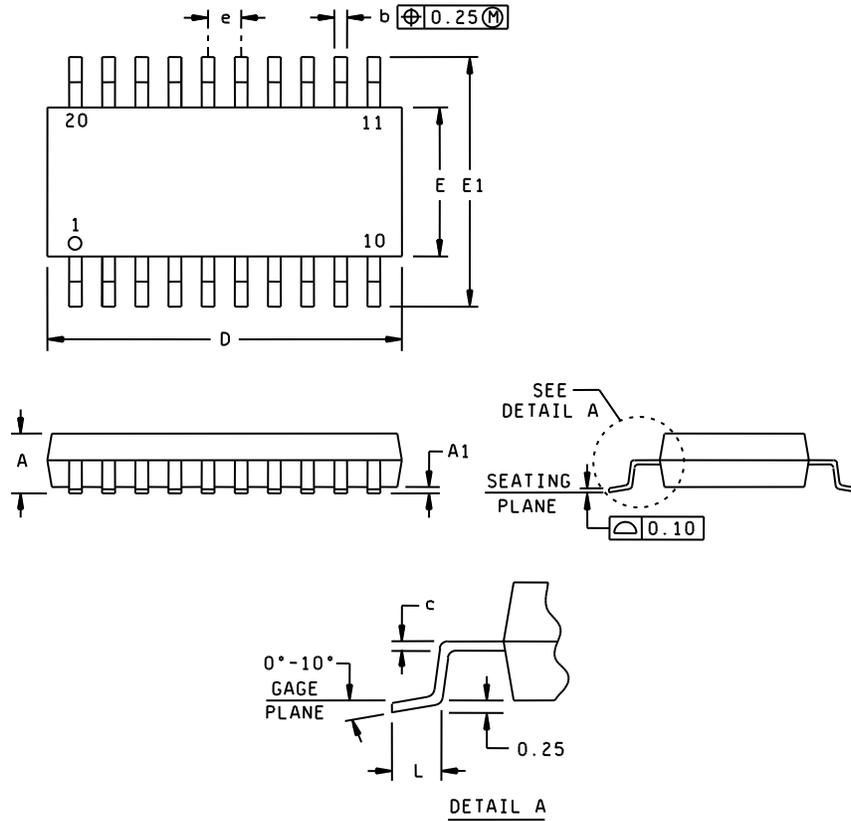
NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-013.

FIGURE 1. Case outline.

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Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	2.00		0.079	E	5.00	5.60	0.197	0.220
A1	0.05	0.15	0.002	0.006	E1	7.40	8.20	0.291	0.323
b	0.35	0.51	0.014	0.020	e	1.27 NOM		0.050 NOM	
c	0.15 NOM		0.006 NOM		L	0.55	1.25	0.022	0.049
D	12.30	12.90	0.484	0.508					

NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).

FIGURE 1. Case outline - Continued.

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(each buffer)

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

FIGURE 2. Truth table.

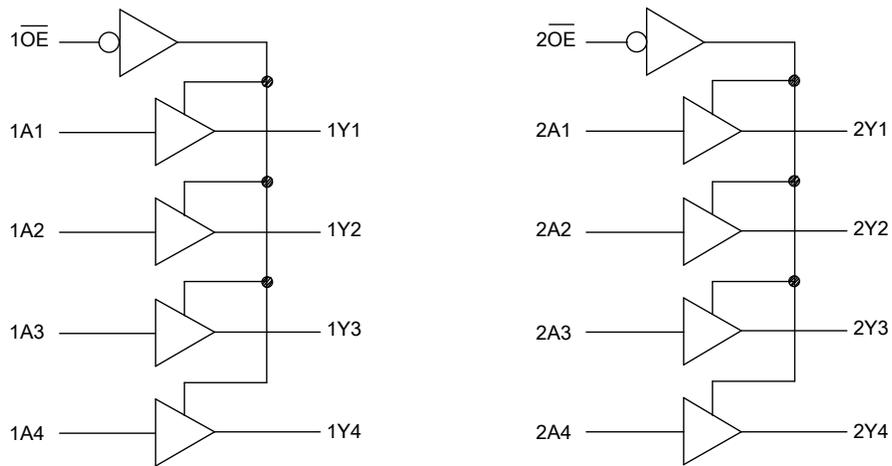
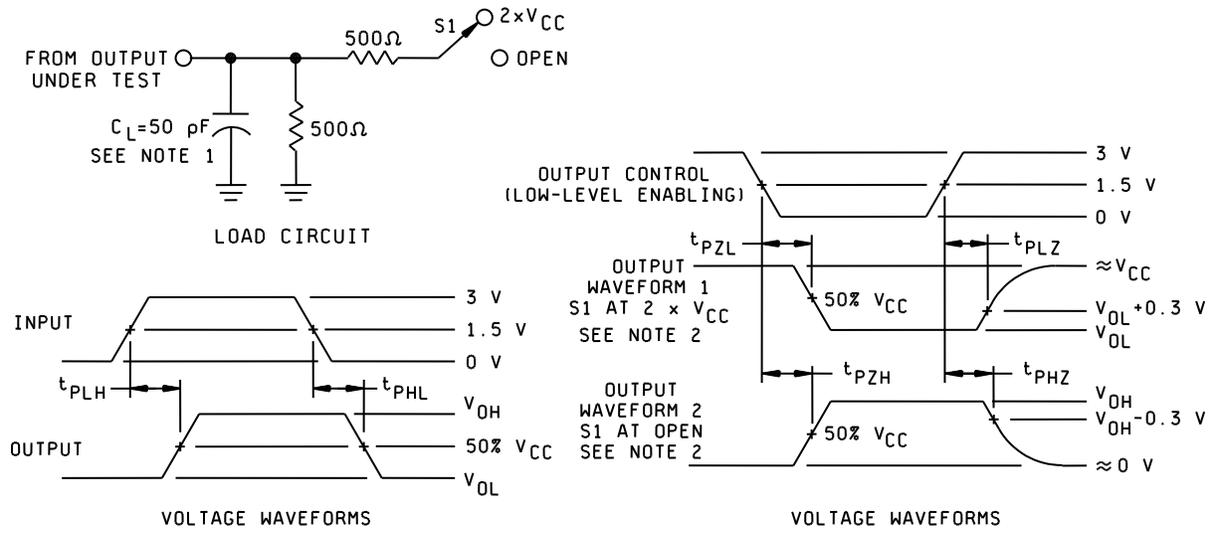


FIGURE 3. Logic diagram.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$1\overline{OE}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	$2\overline{OE}$
10	GND	20	$V_{CC}$

FIGURE 4. Terminal connections.

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NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
4. The outputs are measured one at a time with one input transition per measurement.
5. For 3-state outputs tests:
 

$t_{PLH}/t_{PHL}$	S1 = Open
$t_{PLZ}/t_{PZL}$	S1 = $2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	S1 = Open

FIGURE 5. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/04620-01XE	01295	SN74ACT244MDWREP	SACT244MEP
V62/04620-01YE	01295	SN74ACT244MNSREP	SACT244MEP
V62/04620-02XE	01295	SN74ACT244IDWREP	SACT244IEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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