

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-01-19	Thomas M. Hess

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A	A						
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PMIC N/A	PREPARED BY Phu H. Nguyen		DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990																	
Original date of drawing YY-MM-DD 04-02-18	CHECKED BY Phu H. Nguyen		TITLE MICROCIRCUIT, DIGITAL, IEEE 1394b THREE PORT CABLE TRANSCEIVER/ARBITER, MONOLITHIC SILICON																	
	APPROVED BY Thomas M. Hess																			
	SIZE A	CODE IDENT. NO. 16236		DWG NO. V62/04612																
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance IEEE 1394b Three Port Cable transceiver/arbitrator, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/04612</u> Drawing number	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TSB81BA3-EP	IEEE 1394b Three Port Cable transceiver/arbitrator

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	80	JEDEC MS-026	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 2/

Supply voltage range, (V _{DD})	-0.3 V to +4.0 V 3/
Input voltage range, (V _I)	-0.5 V to V _{DD} + 0.5 V 3/
Output voltage range at any output, (V _O)	-0.5 V to V _{DD} + 0.5 V
Continuous total power dissipation.....	See dissipation rating table.
Operating free air temperature, (T _A).....	-40°C to +85°C
Storage temperature range, (T _{STG}).....	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.
 2/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 3/All voltage values, except differential I/O bus voltage, are with respect to network ground.

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Dissipation Rating Table

Case outline	T _A ≤ 25°C Power rating	Derating Factor <u>4/</u> Above T _A = 25°C	T _A = 70°C Power Rating	T _A = 85°C Power Rating
X <u>5/</u>	5.05 W	52.5 mW/°C	2.69 W	1.9 W
X <u>6/</u>	3.05 W	31.7 mW/°C	1.62 W	1.15 W
X <u>7/</u>	2.01 W	20.3 mW/°C	1.1 W	792 mW

1.4 Recommended operating conditions. 8/

Supply voltage range (3.3 V _{DD})	
Source power node	+3.0 V to +3.6 V
Non source power node <u>9/</u>	+3.0 V to +3.6 V
Supply voltage, (1.8 V _{DD})	+1.85 V to +2.05 V
High level input voltage, (V _{IH})	
LREQ, CTL0, CTL1, D0-D7, LCK	+2.6 V Minimum
LKON/DS2, PC0, PC1, PC2, PD, BMODE	0.7V _{DD} Minimum
RESETz	0.6V _{DD} Minimum
Low level input voltage, (V _{IL})	
LREQ, CTL0, CTL1, D0-D7, LCK	+1.2 V Maximum
LKON/DS2, PC0, PC1, PC2, PD, BMODE	0.2V _{DD} Maximum
RESETz	0.3V _{DD} Maximum
Output current, (I _{OL/OH}) CTL0, CTL1, D0-D7, CAN, LKON/DS2, PINT and PCLK	-4.0 mA to +4.0 mA
Output current, (I _O) TPBIAS outputs	-5.6 mA to 1.3 mA
Maximum junction temperature, (T _J) <u>10/</u>	
R _{θJA} = 19°C/W, T _A = 85°C	+99.1°C
R _{θJA} = 31.5°C/W, T _A = 85°C	+108.4°C
R _{θJA} = 49.2°C/W, T _A = 85°C	+121.5°C
1394b Differential input voltage, (V _{ID})	
Cable inputs, during data reception	+200 mV to +800 mV
1394a Differential input voltage, (V _{ID})	
Cable inputs, during data reception	+118 mV to +260 mV
Cable inputs, during arbitration	+168 mV to +265 mV
1394a Common mode input voltage, (V _{IC})	
TPB cable inputs, source power node	+0.4706 V to 2.515 V
TPB cable inputs, non source power node	+0.4706 V to 2.015 V <u>9/</u>
Power up reset time, (t _{pu}) RESETz input	2 ms Minimum <u>11/</u>
Receiver input jitter	
TPA, TPB cable inputs, S100 operation	±1.08 ns Maximum
TPA, TPB cable inputs, S200 operation	±0.5 ns Maximum
TPA, TPB cable inputs, S400 operation	±0.315 ns Maximum
Receive input skew	
Between TPA and TPB cable inputs, S100 operation	±0.8 ns Maximum
Between TPA and TPB cable inputs, S200 operation	±0.55 ns Maximum
Between TPA and TPB cable inputs, S400 operation	±0.5 ns Maximum

4/ This is the inverse of the traditional junction to ambient thermal resistance (R_{θJA}).

5/ 2 oz. Trace and cooper pad with solder.

6/ 2 oz. Trace and cooper pad without solder.

7/ For more information, see manufacturer package application.

8/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

9/ For a node that does not source power; see Section 4.2.2.2 in IEEE 1394a-2000.

10/ See R_{θJA} values listed in thermal characteristics, table I.

11/ Timer after valid clock received at PHY XI input terminal.

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2. APPLICABLE DOCUMENTS

IEEE Standard 1394b - IEEE Standard for High Speed Serial Buses Allowing Gigabit Signaling.

(Applications for copies should be addressed to the Institute of Electrical and Electronic Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagrams. The block diagrams shall be as specified on figure 3.

3.5.4 Load test circuit. The load test circuit shall be as specified on figure 4.

3.5.5 Timing diagram. The timing diagram shall be as specified on figure 5-6.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 3.0 V ≤ V _{DD} ≤ 3.6 V -40°C ≤ T _A ≤ 125°C unless otherwise specified	Limits		Unit
			Min	Max	
Driver					
Differential output voltage	V _{OD}	56 Ω, See figure 4	172	265	mV
Drive difference current, TPA+, TPA-, TPB+, TPB-	I _{DIFF}	Drivers enabled, speed signaling off	-1.05 <u>1/</u>	1.05 <u>2/</u>	mA
Common mode speed signaling current, TPB+, TPB-	I _{SP200}	S200 speed signaling enabled	-4.84 <u>2/</u>	-2.53 <u>3/</u>	mA
Common mode speed signaling current, TPB+, TPB-	I _{SP400}	S400 speed signaling enabled	-12.4 <u>2/</u>	-8.10 <u>3/</u>	mA
Off state differential voltage	V _{OFF}	Drivers disabled, See figure 4		20	mV
Receiver					
Differential impedance	Z _{ID}	Drivers disabled	4		kΩ
				4	pF
Common mode impedance	Z _{IC}	Drivers disabled	20		kΩ
				24	pF
Receiver input threshold voltage	V _{TH-R}	Drivers disabled	-30	30	mV
Cable bias detect threshold, TPBx cable inputs	V _{TH-CB}	Drivers disabled	0.6	1	V
Positive arbitration comparator threshold voltage	V _{TH+}	Drivers disabled	89	168	mV
Negative arbitration comparator threshold voltage	V _{TH-}	Drivers disabled	-168	-89	mV
Speed signal threshold	V _{TH-SP200}	TPBIAS-TPA common mode voltage, drivers disabled.	49	131	mV
Speed signal threshold	V _{TH-SP400}		314	396	mV
Device					
Supply current 3.3 V _{DD}	I _{DD}	<u>4/</u>	120 Typ		mA
Supply current 1.8 V _{DD}			79 Typ		
Power status threshold, CPS input <u>4/</u>	V _{TH}	400 kΩ resistor <u>5/</u>	4.7	7.5	V
High level output voltage, CTL0, CTL1, D0-D7, CNA, LKON/DS2, PCLK outputs.	V _{OH}	V _{DD} = 3.0 to 3,6 V, I _{OH} = -4 mA	2.8		V
Low level output voltage, CTL0, CTL1, D0-D7, CNA, LKON/DS2, PCLK outputs.	V _{OL}	I _{OL} = 4 mA		0.4	V
Positive peak bus holder current, D0-D7, CTL0-CTL1, LREQ	I _{BH+}	V _{DD} = 3.6 V, V _I = 0 V to V _{DD}	0.05	1	mA
Negative peak bus holder current, D0-D7, CTL0-CTL1, LREQ	I _{BH-}		-1.0	-0.05	
Off state output current, CTL0, CTL1, D0-D7, CNA, LKON/DS2, I/Os	I _{OZ}	V _O = V _{DD} or 0 V		±5	μA
Pullup current, RESETz input	I _{IRST}	V _I = 1.5 V or 0 V	-90	-20	μA
TPBIAS output voltage	V _O	At rated I _O current	1.665	2.015	V

See notes at end of table.

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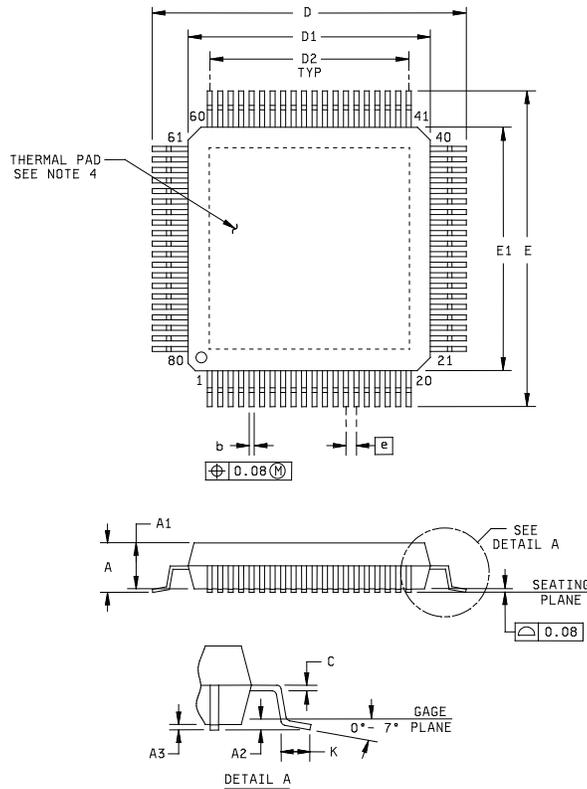
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 3.0 V ≤ V _{DD} ≤ 3.6 V -40°C ≤ T _A ≤ 125°C unless otherwise specified	Limits		Unit
			Min	Max	
Thermal characteristics					
Junction to free air thermal resistance	R _{θJA}	6/	19.04 Typ		°C/W
Junction to case thermal resistance	R _{θJC}		0.17 Typ		
Junction to free air thermal resistance	R _{θJA}	7/	31.52 Typ		
Junction to case thermal resistance	R _{θJC}		0.17 Typ		
Junction to free air thermal resistance	R _{θJA}	8/	49.17 Typ		
Junction to case thermal resistance	R _{θJC}		3.11 Typ		
Switching characteristics					
TP differential rise time, transmit	t _r	10% to 90%, At 1394 connector	0.5	1.2	ns
TP differential fall time, transmit	t _f	90% to 10%, At 1394 connector	0.5	1.2	
Setup time, CTL0, CTL1, D1-D7, LREQ to PCLK	1394a-2000	t _{su}	50% to 50% See figure 5		2.5
Hold time, CTL0, CTL1, D1-D7, LREQ after PCLK	1394a-2000	t _h			0
Setup time, CTL0, CTL1, D1-D7, LREQ to LCLK	1394b	t _{su}			2.5
Hold time, CTL0, CTL1, D1-D7, LREQ after LCLK	1394b	t _h			0
Delay time, PCLK to CTL0, CTL1, D1-D7, PINT	1394a-2000 and 1394b	t _d	50% to 50% See figure 6	0.5	7

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Limits defined as algebraic sum of TPA+ and TPA- driver currents. Limits also apply to TPB+ and TPB- algebraic sum of driver currents.
- 3/ Limits defined as absolute limit of each of TPB+ and TPB- driver currents.
- 4/ Repeat Max Packet (1 port receiving maximum size isochronous packet-8192 bytes, sent on every isochronous interval, s800, data value of 0xCCCCCCCC; 2 ports repeating; all ports with beta mode connection), V_{DD3.3} = 3.3 V, V_{DD1.8} = 1.95 V, T_A = 25°C.
- 5/ Measured at cable power side of resistor.
- 6/ Board mounted, no air flow, high conductivity manufacturer recommended test board, chip soldered or greased to thermal land with 2 oz. copper.
- 7/ Board mounted, no air flow, high conductivity manufacturer recommended test board with thermal land but no solder or greased thermal connection to thermal land with 2 oz. copper.
- 8/ Board mounted, no air flow, high conductivity JEDEC test board with 1 oz. copper.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	13.80	14.20
A1	0.95	1.05	D1/E1	11.80	12.20
A2	0.25 TYP		D2	9.50 TYP	
A3	0.05	0.15	e	0.50 BSC	
b	0.17	0.27	K	0.45	0.75
c	0.13 NOM				

Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusions.
4. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
5. Falls within JEDEC MO-026.

FIGURE 1. Case outline.

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Case X

Pin No.	Terminal name	Pin No.	Terminal name	Pin No.	Terminal name	Pin No.	Terminal name
1	PINT	21	AGND	41	TPB0-	61	AGND
2	LKON/DS2	22	R1	42	TPB0+	62	AGND
3	LREQ	23	R0	43	AGND	63	AV _{DD-3.3}
4	DGND	24	AV _{DD-3.3}	44	AV _{DD-3.3}	64	DGND
5	PCLK	25	PLL _{GND}	45	TPA0-	65	DV _{DD-1.8}
6	DV _{DD-3.3}	26	RSVD	46	TPA0+	66	PC0
7	LCLK	27	XI	47	TPBIAS0	67	PC1
8	DV _{DD-1.8}	28	PLL _{GND}	48	TPB1-	68	PC2
9	CTL0	29	PLL _{V_{DD-1.8}}	49	TPB1+	69	DV _{DD-3.3}
10	CTL1	30	PLL _{V_{DD-1.8}}	50	AGND	70	DV _{DD-3.3}
11	D0	31	PLL _{V_{DD-3.3}}	51	AV _{DD-3.3}	71	DV _{DD-1.8}
12	D1	32	DS1	52	TPA1-	72	DGND
13	D2	33	DS0	53	TPA1+	73	TESTW
14	DGND	34	CPS	54	TPBIAS1	74	BMODE
15	D3	35	SE	55	TPB2-	75	RESETz
16	D4	36	SM	56	TPB2+	76	DGND
17	D5	37	DV _{DD-1.8}	57	AV _{DD-3.3}	77	PD
18	DV _{DD-3.3}	38	DGND	58	TPA2-	78	TESTM
19	D6	39	AV _{DD-3.3}	59	TPA2+	79	CAN
20	D7	40	AGND	60	TPBIAS2	80	LPS

FIGURE 2. Terminal connections.

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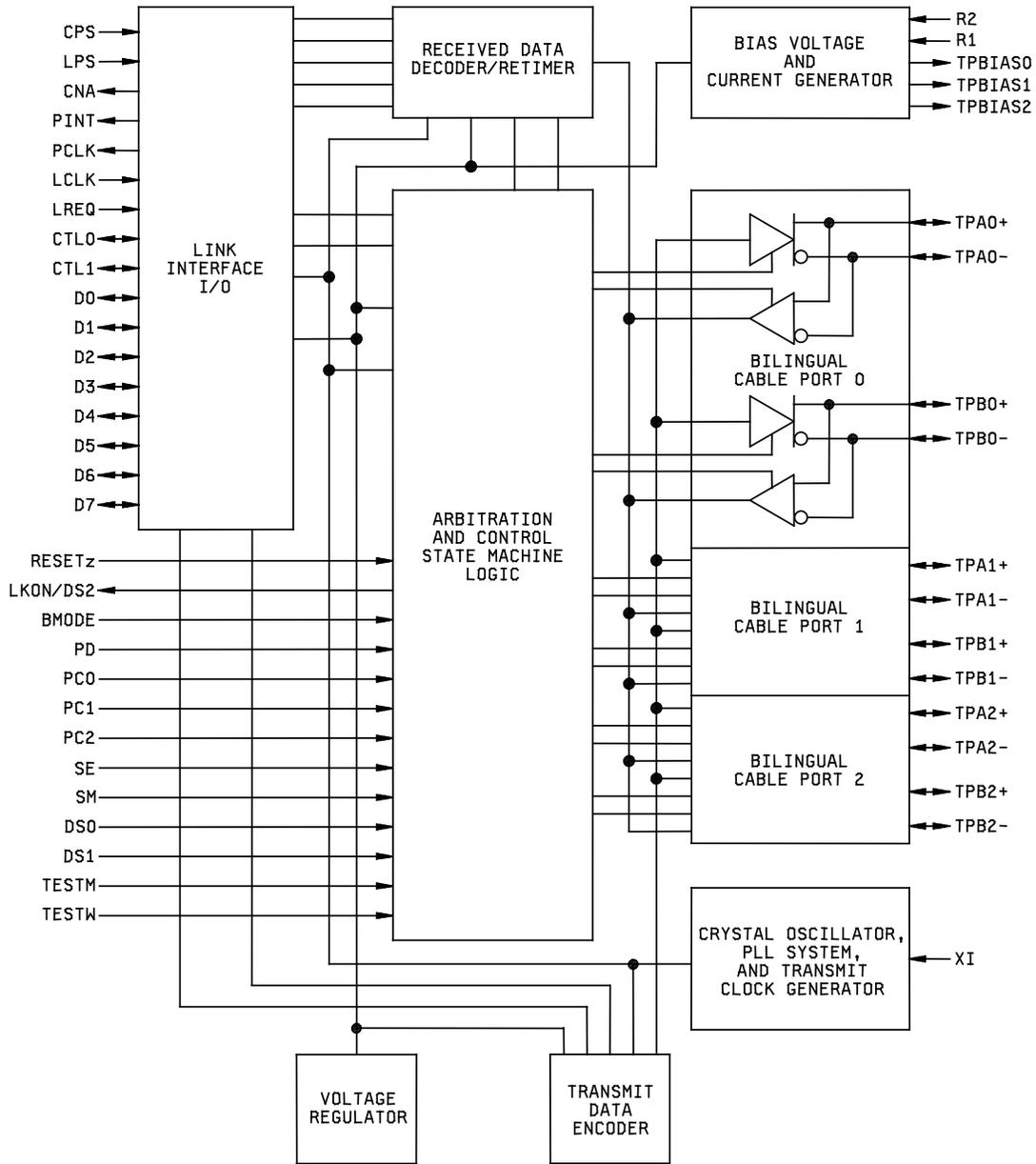


FIGURE 3. Block diagrams.

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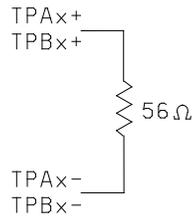


FIGURE 4. Load test circuit.

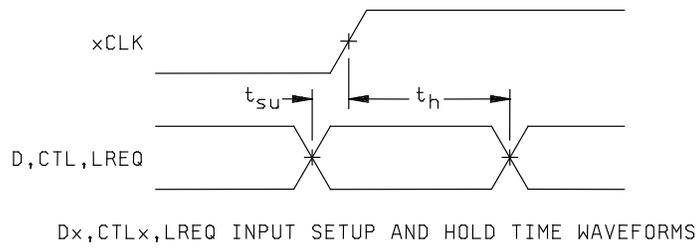


FIGURE 5. Timing diagram.

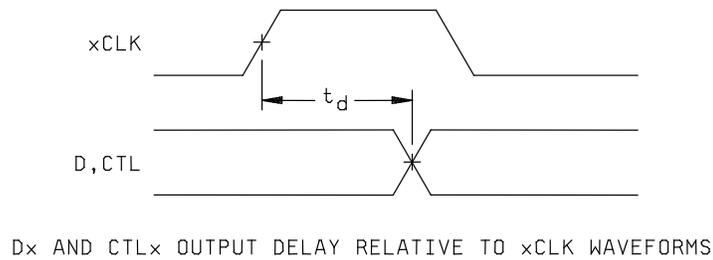


FIGURE 6. Timing diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/04612-01XE	01295	TSB81BA3IPFPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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