

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	10-01-19	Thomas M. Hess

Prepared in accordance with ASME Y14.24

Vendor item drawing

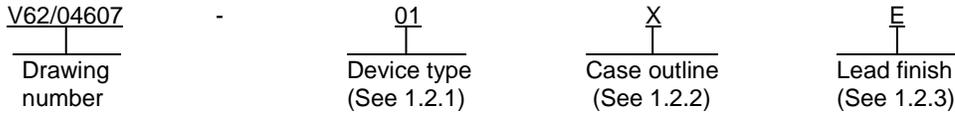
REV	A	A	A	A																		
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PMIC N/A	PREPARED BY Phu H. Nguyen	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990
Original date of drawing  YY MM DD  04-02-11	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, DIGITAL, FIXED POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	DWG NO.  <b>V62/04607</b>
	SIZE <b>A</b>	CODE IDENT. NO. <b>16236</b>
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Fixed-Point Digital Signal Processor microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SM320VC5421-EP	Fixed Point Digital Signal Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>Package style</u>
X	144	Low Profile Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 2/

Supply voltage I/O range, (DV <sub>DD</sub> ) .....	-0.5 V to +4.0 V
Supply voltage core range, (CV <sub>DD</sub> ) .....	-0.5 V to +2.4 V
Supply voltage analog PLL range, (AV <sub>DD</sub> ) .....	-0.5 V to +2.4 V
Input voltage range, (V <sub>I</sub> ) .....	-0.5 V to DV <sub>DD</sub> +0.5 V
Output voltage range (V <sub>O</sub> ) .....	-0.5 V to DV <sub>DD</sub> +0.5 V
Operating case temperature ranges, (T <sub>C</sub> ) .....	-40°C to +85°C
Storage temperature range, (T <sub>STG</sub> ).....	-65°C to +150°C

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.  
 2/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to V<sub>SS</sub>.

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1.4 Recommended operating conditions. 3/ 4/

Device supply voltage, I/O (DV <sub>DD</sub> ) .....	+3.0 V to +3.6 V
Device supply voltage, core (CV <sub>DD</sub> ) .....	+1.75 V to +1.98 V
Device supply voltage, PLL (AV <sub>DD</sub> ) .....	+1.75 V to +1.98 V
Supply voltage, GND (V <sub>SS</sub> ) .....	0 V
High level input voltage, I/O (V <sub>IH</sub> ):	
Schmitt triggered inputs, DV <sub>DD</sub> = 3.3 ±0.3 V .....	0.7DV <sub>DD</sub> to DV <sub>DD</sub>
All other inputs .....	2.0 V to DV <sub>DD</sub>
Low level input voltage, I/O (V <sub>IL</sub> ):	
Schmitt triggered inputs, DV <sub>DD</sub> = 3.3 ±0.3 V .....	0 V to 0.3DV <sub>DD</sub>
All other inputs .....	0 V to + 0.8 V
High level output current, (I <sub>OH</sub> ) .....	-300 µA maximum
Low level output current, (I <sub>OL</sub> ) .....	1.5 mA maximum
Operating case temperature (T <sub>c</sub> ) .....	-40°C to +85°C
Junction to case (R <sub>θJC</sub> ) .....	5°C/W
Junction to air (R <sub>θJA</sub> ) .....	56°C/W

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 Load circuit. The load circuit shall be as specified in figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figure 5-25.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit	
			Min	Max		
High level output voltage 2/	V <sub>OH</sub>	DV <sub>DD</sub> = 3.3 ±0.3 V, I <sub>OH</sub> = Max	2.4		V	
Low level output voltage 2/	V <sub>OL</sub>	I <sub>OL</sub> = Max		0.4	V	
Input current in high impedance	I <sub>Iz</sub>	DV <sub>DD</sub> = Max, V <sub>I</sub> = V <sub>SS</sub> to DV <sub>DD</sub>	-10	10	μA	
Input current (V <sub>I</sub> = V <sub>SS</sub> to DV <sub>DD</sub> )	TRST	I <sub>I</sub>	With internal pulldown	-10	35	
	See pin descriptions		With internal pullups	-35	10	
	PPD[15:0]		Bus holders enabled, DV <sub>DD</sub> = Max 3/	-200	200	
	All other input only pins			-10	10	
Supply current, both core CPUs	I <sub>DDC</sub>	CV <sub>DD</sub> = 1.8 V, T <sub>C</sub> = 25°C f <sub>X</sub> = 100 MHz 4/	90 TYP 5/		mA	
Supply current, pins	I <sub>DDP</sub>	DV <sub>DD</sub> = 3.3 V, f <sub>CLK</sub> = 100 MHz 5/ T <sub>C</sub> = 25°C 6/	54 TYP		mA	
Supply current, PLL	I <sub>DDA</sub>		5 TYP		mA	
Supply current, standby	IDLE2	I <sub>DDC</sub>	PLL x n mode, 20 MHz input	2 TYP		mA
	IDLE3		PLL x n mode, 20 MHz input	600 TYP		μA
Input capacitance	C <sub>I</sub>		10 TYP		pF	
Output capacitance	C <sub>O</sub>		10 TYP		pF	

**CLOCK OPTION**

**Divide by 2 and divide by 4 clock options timing requirements**

Cycle time, CLKIN	t <sub>c(CI)</sub>	See figure 5	20	7/	ns
Fall time, CLKIN	t <sub>f(CI)</sub>			8	
Rise time, CLKIN	t <sub>r(CI)</sub>			8	
Pulse duration, CLKIN low	t <sub>w(CIL)</sub>		5		
Pulse duration, CLKIN high	t <sub>w(CIH)</sub>		5		

**Divide by 2 and divide by 4 clock options switching characteristics 8/**

Cycle time, CLKOUT	t <sub>c(CO)</sub>	See figure 5	40	7/	ns
Cycle time, CLKOUT – bypass mode	t <sub>c(CO)</sub>		40	7/	
Delay time, CLKIN high to CLKOUT high/low	t <sub>d(CIH-CO)</sub>		3	10	
Fall time, CLKOUT	t <sub>f(CO)</sub>		2 Typ		
Rise time, CLKOUT	t <sub>r(CO)</sub>		2 Typ		
Pulse duration, CLKOUT low	t <sub>w(COL)</sub>		H-2	H+2	
Pulse duration, CLKOUT high	t <sub>w(COH)</sub>		H-2	H+2	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	

**CLOCK OPTION – (CONTINUED).**

**Multiply by N clock option timing requirements 8/**

Cycle time, CLKIN	Integer PLL multiplier N (N = 1-15) 9/	t <sub>c(CI)</sub>	See figure 6	20 9/	200	ns
	PLL multiplier N = x.5 9/			20 9/	100	
	PLL multiplier N = x.5, x.75 9/			20 9/	50	
Fall time, CLKIN		t <sub>f(CI)</sub>			8	
Rise time, CLKIN		t <sub>r(CI)</sub>			8	
Pulse duration, CLKIN low		t <sub>W(CIL)</sub>		5		
Pulse duration, CLKIN high		t <sub>W(CIH)</sub>		5		

**Multiply by N clock option switching characteristics 8/**

Cycle time, CLKOUT	t <sub>c(CO)</sub>	See figure 6	10		ns
Delay time, CLKIN high/low to CLKOUT high/low	t <sub>d(CI-CO)</sub>		4	16	
Fall time, CLKOUT	t <sub>f(CO)</sub>		2 Typ		
Rise time, CLKOUT	t <sub>r(CO)</sub>		2 Typ		
Pulse duration, CLKOUT low	t <sub>W(COL)</sub>		H-2	H+2	
Pulse duration, CLKOUT high	t <sub>W(COH)</sub>		H-2	H+2	
Transitory phase, PLL lock up time	t <sub>p</sub>			30	

**EXTERNAL MEMORY INTERFACE TIMING**

**Memory read timing requirements 14/**

Access time, read data access from address valid 11/	t <sub>a(A)M</sub>	See figure 7		2H-12	ns
Access time, read data access from $\overline{\text{MSTRB}}$ low	t <sub>a(MSTRBL)</sub>			2H-11	
Setup time, read data before CLOCKOUT low	t <sub>su(D)R</sub>		9		
Hold time, read data after CLOCKOUT low	t <sub>h(D)R</sub>		0		
Hold time, read data after address invalid	t <sub>h(A-D)R</sub>		0		
Hold time, read data after $\overline{\text{MSTRB}}$ high	t <sub>h(D)MSTRBH</sub>		0		

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	
<b>EXTERNAL MEMORY INTERFACE TIMING (CONTINUED)</b>					
<b>Memory read switching characteristics</b>					
Delay time, CLKOUT low to address valid <u>11/ 12/</u>	t <sub>d</sub> (CLKL-A)	See figure 7	-1	5	ns
Delay time, CLKOUT high (transaction) to address valid <u>11/ 13/</u>	t <sub>d</sub> (CLKH-A)		-1	6	
Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low	t <sub>d</sub> (CLKL-MSL)		-1	4	
Delay time, CLKOUT $\overline{\text{MSTRB}}$ high	t <sub>d</sub> (CLKL-MSH)		-1	4	
Hold time, address valid after CLKOUT low <u>11/ 12/</u>	t <sub>h</sub> (CLKL-A)R		-1	5 <u>13/</u>	
Hold time, address valid after CLKOUT lhigh <u>11/ 13/</u>	t <sub>h</sub> (CLKH-A)R		-1	6 <u>13/</u>	
<b>Memory write switching characteristics <u>14/</u></b>					
Delay time, CLKOUT high to address valid <u>11/ 15/</u>	t <sub>d</sub> (CLKH-A)	See figure 8	-1	6	ns
Delay time, CLKOUT low to address valid <u>11/ 16/</u>	t <sub>d</sub> (CLKL-A)		-1	5	
Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low	t <sub>d</sub> (CLKL-MSL)		-1	4	
Delay time, CLKOUT low to data valid	t <sub>d</sub> (CLKL-D)W		0	7	
Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high	t <sub>d</sub> (CLKL-MSH)		-1	4	
Delay time, CLKOUT high to R/ $\overline{\text{W}}$ low	t <sub>d</sub> (CLKH-RWL)		0	4	
Delay time, CLKOUT high to R/ $\overline{\text{W}}$ high	t <sub>d</sub> (CLKH-RWH)		0	4	
Delay time, R/ $\overline{\text{W}}$ low to $\overline{\text{MSTRB}}$ low	t <sub>d</sub> (RWL-MSTRBL)		H-2	H+2	
Hold time, address valid after CLKOUT high <u>11/ 16/</u>	t <sub>h</sub> (A)W		-1	6	
Hold time, write data valid after $\overline{\text{MSTRB}}$ high	t <sub>h</sub> (D)MSH		H-3	H+3 <u>16/</u>	
Pulse duration, $\overline{\text{MSTRB}}$ low <u>16/</u>	t <sub>w</sub> (SL)MS		2H-4		
Setup time, address valid before $\overline{\text{MSTRB}}$ low <u>11/</u>	t <sub>su</sub> (A)W		2H-4		
Setup time, write data valid before $\overline{\text{MSTRB}}$ high	t <sub>su</sub> (D)MSH		2H-5	2H+5 <u>16/</u>	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	
<b>READY TIMING FOR EXTERNALLY GENERATED WAIT STATES</b>					
<b>Ready timing requirements for externally generated wait states 8/ 17/</b>					
Setup time, READY before CLKOUT low	t <sub>su</sub> (RDY)	See figure 9	8		ns
Hold time, READY after CLKOUT low	t <sub>h</sub> (RDY)		0		
Valid time, READY after $\overline{\text{MSTRB}}$ low 18/	t <sub>v</sub> (RDY)MSTRB			2H-8	
Hold time, READY after $\overline{\text{MSTRB}}$ low 18/	t <sub>h</sub> (RDY)MSTRB		2H		
<b>PARALLEL I/O INTERFACE TIMING</b>					
<b>Parallel I/O port read timing requirements 14/</b>					
Access time, read data access from address valid 19/	t <sub>a</sub> (A)IO	See figure 10		3H-12	ns
Access time, read data access from $\overline{\text{IOSTRB}}$ low	t <sub>a</sub> (ISTRBL)IO			2H-11	
Setup time, read data before CLKOUT high	t <sub>su</sub> (D)IOR		9		
Hold time, read data after CLKOUT high	t <sub>h</sub> (D)IOR		0		
Hold time, read data after $\overline{\text{IOSTRB}}$ high	t <sub>h</sub> (ISTRBH-D)R		0		
<b>Parallel I/O port read switching characteristics</b>					
Delay time, CLKOUT low to address valid 19/	t <sub>d</sub> (CLKL-A)	See figure 10	-1	5	ns
Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ low	t <sub>d</sub> (CLKH-ISTRBL)		0	5	
Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ high	t <sub>d</sub> (CLKH-ISTRBH)		0	5	
Hold time, address after CLKOUT low 19/	t <sub>h</sub> (A)IOR		-1	5	
<b>Parallel I/O port write switching characteristics</b>					
Delay time, CLKOUT low to address valid 19/	t <sub>d</sub> (CLKL-A)	See figure 11	-1	5	ns
Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ low	t <sub>d</sub> (CLKH-ISTRBL)		0	5	
Delay time, CLKOUT high to write data valid	t <sub>d</sub> (CLKH-D)IOW		H-5	H+5	
Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ high	t <sub>d</sub> (CLKH-ISTRBH)		0	5	
Delay time, CLKOUT low R/ $\overline{\text{W}}$ low	t <sub>d</sub> (CLKL-RWL)		0	4	
Delay time, CLKOUT low R/ $\overline{\text{W}}$ high	t <sub>d</sub> (CLKL-RWH)		0	4	
Hold time, address valid after CLKOUT low 19/	t <sub>h</sub> (A)IOW		-1	5	
Hold time, write data after $\overline{\text{IOSTRB}}$ high	t <sub>h</sub> (D)IOW		H-3	H+7	
Setup time, write data before $\overline{\text{IOSTRB}}$ high	t <sub>su</sub> (D)IOSTRBH		H-5	H+1	
Setup time, address valid before $\overline{\text{IOSTRB}}$ low 19/	t <sub>su</sub> (A)IOSTRBL		H-5	H+3	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	

**EXTERNAL GENERATED WAIT STATES**

**Externally generated wait state timing requirements** 8/ 20/

Test	Symbol	Test condition	Min	Max	Unit
Setup time, READY before CLKOUT low	t <sub>su</sub> (RDY)	See figure 12	8		ns
Hold time, READY after CLKOUT low	t <sub>h</sub> (RDY)		0		
Valid time, READY after IOSTRB low <u>18/</u>	t <sub>v</sub> (RDY)IOSTRB			3H-9	
Hold time, READY after IOSTRB low <u>18/</u>	t <sub>h</sub> (RDY)IOSTRB		3H		

**RESET,  $\overline{\text{BIO}}$ , INTERRUPT, AND MP/MC TIMINGS**

**Reset,  $\overline{\text{BIO}}$ , interrupt, and MP/MC timing requirements** 8/

Test	Symbol	Test condition	Min	Max	Unit
Hold time, $\overline{\text{RS}}$ after CLKOUT low	t <sub>h</sub> (RS)	See figure 13	0		ns
Hold time, $\overline{\text{BIO}}$ after CLKOUT low	t <sub>h</sub> (BIO)		0		
Hold time, $\overline{\text{INTn}}$ , $\overline{\text{NMI}}$ after CLKOUT low <u>21/</u>	t <sub>h</sub> (INT)		0		
Pulse duration, $\overline{\text{RS}}$ low <u>22/</u> <u>23/</u>	t <sub>w</sub> (RSL)		4H+5		
Pulse duration, $\overline{\text{BIO}}$ low, asynchronous <u>21/</u>	t <sub>w</sub> (BIO)A		5H		
Pulse duration, $\overline{\text{INTn}}$ , $\overline{\text{NMI}}$ high (asynchronous) <u>21/</u>	t <sub>w</sub> (INT)A		4H		
Pulse duration, $\overline{\text{INTn}}$ , $\overline{\text{NMI}}$ low (asynchronous) <u>21/</u>	t <sub>w</sub> (INTL)A		4H		
Pulse duration, $\overline{\text{INTn}}$ , $\overline{\text{NMI}}$ low for IDLE2/IDLE3 wakeup <u>21/</u>	t <sub>w</sub> (INTL)WKP		8		
Pulse duration, XIO switched	t <sub>w</sub> (XIO)		4H		
Enable time, after XIO switched	t <sub>en</sub> (XIO)			4H+10	
Setup time, $\overline{\text{RS}}$ before CLKIN low <u>23/</u>	t <sub>su</sub> (RS)		5		
Setup time, $\overline{\text{BIO}}$ before CLKOUT low	t <sub>su</sub> (BIO)		9	12	
Setup time, $\overline{\text{INTn}}$ , $\overline{\text{NMI}}$ , $\overline{\text{RS}}$ before CLKOUT low	t <sub>su</sub> (INT)		9	13	

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	
<b>HOLD AND HOLDA TIMINGS</b>					
<u>HOLD and HOLDA timing requirements</u> 8/					
Pulse duration, $\overline{\text{HOLD}}$ low	t <sub>w(HOLD)</sub>	See figure 14	4H+10		ns
Setup time, $\overline{\text{HOLD}}$ low/high before CLKOUT low	t <sub>su(HOLD)</sub>		8		
<u>HOLD and HOLDA switching characteristics</u> 8/					
Disable time, address, $\overline{\text{PS}}$ , $\overline{\text{DS}}$ , $\overline{\text{IS}}$ high impedance from CLKOUT high	t <sub>dis(CLKL-A)</sub>	See figure 14		5	ns
Disable time, R/ $\overline{\text{W}}$ high impedance from CLKOUT high	t <sub>dis(CLKL-RW)</sub>			5	
Disable time, $\overline{\text{MSTRB}}$ , $\overline{\text{IOSTRB}}$ high impedance from CLKOUT high	t <sub>dis(CLKL-S)</sub>			5	
Disable time, data from CLKOUT high	t <sub>dis(CLKL-D)</sub>			5	
Enable time, address, $\overline{\text{PS}}$ , $\overline{\text{DS}}$ , $\overline{\text{IS}}$ from CLKOUT high	t <sub>en(CLKL-A)</sub>			2H+5	
Enable time, data from CLKOUT high	t <sub>en(CLKL-D)</sub>			2H+5	
Enable time, R/ $\overline{\text{W}}$ enable from CLKOUT high	t <sub>en(CLKL-RW)</sub>			2H+5	
Enable time, $\overline{\text{MSTRB}}$ , $\overline{\text{IOSTRB}}$ enable from CLKOUT high	t <sub>en(CLKL-S)</sub>		1	2H+5	
Delay time, $\overline{\text{HOLDA}}$ low after CLKOUT high	t <sub>d(HOLDAL)</sub>		0	11H+5	
Delay time, $\overline{\text{HOLDA}}$ high after CLKOUT high	t <sub>d(HOLDAH)</sub>		0	5	
Pulse duration, $\overline{\text{HOLDA}}$ low duration	t <sub>w(HOLDA)</sub>		2H-3		

See notes at end of table.

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Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	
<b>EXTERNAL FLAG (XF) AND TOUT TIMINGS</b>					
<b>External flag (XF) and TOUT switching characteristics</b> 8/					
Delay time, CLKOUT low to XF high	t <sub>d(XF)</sub>	See figure 15	-1	4	ns
Delay time, CLKOUT low to XF low			0	4	
Delay time, CLKOUT high to TOUT high	t <sub>d(TOUTH)</sub>		-1	5	
Delay time, CLKOUT high to TOUT low	t <sub>d(TOUTL)</sub>		-1	5	
Pulse duration, TOUT	t <sub>w(TOUT)</sub>		2H-5	2H+2	
<b>GENERAL PURPOSE I/O TIMING</b>					
<b>General purpose I/O timing requirements</b>					
Setup time, GPIOx input valid before CLKOUT high, GPIOx configured as general purpose input	t <sub>su(GPIO-COH)</sub>	See figure 16	7		ns
Hold time, GPIOx input valid after CLKOUT high, GPIOx configured as general purpose input	t <sub>h(GPIO-COH)</sub>		0		
<b>General purpose I/O switching characteristics</b>					
Delay time, CLKOUT high to GPIOx output change. GPIOx configured as general purpose output	t <sub>d(COH-GPIO)</sub>	See figure 16	-1	5	ns

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	
<b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING</b>					
<b>McBSP transmit and receive timing requirements</b> 8/ 24/					
Cycle time, BCLKR/X	t <sub>c</sub> (BCKRX)	See figure 17	BCLKR/X ext	4H	ns
Pulse duration, BCLKR/X low or BCLKR/X high	t <sub>w</sub> (BCKRX)		BCLKR/X ext	6	
Hold time, external BFSR high after BCLKR low	t <sub>h</sub> (BCKRL-BFRH)		BCLKR int	0	
			BCLKR ext	4	
Hold time, BDR valid after BCLKX low	t <sub>h</sub> (BCKRL-BDRV)		BCLKR int	0	
			BCLKR ext	5	
Hold time, external BFSX high after BCLKX low	t <sub>h</sub> (BCKXL-BFXH)		BCLKR int	0	
			BCLKR ext	4	
Setup time, external BFSR high before BCLKR low	t <sub>su</sub> (BFRH-BCKRL)		BCLKR int	10	
			BCLKR ext	4	
Setup time, BDR valid before BCLKR low	t <sub>su</sub> (BDRV-BCKRL)		BCLKR int	10	
			BCLKR ext	3	
Setup time, external BFSX high before BCLKX low	t <sub>su</sub> (BFXH-BCKXL)		BCLKR int	10	
			BCLKR ext	6	
Rise time, BCLKR/X	t <sub>r</sub> (BCKRX)	BCLKR/X ext		8	
Fall time, BCLKR/X	t <sub>f</sub> (BCKRX)	BCLKR/X ext		8	

See notes at end of table.

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Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit	
			Min	Max		
<b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING (CONTINUED)</b>						
<b>McBSP transmit and receive switching characteristics</b> <u>8/</u> <u>24/</u>						
Cycle time, BCLKR/X	t <sub>c</sub> (BCKRX)	See figure 17	BCLKR/X int	4H		ns
Pulse duration , BCLKR/X high	t <sub>w</sub> (BCKRXH)		BCLKR/X int	D-4 <u>24/</u>	D+1 <u>24/</u>	
Pulse duration, BCLKR/X low	t <sub>w</sub> (BCKRXL)		BCLKR/X int	C-4 <u>24/</u>	C+1 <u>24/</u>	
Delay time, BCLKR high to internal BFSR valid	t <sub>d</sub> (BCKRH-BFRV)		BCLKR int	-3	3	
Delay time, BCLKX high to internal BFSX valid	t <sub>d</sub> (BCKXH-BFXV)		BCLKR int	-3	8	
Disable time, BCLKX high to BDX high impedance following last data bit	t <sub>dis</sub> (BCKXH-BDXHZ)		BCLKR ext	2	15	
			BCLKR int	-8	3	
Delay time, BCLKX high to BDX valid. This applies to all bits except the first bit transmitted	t <sub>d</sub> (BCKXH-BDXV)		BCLKR ext	1	12	
			BCLKR int	-1	11	
Delay time, BCLKX high to BDX valid <u>26/</u> DXENA = 0	t <sub>d</sub> (BCKXH-BDXV)		BCLKR ext	4	20	
			BCLKR int		11	
Only applies to first bit transmitted when in data delay 1 or 2 (XDATDLY = 01b or 10b) modes DXENA = 1	t <sub>d</sub> (BCKXH-BDXV)		BCLKR ext		20	
			BCLKR int		4H+6	
Enable time, BCLKX high to BDX driven <u>26/</u> Only applies to first bit transmitted when in data delay 1 or 2 (XDATDLY = 01b or 10b) modes DXENA = 0	t <sub>en</sub> (BCKXH-BDX)		BCLKR ext		4H+15	
		BCLKR int	5			
DXENA = 1	t <sub>en</sub> (BCKXH-BDX)	BCLKR ext	16			
		BCLKR int	4H			
Delay time, BFSX high to BDX valid <u>26/</u> Only applies to first bit transmitted when in data delay 0 (XDATDLY = 00b) mode DXENA = 0	t <sub>d</sub> (BFXH-BDXV)	BCLKR ext	4H+12			
		BFSX int		9		
DXENA = 1	t <sub>d</sub> (BFXH-BDXV)	BFSX ext		15		
		BFSX int		4H		
Enable time, BFSX high to BDX driven <u>26/</u> Only applies to first bit transmitted when in data delay 0 (XDATDLY = 00b) mode DXENA = 0	t <sub>en</sub> (BFXH-BDX)	BFSX ext		4H+15		
		BFSX int	2			
DXENA = 1	t <sub>en</sub> (BFXH-BDX)	BFSX ext	14			
		BFSX int	4H-1			
		BFSX ext	2H+5			

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit
			Min	Max	
<b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING (CONTINUED)</b>					
<b>McBSP sample rate generator timing requirements</b> 8/					
Cycle time, SRGR clock input	t <sub>c</sub> (BCKS)	See figure 18	2H		ns
Pulse duration, SRGR clock input high	t <sub>w</sub> (BCKSH)		H-4	H+1	
Pulse duration, SRGR clock input low	t <sub>w</sub> (BCKSL)		H-4	H+1	
Rise time, SRGR clock input	t <sub>r</sub> (BCKS)			8	
Fall time, SRGR clock input	t <sub>f</sub> (BCKS)			8	
<b>McBSP sample rate generator switching characteristics</b>					
Delay time, from SRGR clock input to SRGR output	t <sub>d</sub> (BCKSH-BCLKRXH)	See figure 18	3	13	ns
<b>McBSP GENERAL PURPOSE I/O TIMING</b>					
<b>McBSP general purpose I/O timing requirements</b>					
Setup time, BGPI0x input mode before CLKOUT high <u>27/</u>	t <sub>su</sub> (BGPI0-COH)	See figure 19	9		ns
Hold time, BGPI0x input mode after CLKOUT high <u>27/</u>	t <sub>h</sub> (COH-BGPI0)		0		
<b>McBSP general purpose I/O switching characteristics</b>					
Delay time, CLKOUT high to BGPI0x output mode <u>28/</u>	t <sub>d</sub> (COH-BGPI0)	See figure 19	-5	5	ns

See notes at end of table.

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Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits				Unit
			Master		Slave		
			Min	Max	Min	Max	
<b>MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)</b>							
<b>McBSP as SPI master or slave timing requirements (CLKSTP = 10b, CLKXP = 0) 8/ 29/</b>							
Setup time, BDR valid before BCLKX low	t <sub>su</sub> (BDRV-BCKXL)	See figure 20	12		2-12H		ns
Hold time, BDR valid after BCLKX low	t <sub>h</sub> (BCKXL-BDRV)		4		6+12H		
Setup time, BFSX low before BCLKX high	t <sub>su</sub> (BFXL-BCKXH)				10		
Cycle time, BCLKX	t <sub>c</sub> (BCKX)		12H		32H		
<b>McBSP as SPI master or slave switching characteristics (CLKSTP = 10b, CLKXP = 0) 8/ 29/ 32/</b>							
Hold time, BFSX low after BCLKX low 30/	t <sub>h</sub> (BCKXL-BFXL)	See figure 20	T-5	T+6			ns
Delay time, BFSX low to BCLKX high 31/	t <sub>d</sub> (BFXL-BCKXH)		C-5	C+5			
Delay time, BCLKX high to BDX valid	t <sub>d</sub> (BCKXH-BDXV)		-3	12	6H+4	10H+19	
Disable time, BDX high impedance following last data bit from BCLKX low	t <sub>dis</sub> (BCKXL-BDXHZ)		C-6	C+10			
Disable time, BDX high impedance following last data bit from BFSX high	t <sub>dis</sub> (BFXH-BDXHZ)				4H+4	8H+17	
Delay time, BFSX low to BDX valid	t <sub>d</sub> (BFXL-BDXV)				4H+4	8H+17	
<b>McBSP as SPI master or slave timing requirements (CLKSTP = 11b, CLKXP = 0) 8/ 29/</b>							
Setup time, BDR valid before BCLKX high	t <sub>su</sub> (BDRV-BCKXH)	See figure 20	12		2-12H		ns
Hold time, BDR valid after BCLKX high	t <sub>h</sub> (BCKXH-BDRV)		4		6+12H		
Setup time, BFSX low before BCLKX high	t <sub>su</sub> (BFXL-BCKXH)				10		
Cycle time, BCLKX	t <sub>c</sub> (BCKX)		12H		32H		
<b>McBSP as SPI master or slave switching characteristics (CLKSTP = 11b, CLKXP = 0) 8/ 29/ 32/</b>							
Hold time, BFSX low after BCLKX low 30/	t <sub>h</sub> (BCKXL-BFXL)	See figure 20	C-5	C+6			ns
Delay time, BFSX low to BCLKX high 31/	t <sub>d</sub> (BFXL-BCKXH)		T-5	T+5			
Delay time, BCLKX low to BDX valid	t <sub>d</sub> (BCKXL-BDXV)		-3	12	6H+4	10H+19	
Disable time, BDX high impedance following last data bit from BCLKX low	t <sub>dis</sub> (BCKXL-BDXHZ)		-6	10	6H+4	10H+17	
Delay time, BFSX low to BDX valid	t <sub>d</sub> (BFXL-BDXV)		D-2	D+10	4H+4	8H+17	

See notes at end of table.

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Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits				Unit
			Master		Slave		
			Min	Max	Min	Max	
<b>MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)</b>							
<b>McBSP as SPI master or slave timing requirements (CLKSTP = 10b, CLKXP = 1) 8/ 29/</b>							
Setup time, BDR valid before BCLKX high	t <sub>su</sub> (BDRV-BCKXH)	See figure 21	12		2-12H		ns
Hold time, BDR valid after BCLKX high	t <sub>h</sub> (BCKXH-BDRV)		4		6+12H		
Setup time, BFSX low before BCLKX low	t <sub>su</sub> (BFXL-BCKXL)				10		
Cycle time, BCLKX	t <sub>c</sub> (BCKX)		12H		32H		
<b>McBSP as SPI master or slave switching characteristics (CLKSTP = 10b, CLKXP = 1) 8/ 29/ 32/</b>							
Hold time, BFSX low after BCLKX high 30/	t <sub>h</sub> (BCKXH-BFXL)	See figure 21	T-5	T+6			ns
Delay time, BFSX low to BCLKX low 31/	t <sub>d</sub> (BFXL-BCKXL)		D-5	D+5			
Delay time, BCLKX low to BDX valid	t <sub>d</sub> (BCKXL-BDXV)		-3	12	6H+4	10H+19	
Disable time, BDX high impedance following last data bit from BCLKX high	t <sub>dis</sub> (BCKXH-BDXHZ)		D-6	D+10			
Disable time, BDX high impedance following last data bit from BFSX high	t <sub>dis</sub> (BFXH-BDXHZ)				4H+4	8H+17	
Delay time, BFSX low to BDX valid	t <sub>d</sub> (BFXL-BDXV)				4H+4	8H+17	
<b>McBSP as SPI master or slave timing requirements (CLKSTP = 11b, CLKXP = 1) 8/ 29/</b>							
Setup time, BDR valid before BCLKX low	t <sub>su</sub> (BDRV-BCKXL)	See figure 21	12		2-12H		ns
Hold time, BDR valid after BCLKX low	t <sub>h</sub> (BCKXL-BDRV)		4		6+12H		
Setup time, BFSX low before BCLKX low	t <sub>su</sub> (BFXL-BCKXL)				10		
Cycle time, BCLKX	t <sub>c</sub> (BCKX)		12H		32H		
<b>McBSP as SPI master or slave switching characteristics (CLKSTP = 11b, CLKXP = 1) 8/ 29/ 32/</b>							
Hold time, BFSX low after BCLKX high 30/	t <sub>h</sub> (BCKXH-BFXL)	See figure 21	D-5	D+6			ns
Delay time, BFSX low to BCLKX low 31/	t <sub>d</sub> (BFXL-BCKXL)		T-5	T+5			
Delay time, BCLKX high to BDX valid	t <sub>d</sub> (BCKXH-BDXV)		-3	12	6H+4	10H+19	
Disable time, BDX high impedance following last data bit from BCLKX high	t <sub>dis</sub> (BCKXH-BDXHZ)		-6	10	6H+4	10H+17	
Delay time, BFSX low to BDX valid	t <sub>d</sub> (BFXL-BDXV)		C-2	C+10	4H+4	8H+17	

See notes at end of table.

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Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit		
			Min	Max			
<b>HOST PORT INTERFACE TIMING</b>							
<b>HPI16 mode timing requirements 8/ 33/</b>							
Setup time, HAD valid before $\overline{DS}$ falling edge 34/ 35/	t <sub>su</sub> (HBV-DSL)	See figure 22-25	5		ns		
Hold time, HAD valid after $\overline{DS}$ falling edge 34/ 35/	t <sub>h</sub> (DSL-HBV)		5				
Setup time, HAD valid before $\overline{HAS}$ falling edge 34/	t <sub>su</sub> (HBV-HSL)		5				
Hold time, HAD valid after $\overline{HAS}$ falling edge 34/	t <sub>h</sub> (HSL-HBV)		5				
Setup time, address valid before $\overline{DS}$ rising edge (nonmultiplexed write) 35/	t <sub>su</sub> (HAV-DSH)		5				
Setup time, address valid before $\overline{DS}$ falling edge (nonmultiplexed read) 35/	t <sub>su</sub> (HAV-DSL)		-(4H+5)				
Hold time, address valid after $\overline{DS}$ rising edge (nonmultiplexed mode) 35/	t <sub>h</sub> (DSH-HAV)		1				
Setup time, $\overline{HAS}$ low before $\overline{DS}$ falling edge 35/	t <sub>su</sub> (HSL-DSL)		5				
Hold time, $\overline{HAS}$ low after $\overline{DS}$ falling edge 35/	t <sub>h</sub> (HSL-DSL)		2				
Pulse duration, $\overline{DS}$ low 35/	t <sub>w</sub> (DSL)		30				
Pulse duration, $\overline{DS}$ high 35/	t <sub>w</sub> (DSH)		10				
Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge 35/	Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with no DMA activity.		t <sub>c</sub> (DSH-DSH)  36/	Reads		10H+30	
	Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with 16 bit DMA activity.			Writes		10H+10	
	Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with 32 bit DMA activity.			Reads		16H+30	
Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge 35/ 37/	Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with no DMA activity.	Writes		16H+10			
	Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with 16 bit DMA activity.	Reads		24H+30			
	Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with 32 bit DMA activity.	Writes		24H+10			
Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge for writes to DSPINT and $\overline{HINT}$ 35/				10H+10			
Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge for HPIC reads, HPIC XADD bit writes, and address register reads and writes 35/				16H+10			
				24H+10			
				8H			
				40			

See notes at end of table.

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Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit	
			Min	Max		
<b>HOST PORT INTERFACE TIMING (CONTINUED)</b>						
<b>HPI16 mode timing requirements (Continued) 8/ 33/</b>						
Setup time, HD valid before $\overline{DS}$ rising edge 35/	t <sub>su</sub> (HDV-DSH)W	See figure 22-25	10		ns	
Hold time, HD valid after $\overline{DS}$ rising edge, write 35/	t <sub>h</sub> (DSH-HDV)W		1			
Setup time, SELA/B valid before $\overline{DS}$ falling edge 35/	t <sub>su</sub> (SELV-DSL)		5			
Hold time, SELA/B valid after $\overline{DS}$ rising edge 35/	t <sub>h</sub> (DSH-SELV)		0			
<b>HPI16 mode switching characteristics 8/ 33/</b>						
Delay time, $\overline{DS}$ low to HD driven 34/	t <sub>d</sub> (DSL-HDD)	See figure 22-25	3	20	ns	
Delay time, $\overline{DS}$ low to HD valid for first word of an HPI read  34/	Case 1a: Memory accesses initiated immediately following a write when DMAC is active in 16 bit mode and t <sub>w</sub> (DSH) was < 18H		t <sub>d</sub> (DSL-HDV1)  36/			32H+20 - t <sub>w</sub> (DSH)
	Case 1b: Memory accesses initiated by an autoincrement when DMAC is active in 16 bit mode and t <sub>w</sub> (DSH) was < 18H					16H+20 - t <sub>w</sub> (DSH)
	Case 1c: Memory accesses not initiated by an autoincrement (or not immediately following a write) when DMAC is active in 16 bit mode					16H+20
	Case 1d: Memory accesses initiated by an autoincrement when DMAC is active in 16 bit mode and t <sub>w</sub> (DSH) was ≥ 18H					20
	Case 1e: Memory accesses initiated immediately following a write when DMAC is active in 32 bit mode and t <sub>w</sub> (DSH) was < 26H					48H+20 - t <sub>w</sub> (DSH)
	Case 1f: Memory accesses initiated by an autoincrement when DMAC is active in 32 bit mode and t <sub>w</sub> (DSH) was < 26H					24H+20 - t <sub>w</sub> (DSH)
	Case 1g: Memory accesses not initiated by an autoincrement (or not immediately following a write) when DMAC is active in 32 bit mode					24H+20
	Case 1h: Memory accesses initiated by an autoincrement when DMAC is active in 32 bit mode and t <sub>w</sub> (DSH) was ≥ 26H					20

See notes at end of table.

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Test	Symbol	Test condition -40°C ≤ T <sub>C</sub> ≤ +85°C 1.75 V ≤ CV <sub>DD</sub> ≤ 1.98 V 3.0 V ≤ DV <sub>DD</sub> ≤ 3.6 V unless otherwise noted	Limits		Unit	
			Min	Max		
<b>HOST PORT INTERFACE TIMING (CONTINUED)</b>						
<b>HPI16 mode switching characteristics (Continued) 8/ 33/</b>						
Delay time, $\overline{\text{HAS}}$ low to HD valid for first word of an HPI read	Case 2a: Memory accesses initiated immediately following a write when DMAC is inactive and $t_{w(\text{DSH})}$ was < 10H	$t_{d(\text{DSL-HDV1})}$  <u>36/</u>	See figure 22-25		20H+20 - $t_{w(\text{DSH})}$	ns
	Case 2b: Memory accesses initiated by an autoincrement when DMAC is inactive and $t_{w(\text{DSH})}$ was < 10H				10H+20 - $t_{w(\text{DSH})}$	
	Case 2c: Memory accesses not initiated by an autoincrement (or not immediately following a write) when DMAC is inactive				10H+20	
	Case 2d: Memory accesses initiated by an autoincrement when DMAC is inactive and $t_{w(\text{DSH})}$ was ≥ 10H				20	
	Case 3: HPI16/HPIA reads				20	
Multiplexed reads with autoincrement. Prefetch completed.	$t_{d(\text{DSL-HDV2})}$		3	20		
Delay time, $\overline{\text{DS}}$ high to HRDY high <u>35/</u> (writes and autoincrement reads)	Memory accesses (or writes to the FETCH bit) when no DMAC is active	$t_{d(\text{DSH-HYH})}$  <u>36/</u>			10H+5	
	Memory accesses (or writes to the FETCH bit) with one or more 16 bit DMAC channels active				16H+5	
	Memory accesses (or writes to the FETCH bit) with one or more 32 bit DMAC channels active				24H+5	
	Writes to DSPINT and $\overline{\text{HINT}}$ <u>38/</u>				4H+5	
Valid time, HD valid after HRDY high	$t_{v(\text{HYH-HDV})}$				7	
Hold time, HD valid after $\overline{\text{DS}}$ rising edge, read <u>38/</u>	$t_{h(\text{DSH-HDV})R}$		0		10	
Delay time, CLKOUT rising edge to HRDY high	$t_{d(\text{COH-HYH})}$				5	
Delay time, $\overline{\text{DS}}$ low to HRDY low <u>39/</u>	$t_{d(\text{DSL-HYL})}$				12	
Delay time, $\overline{\text{DS}}$ high to HRDY low <u>39/</u>	$t_{d(\text{DSH-HYL})}$				12	
Delay time, $\overline{\text{HAS}}$ low to HRDY low, read	$t_{d(\text{HSL-HYL})}$				12	
Delay time, CLKOUT rising edge to $\overline{\text{HINT}}$ change	$t_{d(\text{COH-HTX})}$				5	

See notes at end of table.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV A	PAGE 19

TABLE I. Electrical performance characteristics - Continued.

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ All input and output voltage levels except  $\overline{RS}$ ,  $\overline{INT0}$ ,  $\overline{INT1}$ ,  $\overline{NMI}$ , CLKIN, BCLKX, BCLKR,  $\overline{HAS}$ ,  $\overline{HCS}$ ,  $\overline{HDS1}$ ,  $\overline{HDS2}$ , and  $\overline{HPIRS}$  are LVTTTL compatible.
- 3/  $V_{IL(MIN)} \leq V_I \leq V_{IL(MAX)}$  or  $V_{IH(MIN)} \leq V_I \leq V_{IH(MAX)}$ .
- 4/ Clock mode: PLL x 1 with external source.
- 5/ This value is based on 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with the program being executed.
- 6/ This value was obtained using the following conditions: external memory writes at a rate 20 million writes per second, CLKOFF = 0, full duplex operation of all six McBSP at a rate of 10 million bits per second each, and 15 pF loads on all outputs. For more details on how this calculation is performed, refer to the Calculation of TMS320LC54x Power Dissipation Application Report (literature number SPRA164).
- 7/ This device utilizes a fully static design and therefore can operate with  $t_{c(CI)}$  approaching  $\infty$ . The device is characterized at frequencies approaching 0 Hz.
- 8/  $H = 0.5t_{c(CO)}$ .
- 9/ N = Multiplication factor.
- 10/ The multiplication factor and minimum CLKIN cycle time should be chosen such that the resulting CLKOUT cycle time is within the specified range ( $t_{c(CO)}$ ).
- 11/ Address,  $\overline{PS}$ , and  $\overline{DS}$  timings are all included in timings referenced as address.
- 12/ In the case of a memory read preceded by a memory read.
- 13/ In the case of a memory read preceded by a memory write.
- 14/  $\overline{MSTRB} = 0$ ,  $H = 0.5t_{c(CO)}$ .
- 15/ In the case of a memory write preceded by a memory write.
- 16/ In the case of a memory write preceded by an I/O cycle
- 17/ The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.
- 18/ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.
- 19/ Address and  $\overline{IS}$  timings are included in timings referenced as address.
- 20/ The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states using READY, at least two software wait states must be programmed.
- 21/ The external interrupts ( $\overline{INT0}$  -  $\overline{INT1}$ ,  $\overline{NMI}$ ) are synchronized to the core CPU by way of a two flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1-0-0 sequence at the timing that is corresponding to the three-CLKOUT sampling sequence.
- 22/ If the PLL mode is selected, then at power on sequence, or at wakeup from IDLE3,  $\overline{RS}$  must be held low for at least 50  $\mu$ s to ensure synchronization and clock in of the PLL.
- 23/  $\overline{RS}$  can cause a change in clock frequency, changing the value of H (see the software programmable phase locked loop (PLL) section).
- 24/ Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- 25/  $T = \text{BCLKRX period} = (1 + \text{CLKGDV}) * 2H$   
 $C = \text{BCLKRX low pulse width} = T/2$  when CLKGDV is odd or zero and  $= (\text{CLKGDV}/2) * 2H$  when CLKGDV is even  
 $D = \text{BCLKRX high pulse width} = T/2$  when CLKGDV is odd or zero and  $= (\text{CLKGDV}/2 + 1) * 2H$  when CLKGDV is even.
- 26/ See manufacturer TMS320C54x DSP reference set, Volume 5: Enhanced peripherals (literature number SPRU302) for a description of the DX enable (DXENA) and data delay features of the McBSP.

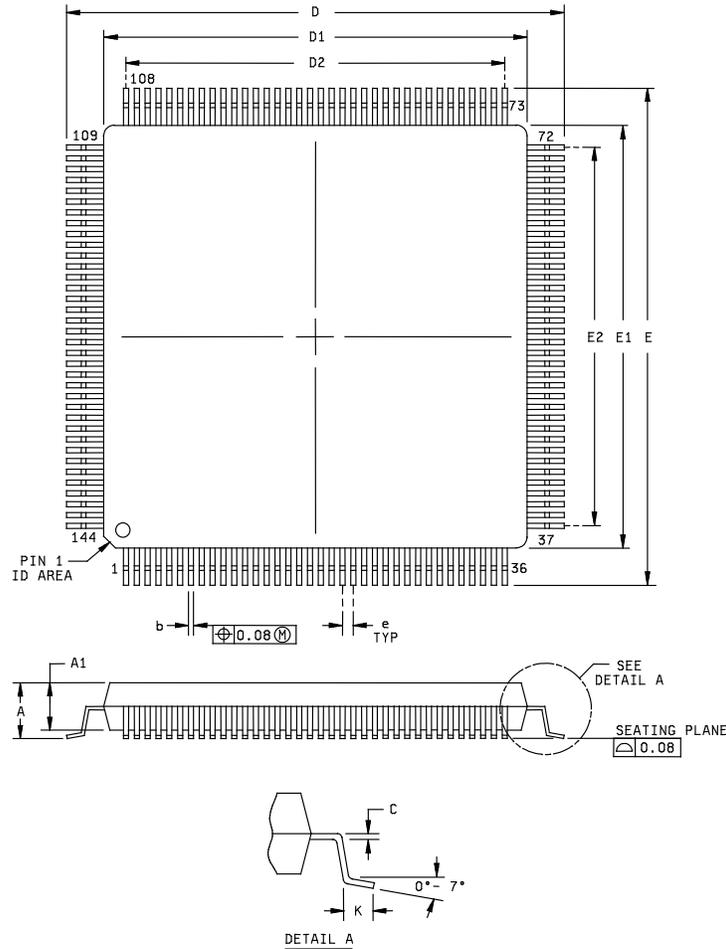
<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV    A	PAGE    20

TABLE I. Electrical performance characteristics - Continued.

- 27/ BGPI0x refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general purpose input.
- 28/ BGPI0x refers to BCLKRx, BFSRx, BCLKXx, BFSXx or BDXx when configured as a general purpose output.
- 29/ For all SPI slave modes, CLKG is programmed as ½ of the CPU clock by setting CLKSM = CLKGDV = 1
- 30/ FSRP = FSXP =1. As a SPI master, BFSX is inverted to provide active low slave enable output. As a slave, the active low signal input on BFSX and BFSR is inverted before being used internally.  
 CLKXM = FSXM = 1, CLKRM = BFSRM = 0 for master McBSP  
 CLKXM = CLKRM = FSXM = BFSRM = 0 for slave McBSP
- 31/ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).
- 32/ T = BCLKX period = (1 + CLKGDV) \* 2H  
 C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) \* 2H when CLKGDV is even  
 D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) \* 2H when CLKGDV is even.
- 33/  $\overline{DS}$  refers to the logical OR of  $\overline{HCS}$ ,  $\overline{HDS1}$ , and  $\overline{HDS2}$ , and HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.).
- 34/ HAD stands for HCNTL0, HCNTL11, and  $\overline{HR/W}$ .
- 35/  $\overline{DS}$  refers to either  $\overline{HCS}$  or  $\overline{HDS}$ , whichever is controlling the transfer. Refer to the manufacturer TMS320C54x DSP Reference set, Volume 5: Enhanced Peripherals (literature number SPRU302) for information regarding logical operation of the HPI16. These timings are shown assuming that  $\overline{HDS}$  is the signal controlling the transfer.
- 36/ These timings are for HPI access which do not cross from one subsystem to the other. For access which do cross from one subsystem to the other, additional cycles are required. A detailed description of these considerations is provided in the application note Memory Transfer with TMS320VC5420 and TMS320VC5421 DSPs (literature number DPRA620).
- 37/ In autoincrement mode, WRTE timings are the same as READ timings.
- 38/  $\overline{HDS}$  refers to either  $\overline{HDS1}$  or  $\overline{HDS2}$ .
- 39/ HRDY does not go low for other register accesses.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p>SIZE <b>A</b></p>	<p>CODE IDENT NO. <b>16236</b></p>	<p>DWG NO. <b>V62/04607</b></p>
		<p>REV     <b>A</b></p>	<p>PAGE    <b>21</b></p>

Case X



Millimeters					
Symbol	Min	Max	Symbol	Min	Max
A		1.60	D1/E1	19.80	20.20
A1	1.35	1.45	D2/E2	17.50 TYP	
b	0.17	0.27	e	0.50 TYP	
c	0.13 NOM		K	0.45	0.75
D/E	21.80	22.20			

Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Fall within JEDEC MO-136

FIGURE 1. Case outlines.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	SIZE <b>A</b>	CODE IDENT NO. <b>16236</b>	DWG NO. <b>V62/04607</b>
		REV <b>A</b>	PAGE <b>22</b>

Case X

Pin No.	Signal Name (non multiplexed)	Signal Name (multiplexed)	Pin No.	Signal Name (non multiplexed)	Signal Name (multiplexed)
1	PPD7	HD7	37	V <sub>SS</sub>	
2	PPA8	HA8	38	PPD15	HD15
3	PPA0	A_HINT/HA0	39	PPD14	HD14
4	DV <sub>DD</sub>		40	V <sub>SS</sub>	
5	PPA9	HA9	41	PPD13	HD13
6	PPD1	HD1	42	PPD12	HD12
7	A_INT1		43	A_BFSR0	
8	A_NMI		44	A_BDR0	
9	IOSTRB	A_GPIO3/A_TOUT	45	A_BCLKR0	
10	A_GPIO2/BIO		46	A_BFSX0	
11	A_GPIO1		47	V <sub>SS</sub>	
12	A_RS		48	CV <sub>DD</sub>	
13	A_GPIO0	A_ROMEN	49	A_BDX0	
14	V <sub>SS</sub>		50	A_BCLKX0	
15	V <sub>SS</sub>		51	MSTRB	HCS
16	CV <sub>DD</sub>		52	DS	HDS2
17	A_BFSR1		53	PS	HDS1
18	A_BDR1		54	B_BCLKX0	
19	A_BCLKR1		55	B_BDX0	
20	A_BFSX1		56	DV <sub>DD</sub>	
21	CV <sub>DD</sub>		57	V <sub>SS</sub>	
22	V <sub>SS</sub>		58	B_BFSX0	
23	A_BDX1		59	B_BCLKR0	
24	A_BCLKX1		60	B_BDR0	
25	A_XF		61	CV <sub>DD</sub>	
26	A_CLKOUT		62	V <sub>SS</sub>	
27	HOLDA		63	B_BFSR0	
28	TCK		64	R/W	HR/W
29	TMS		65	PPA2	HCNTL1/HA2
30	TDI		66	PPA3	HCNTL0/HA3
31	TRST		67	SELA/B	PPA18
32	EMU1/OFF		68	PPD8	HD8
33	DV <sub>DD</sub>		69	PPD9	HD9
34	A_INT0		70	PPD10	HD10
35	EMU0		71	PPD11	HD11
36	TDO		72	V <sub>SS</sub>	

FIGURE 2. Terminal connections.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV A	PAGE 23

## Case X

Pin No.	Signal Name (non multiplexed)	Signal Name (multiplexed)	Pin No.	Signal Name (non multiplexed)	Signal Name (multiplexed)
73	PPA10	HA10	109	PPA17	HA7
74	PPA11	HA11	110	PPA6	HA6
75	DV <sub>DD</sub>		111	PPA4	HAS /HA4
76	V <sub>SS</sub>		112	DV <sub>DD</sub>	
77	PPA12	HA12	113	PPA5	HA5
78	PPA13	HA13	114	PPA1	B _HINT /HA1
79	HPIRS		115	PPD3	HD3
80	HMODE		116	PPD2	HD2
81	B_CLKOUT		117	B_BFSR2	
82	B_XF		118	B_BDR2	
83	B_RS		119	V <sub>SS</sub>	
84	XIO		120	CV <sub>DD</sub>	
85	TEST		121	B_BCLKR2	
86	V <sub>SS</sub>		122	B_BFSX2	
87	CV <sub>DD</sub>		123	B_BDX2	
88	B_BCLKX1		124	B_BCLKX2	
89	B_BDX1		125	V <sub>SS</sub>	
90	V <sub>SS</sub>		126	AV <sub>DD</sub>	
91	B_BFSX1		127	V <sub>SSA</sub>	
92	B_BCLKR1		128	HOLD	
93	V <sub>SS</sub>		129	CLKIN	
94	CV <sub>DD</sub>		130	DV <sub>DD</sub>	
95	B_BDR1		131	READY	HRDY
96	B_BFSR1		132	A_BCLKX2	
97	B_GPIO0	B_ROMEN	133	CV <sub>DD</sub>	
98	B_GPIO1		134	V <sub>SS</sub>	
99	B_GPIO2/BIO		135	A_BCLKR2	
100	IS	B_GPIO3/B_TOUT	136	A_BDR2	
101	B_NMI		137	A_BFSX2	
102	B_INT1		138	A_BDX2	
103	B_INT0		139	A_BFSX2	
104	PPA17	HA117	140	PPD6	HD6
105	PPA16	HA16	141	PPD4	HD4
106	V <sub>SS</sub>		142	PPD5	HD5
107	PPA15	HA15	143	PPD0	HD0
108	PPA14	HA14	144	V <sub>SS</sub>	

FIGURE 2. Terminal connections - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV A	PAGE 24

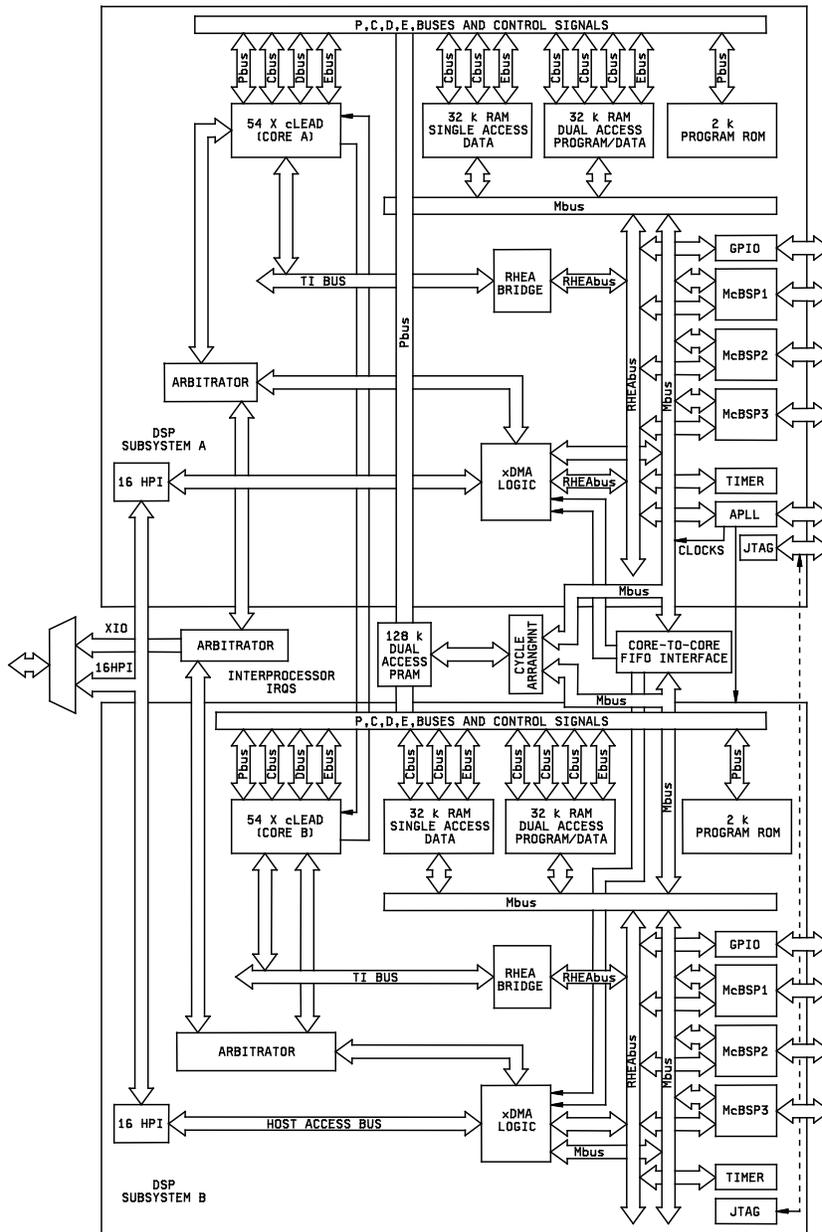
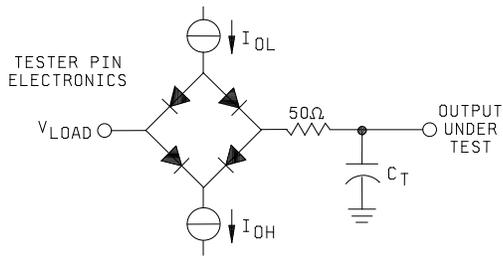


FIGURE 3. Block diagram.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/04607</b></p>
		<p>REV A</p>	<p>PAGE 25</p>



Where:  $I_{OL}$  = 1.5 mA (all outputs)  
 $I_{OH}$  = 300  $\mu$ A (all outputs)  
 $V_{Load}$  = 1.5 V  
 $C_T$  = 40 pF typical load circuit capacitance.

FIGURE 4. Load circuit.

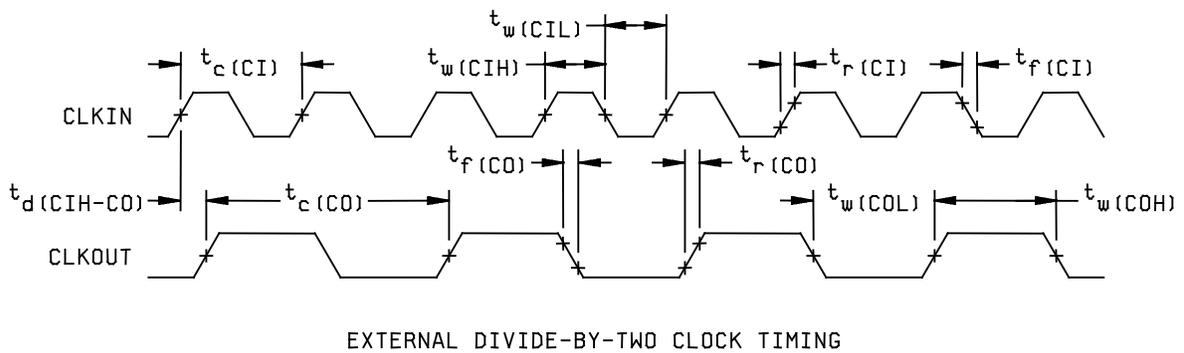


FIGURE 5. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. <b>V62/04607</b>
		REV    A	PAGE    26

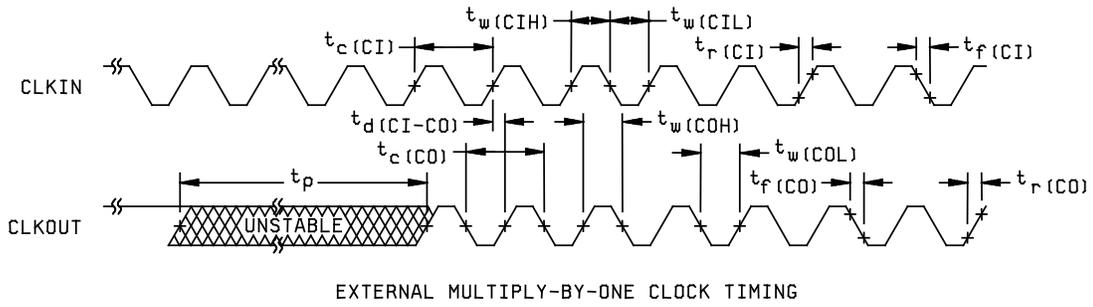


FIGURE 6. Timing waveforms - Continued.

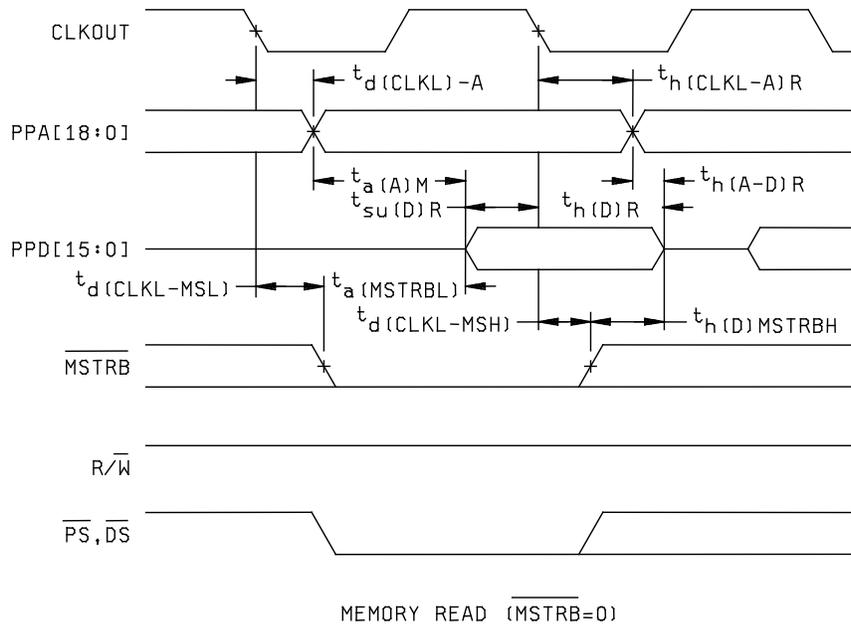


FIGURE 7. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV    A	PAGE    27

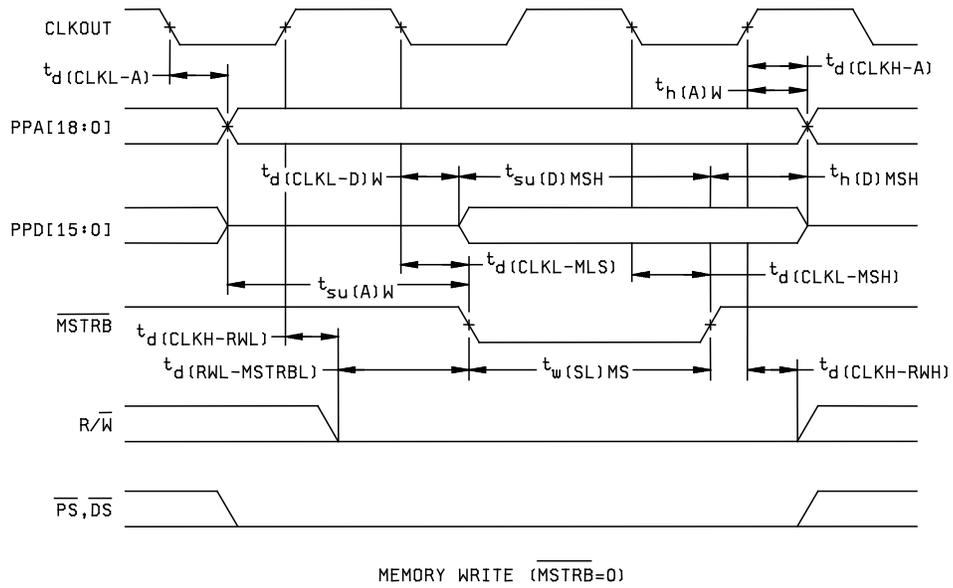
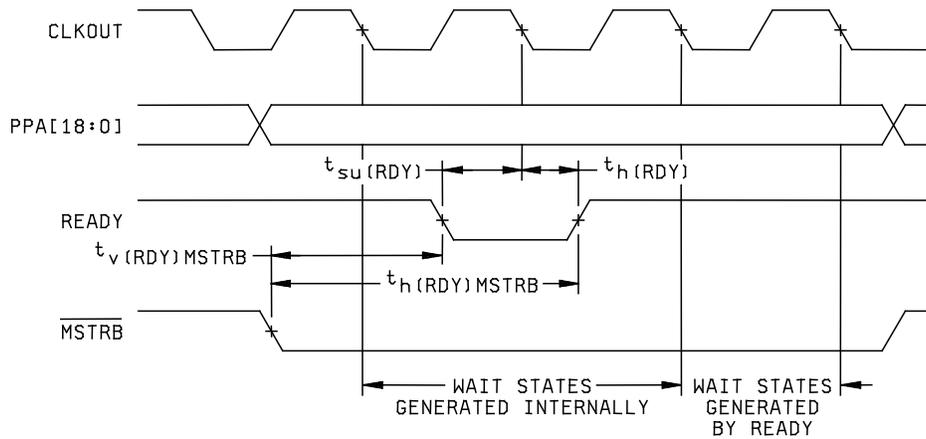
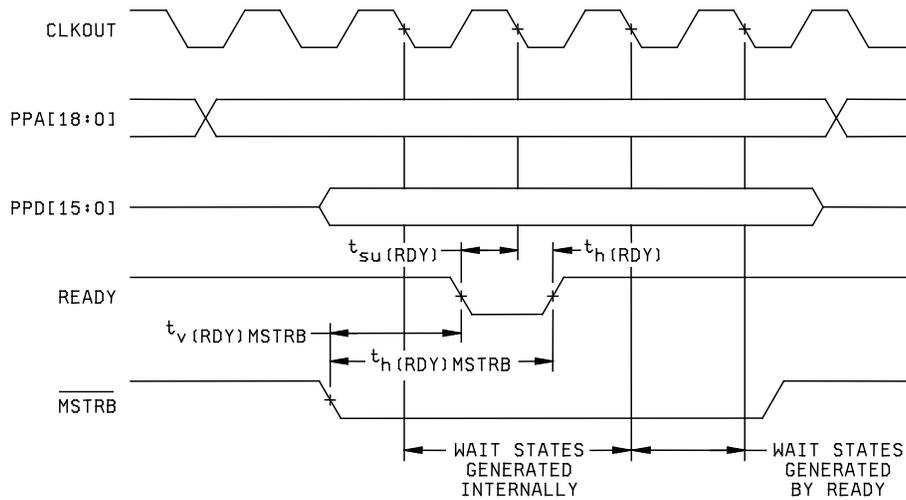


FIGURE 8. Timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. <b>V62/04607</b>
		REV    A	PAGE    28



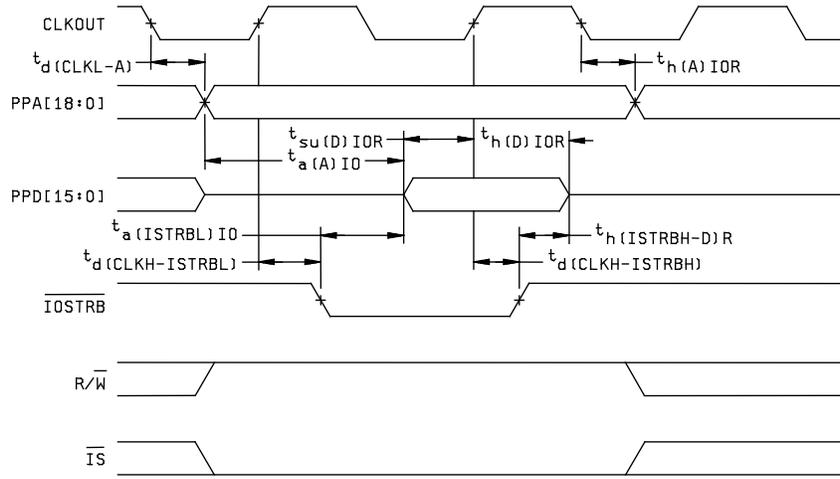
MEMORY READ WITH EXTERNALLY GENERATED WAIT STATES



MEMORY WRITE WITH EXTERNALLY GENERATED WAIT STATES

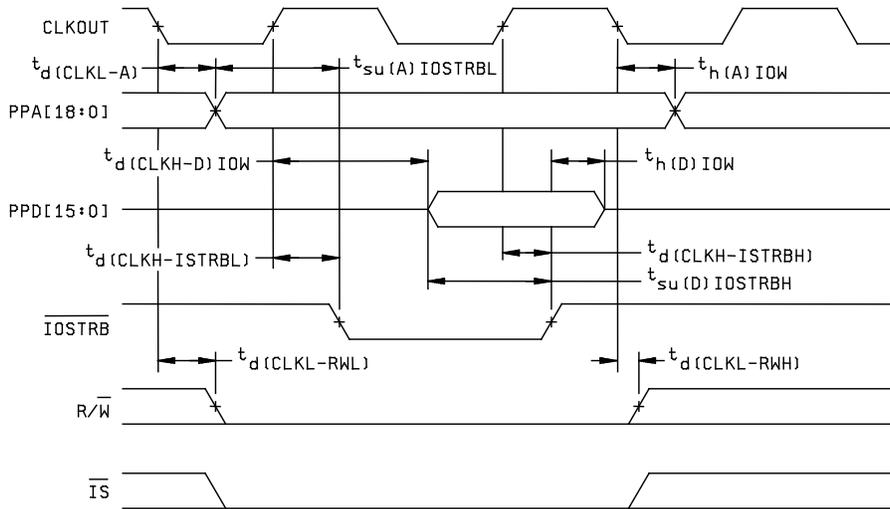
FIGURE 9. Timing waveforms - Continued.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/04607</b></p>
		<p>REV A</p>	<p>PAGE 29</p>



PARALLEL I/O PORT READ ( $\overline{\text{IOSTRB}}=0$ )

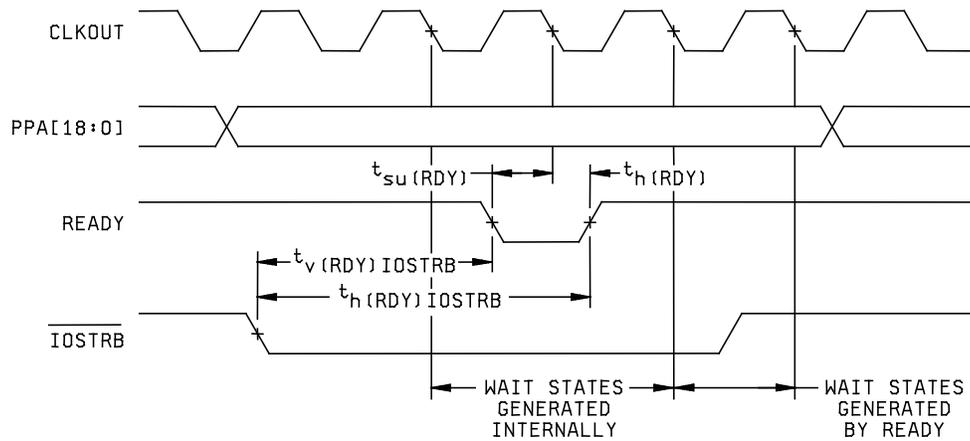
FIGURE 10. Timing waveforms - Continued.



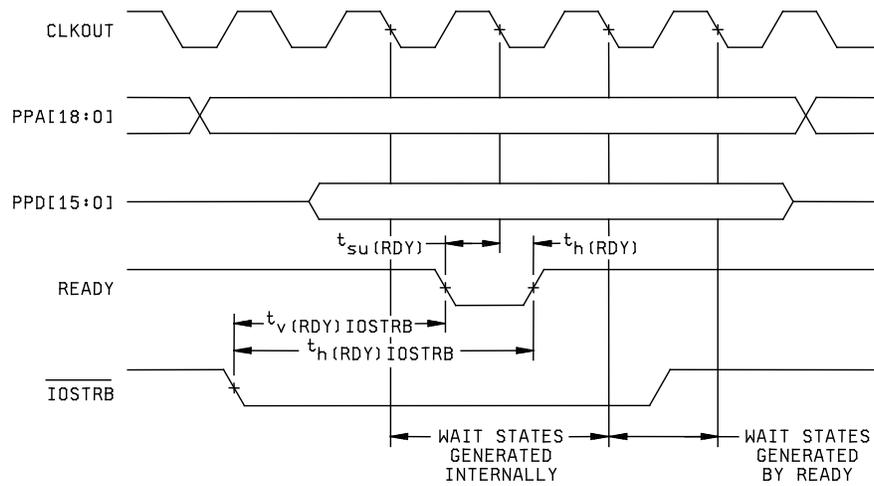
PARALLEL I/O PORT WRITE ( $\overline{\text{IOSTRB}}=0$ )

FIGURE 11. Timing waveforms - Continued.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/04607</b></p>
		<p>REV A</p>	<p>PAGE 30</p>



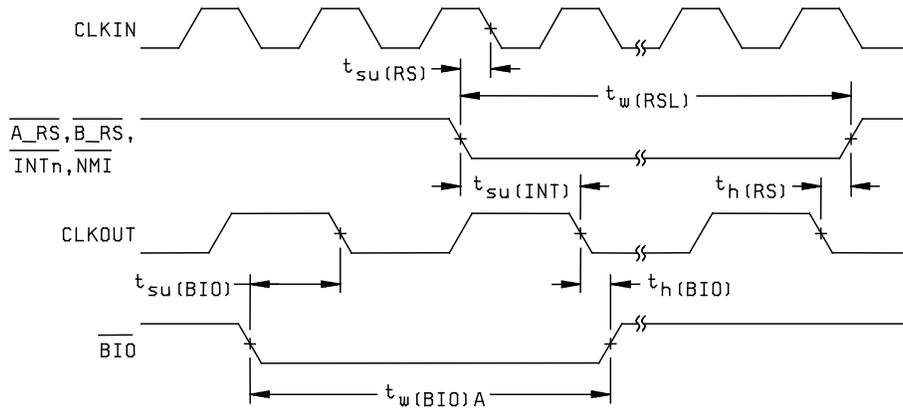
I/O PORT READ WITH EXTERNALLY GENERATED WAIT STATES



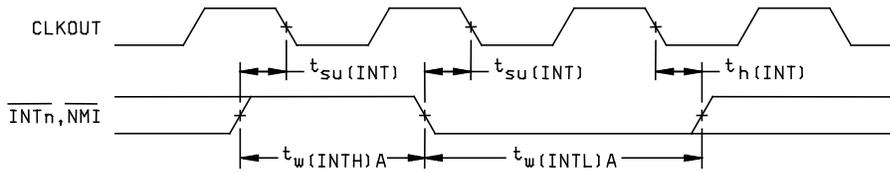
I/O PORT WRITE WITH EXTERNALLY GENERATED WAIT STATES

FIGURE 12. Timing waveforms - Continued.

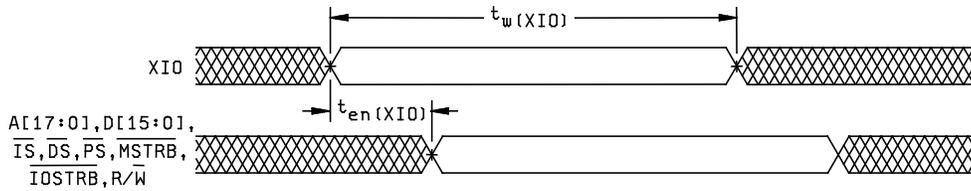
<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		<b>REV    A</b>	<b>PAGE    31</b>



RESET AND  $\overline{\text{BIO}}$  TIMINGS



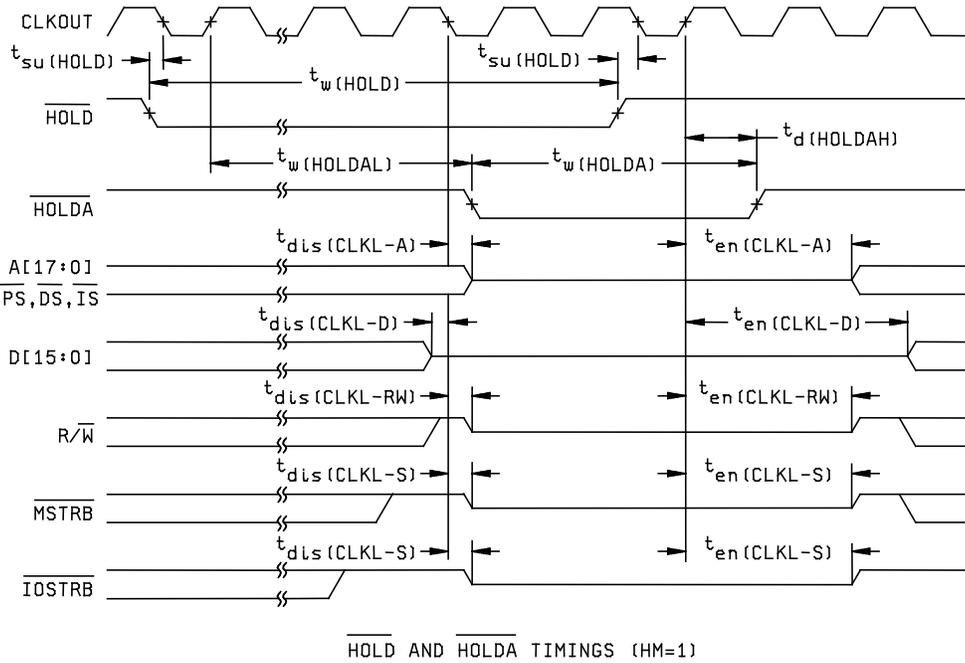
INTERRUPT TIMING



XIO TIMING

FIGURE 13. Timing waveforms - Continued.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/04607</b></p>
		<p>REV A</p>	<p>PAGE 32</p>

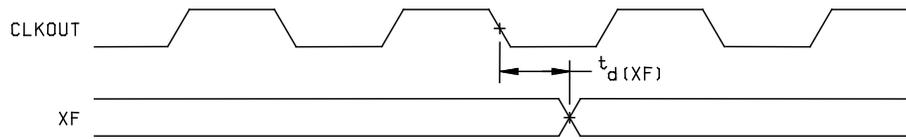


Note:

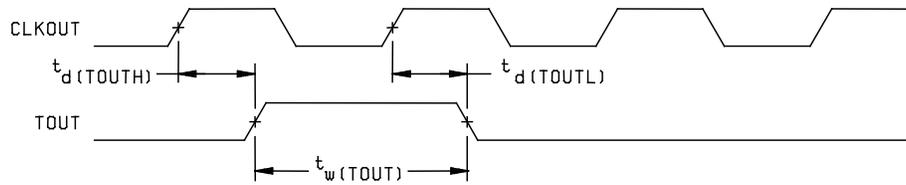
A[17:16] apply to DMA accesses to extended DATA and PROGRAM memory. The CPU has access to only extended PROGRAM memory.

FIGURE 14. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV    A	PAGE    33

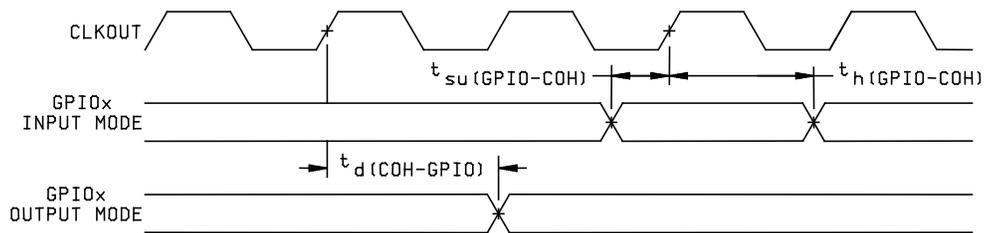


EXTERNAL FLAG (XF) TIMING



TIMER (TOUT) TIMING

FIGURE 15. Timing waveforms - Continued.



GPIO TIMINGS

FIGURE 16. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		<b>REV    A</b>	<b>PAGE    34</b>

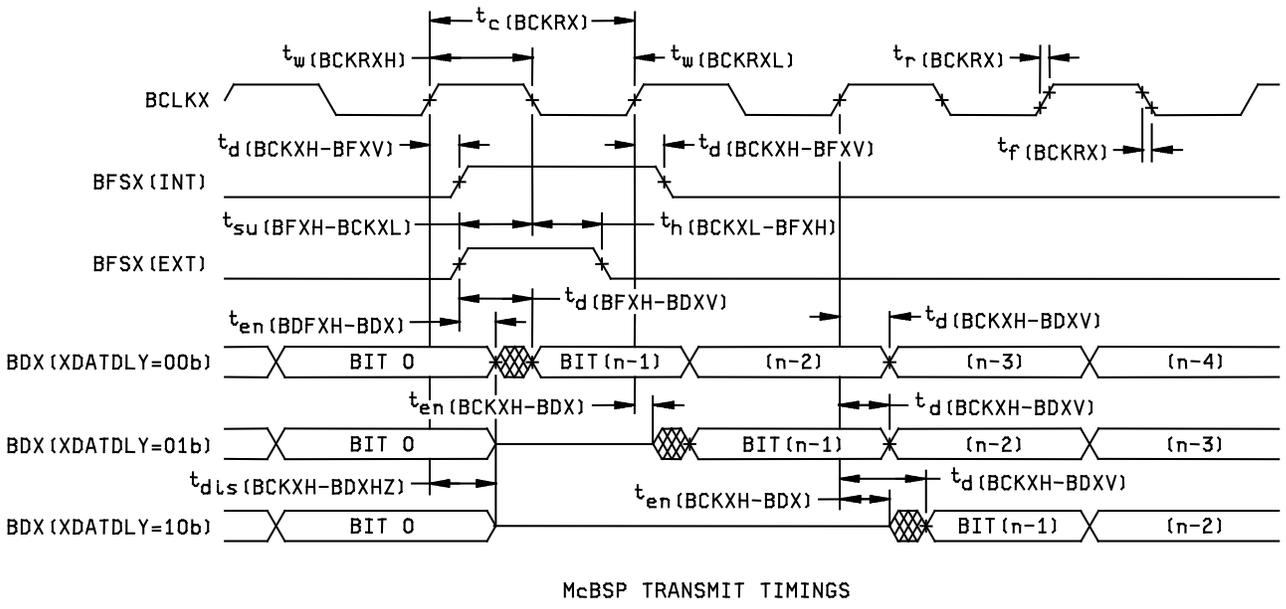
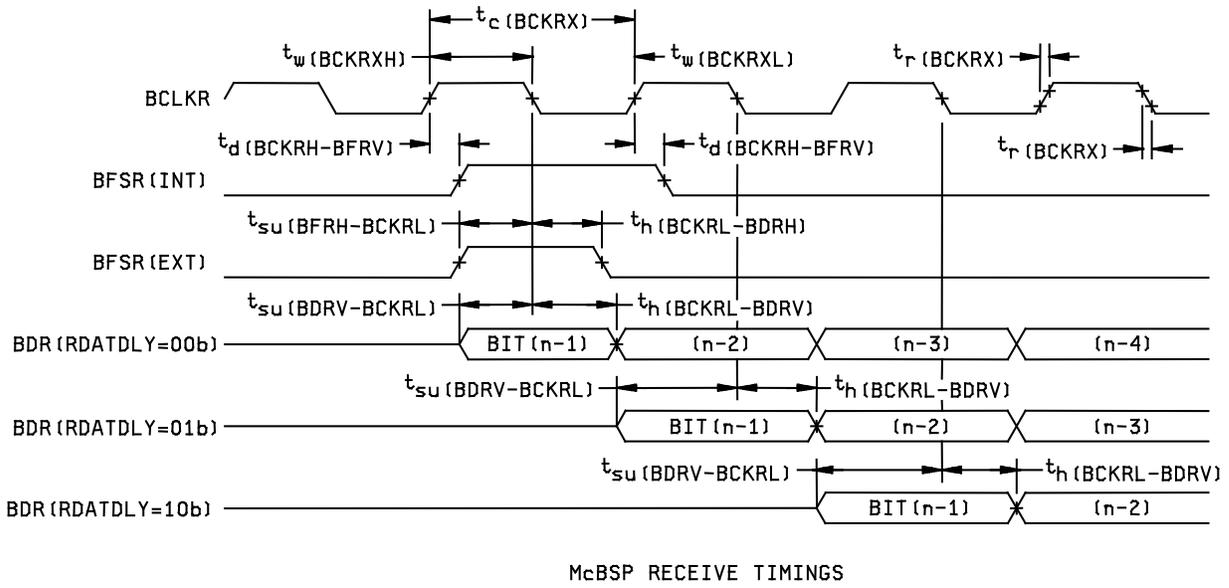


FIGURE 17. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV    A	PAGE    35

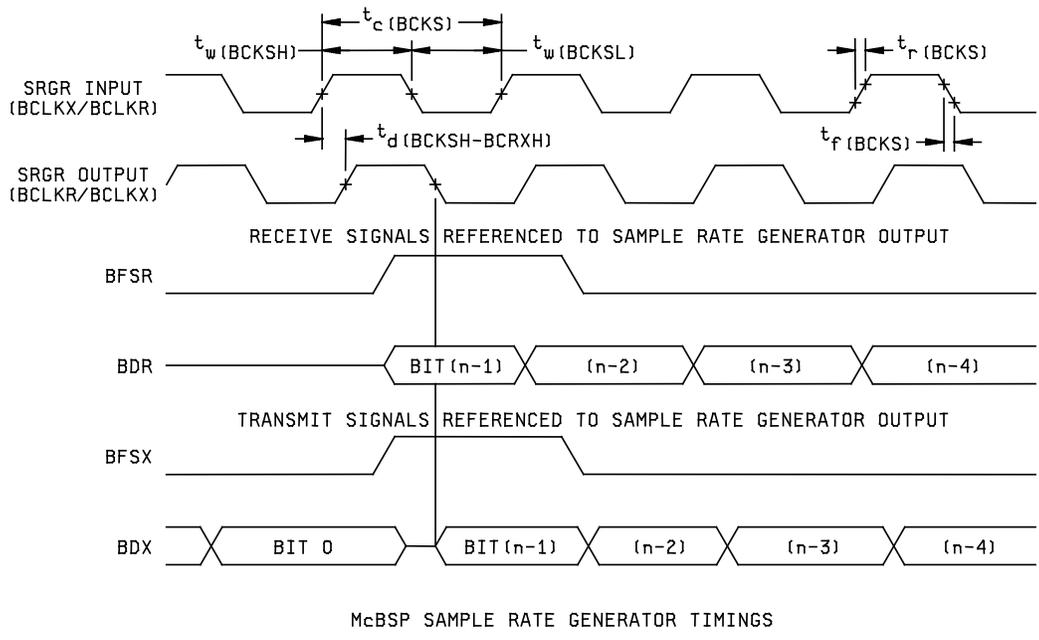
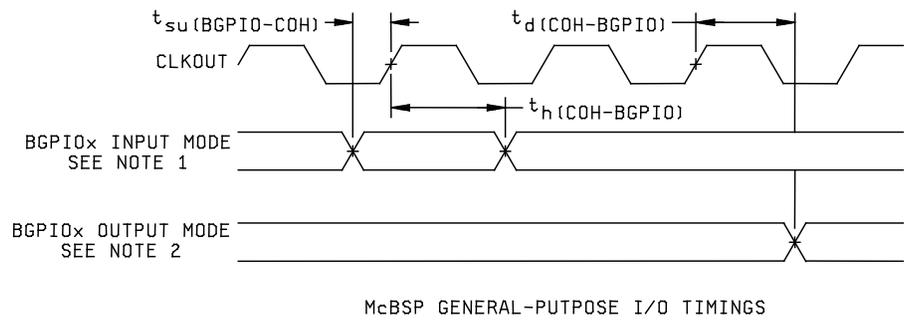


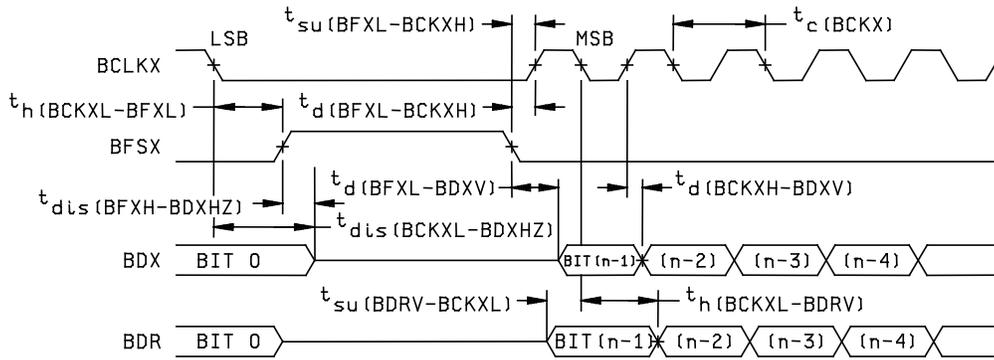
FIGURE 18. Timing waveforms - Continued.



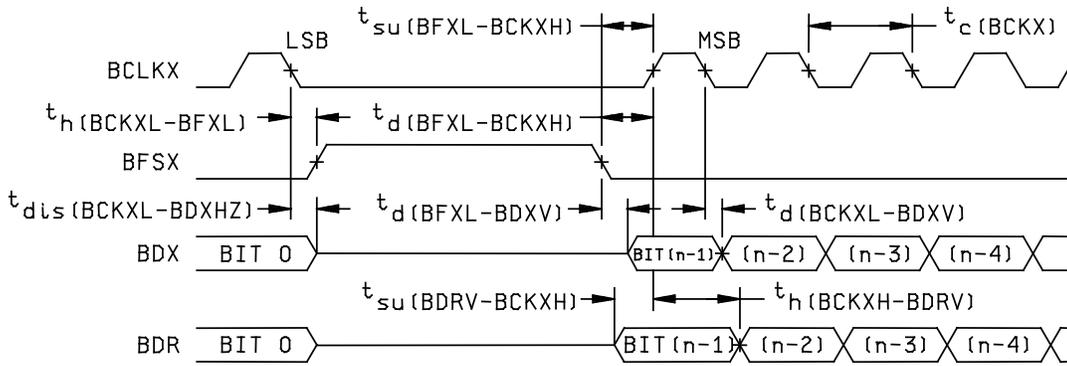
- Notes:
1. BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general purpose input.
  2. BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general purpose output

FIGURE 19. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV    A	PAGE    36



McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=10b, CLKXP=0



McBSP TIMING AS SPI MASTER OR SLAVE: CLKSTP=11b, CLKXP=0

FIGURE 20. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		<b>REV    A</b>	<b>PAGE    37</b>

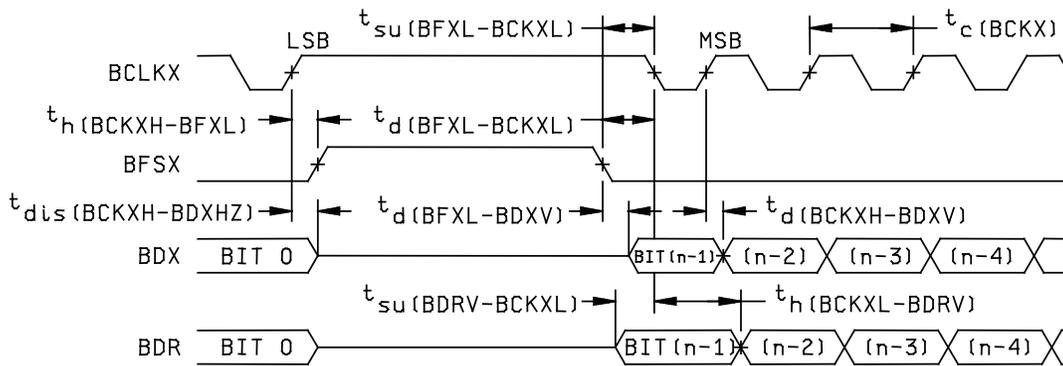
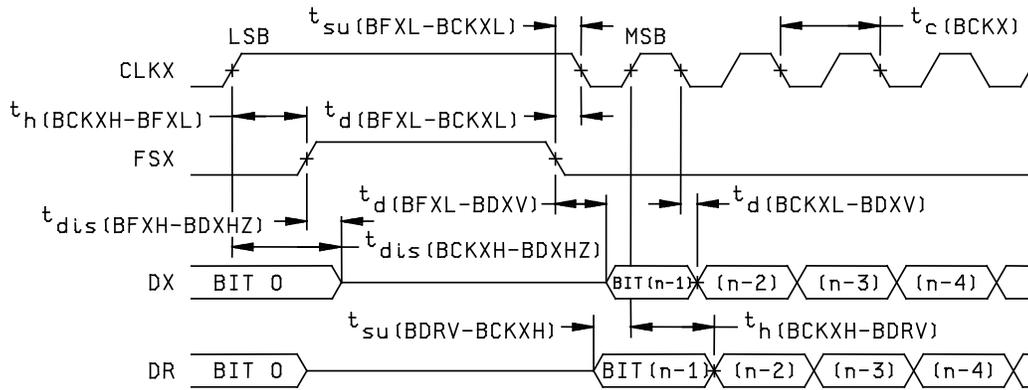
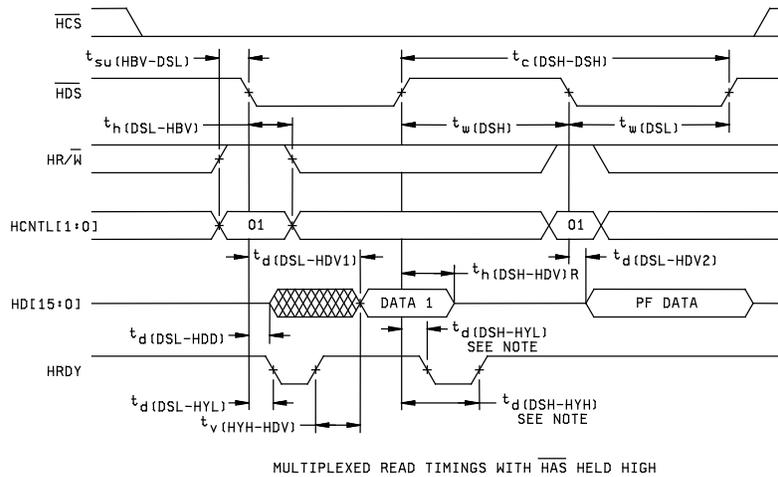
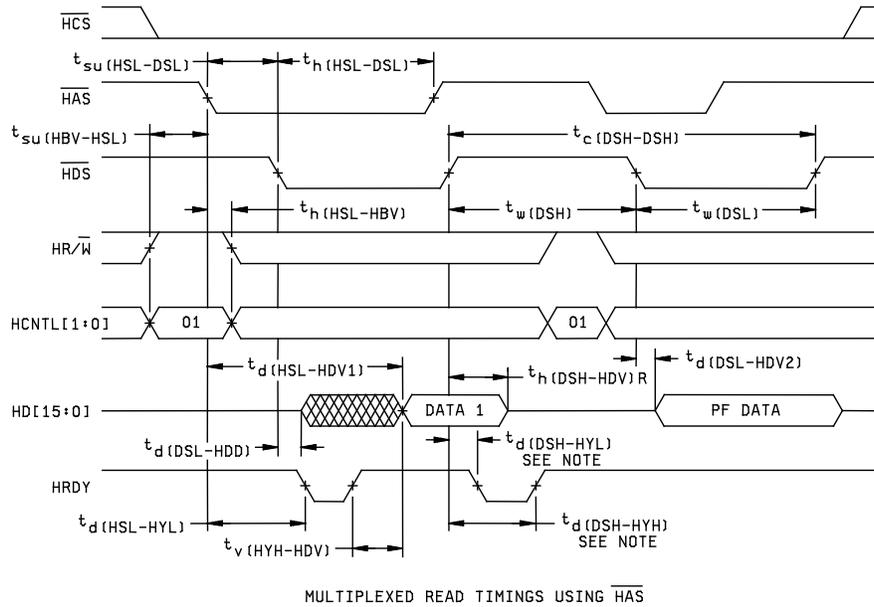


FIGURE 21. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
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Note:  
HRDY goes low at these times only after autoincrement reads.

FIGURE 22. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		REV    A	PAGE    39

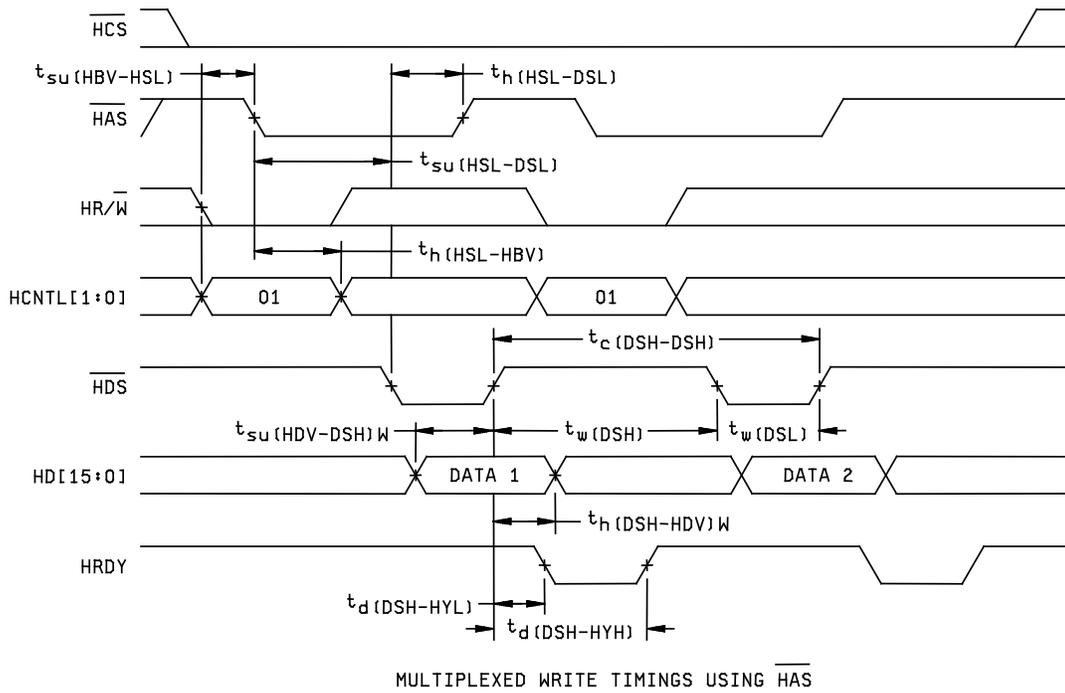


FIGURE 23. Timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. <b>V62/04607</b>
		REV    A	PAGE    40

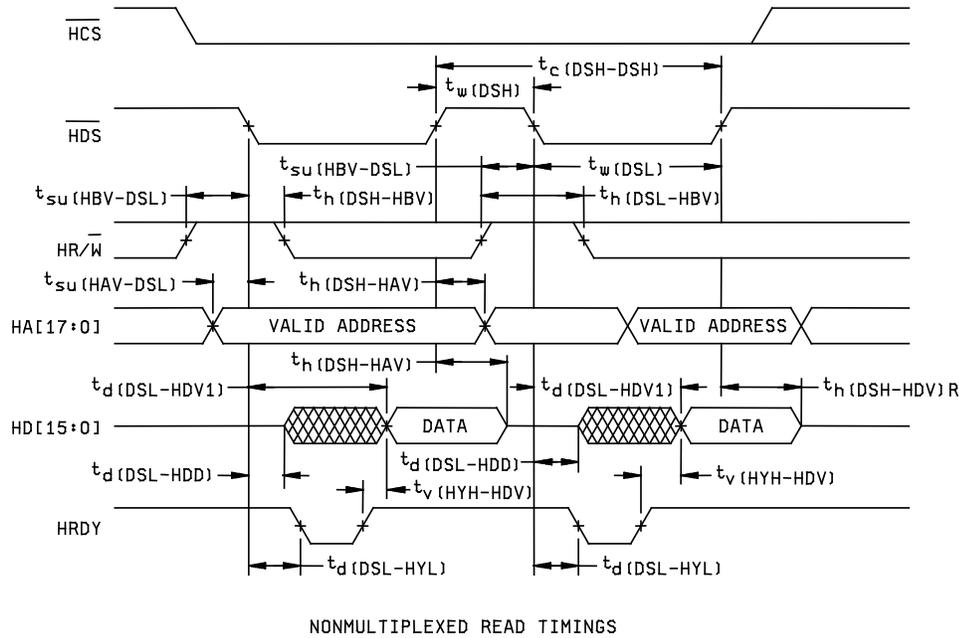
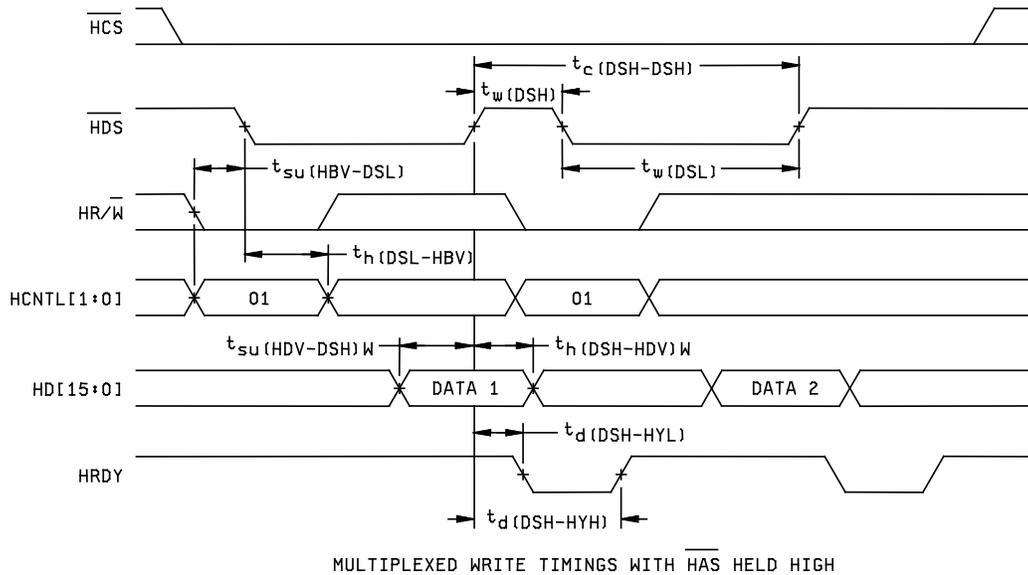


FIGURE 24. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		<b>REV    A</b>	<b>PAGE    41</b>

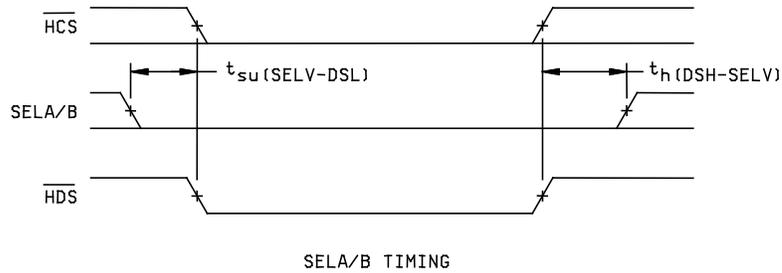
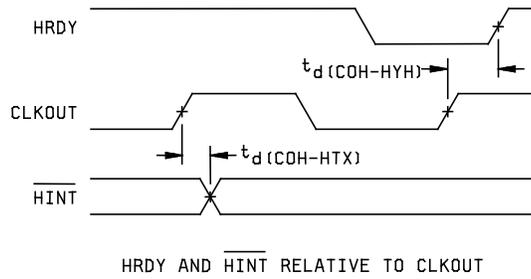
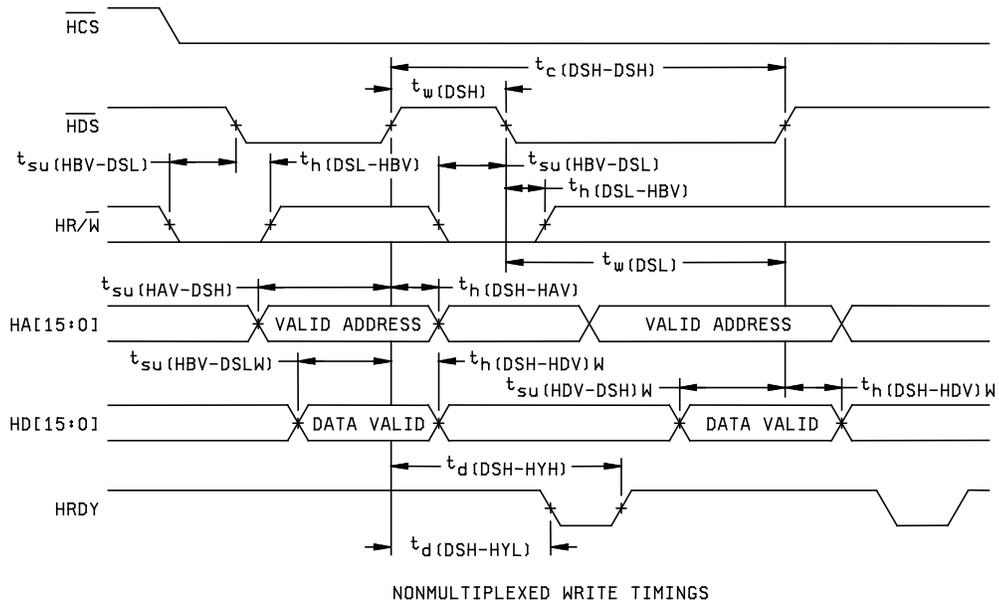


FIGURE 25. Timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/04607
		REV A	PAGE 42

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/04607-01XE	01295	SM320VC5421PGE20EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/04607</b>
		<b>REV      A</b>	<b>PAGE    43</b>