| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPROVED |
| A | Correct lead finish. Update boilerplate. - CFS | 05-11-08 | Thomas M. Hess |
| B | Update boilerplate paragraphs to current requirements. - PHN | 12-03-22 | Thomas M. Hess |
| | | | |

**CURRENT DESIGN ACTIVITY CAGE CODE 16236**
**HAS CHANGED NAMES TO:**
**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **REV** | B | B | B | | | | | | | | | | | | | | | | | | | |
| **PAGE** | 40 | 41 | 42 | | | | | | | | | | | | | | | | | | | |
| **REV** | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B |
| **PAGE** | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 |
| **REV STATUS OF PAGES** | **REV** | | | | | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B |
| | **PAGE** | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |

| | | |
|---|---|---|
| **PMIC N/A** | **PREPARED BY**<br>Phu H. Nguyen | **DEFENSE SUPPLY CENTER, COLUMBUS**<br>**COLUMBUS, OHIO 43218-3990** |
| Original date of drawing<br>YY-MM-DD<br>04-01-28 | **CHECKED BY**<br>Phu H. Nguyen<br>**APPROVED BY**<br>Thomas M. Hess | **TITLE**<br>MICROCIRCUIT, DIGITAL, FIXED POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON |
| | **SIZE** A / **CODE IDENT. NO.** 16236 | **DWG NO.** **V62/04606** |
| | **REV** B | **PAGE** 1 **OF** 42 |

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a fixed point digital signal processor, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/04606 | 01 | X | A |
|---|---|---|---|
| Drawing number | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s). 1/

| Device | Generic number | Circuit function |
|---|---|---|
| 01 | SM320C6201-EP | Fixed point digital signal processor |

1.2.2 Case outline(s). The case outlines are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 352 | JEDEC MO-151/BAR-2 | Plastic ball grid array |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| Z | Other |

1.3 Absolute maximum ratings. 2/

Supply voltage range, ($CV_{DD}$) ..... -0.3 V to +2.3 V 3/
Supply voltage range, ($DV_{DD}$) ..... -0.3 V to +4.0 V 3/
Input voltage range ..... -0.3 V to +4.0 V
Output voltage range ..... -0.3 V to +4.0 V
Operating case temperature ranges, ($T_C$): (A version) ..... -40°C to +105°C
Storage temperature range, ($T_{STG}$)..... -65°C to +150°C

'
-

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.
2/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3/ All voltage values are with respect to $V_{SS}$.

1.4 Recommended operating conditions.

Supply voltage, ($CV_{DD}$) ..... +1.71 V to +1.89 V
Supply voltage, ($DV_{DD}$) ..... +3.14 V to +3.46 V
Supply ground ($V_{SS}$) ..... 0.0 V
High level input voltage, ($V_{IH}$) ..... +2.0 V minimum
Low level input voltage, ($V_{IL}$) ..... +0.8 V maximum
High level output current, ($I_{OH}$) ..... -12 mA maximum
Low level output current, ($I_{OL}$) ..... +12 mA maximum
Operating case temperature ($T_C$) (A version) ..... -40°C to +105°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagram. The block diagram shall be as specified on figure 3.

3.5.4 Load circuit. The load circuit shall be as specified on figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as specified on figure 5-31.

TABLE I. Electrical performance characteristics. 1/

| No. | Test | Symbol | Test condition<br>$-40°C \le T_C \le +105°C$<br>$1.71\ V \le CV_{DD} \le 1.89\ V$<br>$3.14\ V \le DV_{DD} \le 3.46\ V$<br>unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| | High level output voltage | $V_{OH}$ | $DV_{DD}$ = MIN, $I_{OH}$ = MAX | 2.4 | | V |
| | Low level output voltage | $V_{OL}$ | $DV_{DD}$ = MIN, $I_{OL}$ = MAX | | 0.6 | V |
| | Input current 2/ | $I_I$ | $V_I = V_{SS}$ to $DV_{DD}$ | | ±10 | µA |
| | Off state output current | $I_{OZ}$ | $V_O = DV_{DD}$ or 0 V | | ±10 | µA |
| | Supply current, CPU + CPU memory access 3/ | $I_{DD2V}$ | $CV_{DD}$ = NOM,<br>CPU clock = 167 MHz | 380 Typ | | mA |
| | Supply current, peripheral 3/ | $I_{DD2V}$ | $CV_{DD}$ = NOM,<br>CPU clock = 167 MHz | 240 Typ | | mA |
| | Supply current, I/O pins 3/ | $I_{DD3V}$ | $DV_{DD}$ = NOM,<br>CPU clock = 167 MHz | 90 Typ | | mA |
| | Input capacitance | $C_I$ | | | 10 | pF |
| | Output capacitance | $C_O$ | | | 10 | pF |

| No. | Test | Symbol | Test condition<br>$-40°C \le T_C \le +105°C$<br>$1.71\ V \le CV_{DD} \le 1.89\ V$<br>$3.14\ V \le DV_{DD} \le 3.46\ V$<br>unless otherwise noted | Limits | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | CLKMODE = x4 | | CLKMODE = x1 | | |
| | | | | Min | Max | Min | Max | |
| **INPUT AND OUTPUT CLOCKS** | | | | | | | | |
| **Timing requirements for CLKIN 4/ 5/** | | | | | | | | |
| 1 | Cycle time, CLKIN | $t_{c(CLKIN)}$ | See figure 7 | 20 | | 5 | | ns |
| 2 | Pulse duration, CLKIN high | $t_{w(CLKINH)}$ | | 0.4C | | 0.45C | | |
| 3 | Pulse duration, CLKIN low | $t_{w(CLKINL)}$ | | 0.4C | | 0.45C | | |
| 4 | Transition time, CLKIN | $t_{t(CLKIN)}$ | | | 5 | | 0.6 | |
| **Switching characteristics over recommended operating conditions for CLKOUT1 4/ 6/ 7/** | | | | | | | | |
| 1 | Cycle time, CLKOUT1 | $t_{c(CKO1)}$ | See figure 8 | P-0.7 | P+0.7 | P-0.7 | P+0.7 | ns |
| 2 | Pulse duration, CLKOUT1 high | $t_{w(CKO1H)}$ | | (P/2)-0.5 | (P/2)+0.5 | PH-0.5 | PH+0.5 | |
| 3 | Pulse duration, CLKOUT1 low | $t_{w(CKO1L)}$ | | (P/2)-0.5 | (P/2)+0.5 | PL-0.5 | PL+0.5 | |
| 4 | Transition time, CLKOUT1 | $t_{t(CKO1)}$ | | | 0.6 | | 0.6 | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| | **INPUT AND OUTPUT CLOCKS (CONTINUED)** | | | | | |
| | **Switching characteristic over recommended operating conditions for CLKOUT2** 4/ 6/ | | | | | |
| 1 | Cycle time, CLKOUT | $t_{c(CKO2)}$ | See figure 9 | 2P–0.7 | 2P+0.7 | ns |
| 2 | Pulse duration, CLKOUT2 high | $t_{w(CKO2H)}$ | | P–0.7 | P+0.7 | |
| 3 | Pulse duration, CLKOUT2 low | $t_{w(CKO2L)}$ | | P–0.7 | P+0.7 | |
| 4 | Transition time, CLKOUT2 | $t_{t(CKO2)}$ | | | 0.6 | |
| | **Switching characteristics over recommended operating conditions for the relation of SSCLK, SDCLK, and CLKOUT2 to CLKOUT1** 6/ | | | | | |
| 1 | Delay time, CLKOUT1 edge to SSCLK edge | $t_{d(CKO1-SSCLK)}$ | See figure 10 | (P/2)+0.2 | (P/2)+4.2 | ns |
| 2 | Delay time, CLKOUT1 edge to SSCLH edge (1/2 clock rate) | $t_{d(CKO1-SSCLK1/2)}$ | | (P/2)-1 | (P/2)+2.4 | |
| 3 | Delay time, CLKOUT1 edge to CLKOUT2 edge | $t_{d(CKO1-CKO2)}$ | | (P/2)-1 | (P/2)+2.4 | |
| 4 | Delay time, CLKOUT1 edge to SDCLK edge | $t_{d(CKO1-SDCLK)}$ | | (P/2)-1 | (P/2)+2.4 | |
| | **ASYNCHRONOUS MEMORY TIMING** | | | | | |
| | **Timing requirements for asynchronous memory cycles** 8/ | | | | | |
| 6 | Setup time, read EDx valid before CLKOUT1 high | $t_{su(EDV-CKO1H)}$ | See figure 11 | 4 | | ns |
| 7 | Hold time, read EDx valid after CLKOUT1 high | $t_{h(CKO1H-EDV)}$ | | 0.8 | | |
| 10 | Setup time, ARDY valid before CLKOUT1 high | $t_{su(ARDY-CKO1H)}$ | | 3 | | |
| 11 | Hold time, read ARDY valid after CLKOUT1 high | $t_{h(CKO1H-ARDY)}$ | | 1.8 | | |
| | **Switching characteristics over recommended operating conditions for asynchronous memory cycles** 9/ | | | | | |
| 1 | Delay time, CLKOUT1 high to $\overline{CEx}$ valid | $t_{d(CKO1H-CEV)}$ | See figure 11 | -0.2 | 4 | ns |
| 2 | Delay time, CLKOUT1 high to $\overline{BEx}$ valid | $t_{d(CKO1H-BEV)}$ | | | 4 | |
| 3 | Delay time, CLKOUT1 high to $\overline{BEx}$ invalid | $t_{d(CKO1H-BEIV)}$ | | -0.2 | | |
| 4 | Delay time, CLKOUT1 high to EAx valid | $t_{d(CKO1H-EAV)}$ | | | 4 | |
| 5 | Delay time, CLKOUT1 high to EAx invalid | $t_{d(CKO1H-EAIV)}$ | | -0.2 | | |
| 8 | Delay time, CLKOUT1 high to $\overline{AOE}$ valid | $t_{d(CKO1H-AOEV)}$ | | -0.2 | 4 | |
| 9 | Delay time, CLKOUT1 high to $\overline{ARE}$ valid | $t_{d(CKO1H-AREV)}$ | | -0.2 | 4 | |
| 12 | Delay time, CLKOUT1 high to EDx valid | $t_{d(CKO1H-EDV)}$ | | | 4 | |
| 13 | Delay time, CLKOUT1 high to EDx invalid | $t_{d(CKO1H-EDIV)}$ | | -0.2 | | |
| 14 | Delay time, CLKOUT1 high to $\overline{AWE}$ valid | $t_{d(CKO1H-AWEV)}$ | | -0.2 | 4 | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| | **SYNCHRONOUS BURST MEMORY TIMING** | | | | | |
| **Timing requirements for synchronous burst SRAM cycles (full rate SSCLK)** | | | | | | |
| 7 | Setup time, read EDx valid before SSCLK high | $t_{su(EDV-SSCLKH)}$ | See figure 12 | 1.5 | | ns |
| 8 | Hold time, read EDx valid after SSCLK high | $t_{h(SSCLKH-EDV)}$ | | 1.5 | | |
| **Switching characteristics over recommended operating conditions for synchronous burst SRAM cycles (full rate SSCLK)** 10/ | | | | | | |
| 1 | Output setup time, $\overline{CEx}$ valid before SSCLK high | $t_{osu(CEV-SSCLKH)}$ | See figure 12 | 0.5P-1.3 | | ns |
| 2 | Output hold time, $\overline{CEx}$ valid after SSCLK high | $t_{oh(SSCLKH-CEV)}$ | | 0.5P-2.3 | | |
| 3 | Output setup time, $\overline{BEx}$ valid before SSCLK high | $t_{osu(BEV-SSCLKH)}$ | | 0.5P-1.3 | | |
| 4 | Output hold time, $\overline{BEx}$ invalid after SSCLK high | $t_{oh(SSCLKH-BEIV)}$ | | 0.5P-2.3 | | |
| 5 | Output setup time, EAx valid before SSCLK high | $t_{osu(EAV-SSCLKH)}$ | | 0.5P-1.3 | | |
| 6 | Output hold time, EAx invalid after SSCLK high | $t_{oh(SSCLKH-EAIV)}$ | | 0.5P-2.3 | | |
| 9 | Output setup time, $\overline{SSADS}$ valid before SSCLK high | $t_{osu(ADSV-SSCLKH)}$ | | 0.5P-1.3 | | |
| 10 | Output hold time, $\overline{SSADS}$ valid after SSCLK high | $t_{oh(SSCLKH-ADSV)}$ | | 0.5P-2.3 | | |
| 11 | Output setup time, $\overline{SSOE}$ valid before SSCLK high | $t_{osu(OEV-SSCLKH)}$ | | 0.5P-1.3 | | |
| 12 | Output hold time, $\overline{SSOE}$ valid after SSCLK high | $t_{oh(SSCLKH-OEV)}$ | | 0.5P-2.3 | | |
| 13 | Output setup time, EDx valid before SSCLK high | $t_{osu(EDV-SSCLKH)}$ | | 0.5P-1.3 | | |
| 14 | Output hold time, EDx invalid after SSCLK high | $t_{oh(SSCLKH-EDIV)}$ | | 0.5P-2.3 | | |
| 15 | Output setup time, $\overline{SSWE}$ valid before SSCLK high | $t_{osu(WEV-SSCLKH)}$ | | 0.5P-1.3 | | |
| 16 | Output hold time, $\overline{SSWE}$ valid after SSCLK high | $t_{oh(SSCLKH-WEV)}$ | | 0.5P-2.3 | | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **SYNCHRONOUS BURST MEMORY TIMING – (CONTINUED)** | | | | | | |
| **Timing requirements for synchronous burst SRAM cycles (half rate SSCLK)** | | | | | | |
| 7 | Setup time, read EDx valid before SSCLK high | $t_{su(EDV-SSCLKH)}$ | See figure 13 | 2.5 | | ns |
| 8 | Hold time, read EDx valid after SSCLK high | $t_{h(SSCLKH-EDV)}$ | | 1.5 | | |
| **Switching characteristics over recommended operating conditions for synchronous burst SRAM cycles (half rate SSCLK)** 11/ | | | | | | |
| 1 | Output setup time, $\overline{CEx}$ valid before SSCLK high | $t_{osu(CEV-SSCLKH)}$ | See figure 13 | 1.5P-3 | | ns |
| 2 | Output hold time, $\overline{CEx}$ valid after SSCLK high | $t_{oh(SSCLKH-CEV)}$ | | 0.5P-1.5 | | |
| 3 | Output setup time, $\overline{BEx}$ valid before SSCLK high | $t_{osu(BEV-SSCLKH)}$ | | 1.5P-3 | | |
| 4 | Output hold time, $\overline{BEx}$ invalid after SSCLK high | $t_{oh(SSCLKH-BEIV)}$ | | 0.5P-1.5 | | |
| 5 | Output setup time, EAx valid before SSCLK high | $t_{osu(EAV-SSCLKH)}$ | | 1.5P-3 | | |
| 6 | Output hold time, EAx invalid after SSCLK high | $t_{oh(SSCLKH-EAIV)}$ | | 0.5P-1.5 | | |
| 9 | Output setup time, $\overline{SSADS}$ valid before SSCLK high | $t_{osu(ADSV-SSCLKH)}$ | | 1.5P-3 | | |
| 10 | Output hold time, $\overline{SSADS}$ valid after SSCLK high | $t_{oh(SSCLKH-ADSV)}$ | | 0.5P-1.5 | | |
| 11 | Output setup time, $\overline{SSOE}$ valid before SSCLK high | $t_{osu(OEV-SSCLKH)}$ | | 1.5P-3 | | |
| 12 | Output hold time, $\overline{SSOE}$ valid after SSCLK high | $t_{oh(SSCLKH-OEV)}$ | | 0.5P-1.5 | | |
| 13 | Output setup time, EDx valid before SSCLK high | $t_{osu(EDV-SSCLKH)}$ | | 1.5P-3 | | |
| 14 | Output hold time, EDx invalid after SSCLK high | $t_{oh(SSCLKH-EDIV)}$ | | 0.5P-1.5 | | |
| 15 | Output setup time, $\overline{SSWE}$ valid before SSCLK high | $t_{osu(WEV-SSCLKH)}$ | | 1.5P-3 | | |
| 16 | Output hold time, $\overline{SSWE}$ valid after SSCLK high | $t_{oh(SSCLKH-WEV)}$ | | 0.5P-1.5 | | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| | **SYNCHRONOUS DRAM TIMING** | | | | | |
| **Timing requirements for synchronous DRAM cycles** | | | | | | |
| 7 | Setup time, read EDx valid before SDCLK high | $t_{su(EDV-SDCLKH)}$ | See figure 14 | 0.5 | | ns |
| 8 | Hold time, read EDx valid after SDCLK high | $t_{h(SDCLKH-EDV)}$ | | 3 | | |
| **Switching characteristics over recommended operating conditions for synchronous DRAM cycles** 11/ | | | | | | |
| 1 | Output setup time, $\overline{CEx}$ valid before SDCLK high | $t_{osu(CEV-SDCLKH)}$ | See figure 14-16 | 1.5P-3.5 | | ns |
| 2 | Output hold time, $\overline{CEx}$ valid after SDCLK high | $t_{oh(SDCLKH-CEV)}$ | | 0.5P-1 | | |
| 3 | Output setup time, $\overline{BEx}$ valid before SDCLK high | $t_{osu(BEV-SDCLKH)}$ | | 1.5P-3.5 | | |
| 4 | Output hold time, $\overline{BEx}$ invalid after SDCLK high | $t_{oh(SDCLKH-BEIV)}$ | | 0.5P-1 | | |
| 5 | Output setup time, EAx valid before SDCLK high | $t_{osu(EAV-SDCLKH)}$ | | 1.5P-3.5 | | |
| 6 | Output hold time, EAx invalid after SDCLK high | $t_{oh(SDCLKH-EAIV)}$ | | 0.5P-1 | | |
| 9 | Output setup time, $\overline{SDCAS}$ valid before SDCLK high | $t_{osu(SDCAS-SDCLKH)}$ | | 1.5P-3.5 | | |
| 10 | Output hold time, $\overline{SDCAS}$ valid after SDCLK high | $t_{oh(SDCLKH-SDCAS)}$ | | 0.5P-1 | | |
| 11 | Output setup time, EDx valid before SDCLK high | $t_{osu(EDV-SDCLKH)}$ | | 1.5P-3.5 | | |
| 12 | Output hold time, EDx invalid after SDCLK high | $t_{oh(SDCLKH-EDIV)}$ | | 0.5P-1 | | |
| 13 | Output setup time, $\overline{SDWE}$ valid before SDCLK high | $t_{osu(SDWE-SDCLKH)}$ | | 1.5P-3.5 | | |
| 14 | Output hold time, $\overline{SDWE}$ valid after SDCLK high | $t_{oh(SDCLKH-SDWE)}$ | | 0.5P-1 | | |
| 15 | Output setup time, SDA10 valid before SDCLK high | $t_{osu(SDA10V-SDCLKH)}$ | | 1.5P-3.5 | | |
| 16 | Output hold time, SDA10 valid after SDCLK high | $t_{oh(SDCLKH-SDA10IV)}$ | | 0.5P-1 | | |
| 17 | Output setup time, $\overline{SDRAS}$ valid before SDCLK high | $t_{osu(SDRAS-SDCLKH)}$ | | 1.5P-3.5 | | |
| 18 | Output hold time, $\overline{SDRAS}$ valid after SDCLK high | $t_{oh(SDCLKH-SDRAS)}$ | | 0.5P-1 | | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| | **$\overline{HOLD}$ AND $\overline{HOLDA}$ TIMINGS** | | | | | |
| **Timing requirements for the $\overline{HOLD}$ / $\overline{HOLDA}$ cycles** 12/ | | | | | | |
| 1 | Setup time, $\overline{HOLD}$ high before CLKOUT1 high | $t_{su(HOLDH-CKO1H)}$ | See figure 17 | 1 | | ns |
| 2 | Hold time, $\overline{HOLD}$ low after CLKOUT1 high | $t_{h(CKO1H-HOLDL)}$ | | 4 | | |
| **Switching characteristics over recommended operating conditions for the $\overline{HOLD}$ / $\overline{HOLDA}$ cycles** 6/ | | | | | | |
| 3 | Delay time, $\overline{HOLD}$ low to EMIF bus high impedance | $t_{d(HOLDL-BHZ)}$ | See figure 17 | 4P | 13/ | ns |
| 4 | Delay time, EMIF bus high impedance to $\overline{HOLDA}$ low | $t_{d(BHZ-HOLDAL)}$ | | P | 2P | |
| 5 | Delay time, $\overline{HOLD}$ high to $\overline{HOLDA}$ high | $t_{d(HOLDH-HOLDAH)}$ | | 4P | 7P | |
| 6 | Delay time, CLKOUT1 high to $\overline{HOLDA}$ valid | $t_{d(CKO1H-HOLDAL)}$ | | 1 | 8 | |
| 7 | Delay time, CLKOUT1 high to EMIF bus high impedance 14/ | $t_{d(CKO1H-BHZ)}$ | | 3 | 11 | |
| 8 | Delay time, CLKOUT1 high to EMIF bus low impedance 14/ | $t_{d(CKO1H-BLZ)}$ | | 3 | 11 | |
| 9 | Delay time, HOLD high to EMIF bus low impedance | $t_{d(HOLDH-BLZ)}$ | | 3P | 6P | |
| | **RESET TIMING** | | | | | |
| **Timing requirements for reset** | | | | | | |
| 1 | Width of the $\overline{RESET}$ pulse (PLL stable) 15/ | $t_{w(RST)}$ | See figure 18 | 10 | | 17/ |
| | Width of the $\overline{RESET}$ pulse (PLL needs to sync up) 16/ | | | 250 | | µs |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **RESET TIMING – (CONTINUED)** | | | | | | |
| **Switching characteristics over recommended operating conditions during reset** 18/ 19/ | | | | | | |
| 2 | Response time to change of value $\overline{RESET}$ signal | $t_{R(RST)}$ | See figure 18 | 2 | | 17/ |
| 3 | Delay time, CLKOUT1 high to CLKOUT2 invalid | $t_{d(CKO1H-CKO2IV)}$ | | -1 | | ns |
| 4 | Delay time, CLKOUT1 high to CLKOUT2 valid | $t_{d(CKO1H-CKO2V)}$ | | | 10 | |
| 5 | Delay time, CLKOUT1 high to SDCLK invalid | $t_{d(CKO1H-SDCLKIV)}$ | | -1 | | |
| 6 | Delay time, CLKOUT1 high to SDCLK valid | $t_{d(CKO1H-SDCLKV)}$ | | | 10 | |
| 7 | Delay time, CLKOUT1 high to SSCLK invalid | $t_{d(CKO1H-SSCKIV)}$ | | -1 | | |
| 8 | Delay time, CLKOUT1 high to SSCLK valid | $t_{d(CKO1H-SSCKV)}$ | | | 10 | |
| 9 | Delay time, CLKOUT1 high to low group invalid | $t_{d(CKO1H-LOWIV)}$ | | -1 | | |
| 10 | Delay time, CLKOUT1 high to low group valid | $t_{d(CKO1H-LOWV)}$ | | | 10 | |
| 11 | Delay time, CLKOUT1 high to high group invalid | $t_{d(CKO1H-HIGHIV)}$ | | -1 | | |
| 12 | Delay time, CLKOUT1 high to high group valid | $t_{d(CKO1H-HIGHV)}$ | | | 10 | |
| 13 | Delay time, CLKOUT1 high to Z group high impedance | $t_{d(CKO1H-ZHZ)}$ | | -1 | | |
| 14 | Delay time, CLKOUT1 high to Z group valid | $t_{d(CKO1H-ZV)}$ | | | 10 | |
| **EXTERNAL INTERRUPT TIMING** | | | | | | |
| **Timing requirements for interrupt response cycles** 6/ 20/ | | | | | | |
| 2 | Width of the interrupt pulse low | $t_{w(ILOW)}$ | See figure 19 | 2P | | ns |
| 3 | Width of the interrupt pulse high | $t_{w(IHIGH)}$ | | 2P | | |
| **Switching characteristics over recommended operating conditions during interrupt response cycles** 21/ | | | | | | |
| 1 | Delay time, EXT_INTx high to IACK high | $t_{d(EINTH-IACKH)}$ | See figure 19 | 9P | | ns |
| 4 | Delay time, CLKOUT2 low to IACK valid | $t_{d(CKO2L-IACKV)}$ | | -4 | 6 | |
| 5 | Delay time, CLKOUT2 low to INUMx valid | $t_{d(CKO2L-INUMV)}$ | | | 6 | |
| 6 | Delay time, CLKOUT2 low to INUMx invalid | $t_{d(CKO2L-INUMIV)}$ | | -4 | | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|
| | **HOST PORT INTERFACE TIMING** | | | | | |
| | **Timing requirements for host port interface cycles** 22/ 23/ | | | | | |
| 1 | Setup time, select signal 24/ valid before $\overline{HSTROBE}$ low | $t_{su(SEL-HSTBL)}$ | See figure 20 and 21 | 4 | | ns |
| 2 | Hold time, select signal 24/ valid after $\overline{HSTROBE}$ low | $t_{h(HSTBL-SEL)}$ | | 2 | | |
| 3 | Pulse duration, $\overline{HSTROBE}$ low | $t_{w(HSTBL)}$ | | 2P | | |
| 4 | Pulse duration, $\overline{HSTROBE}$ high between consecutive accesses | $t_{w(HSTBH)}$ | | 2P | | |
| 10 | Setup time, select signal 24/ valid before $\overline{HAS}$ low | $t_{su(SEL-HASL)}$ | | 4 | | |
| 11 | Hold time, select signal 24/ valid after $\overline{HAS}$ low | $t_{h(HASL-SEL)}$ | | 2 | | |
| 12 | Setup time, host data valid before $\overline{HSTROBE}$ low | $t_{su(HDV-HSTBH)}$ | | 3 | | |
| 13 | Hold time, host data valid after $\overline{HSTROBE}$ low | $t_{h(HSTBH-HDV)}$ | | 2 | | |
| 14 | Hold time, $\overline{HSTROBE}$ low after $\overline{HRDY}$ low. $\overline{HSTROBE}$ should not be inactivated until $\overline{HRDY}$ is active (low); otherwise, HPI writes will not complete properly. | $t_{h(HRDYL-HSTBL)}$ | | 1 | | |
| 18 | Setup time, $\overline{HAS}$ low before $\overline{HSTROBE}$ low | $t_{su(HASL-HSTBL)}$ | | 2 | | |
| 19 | Hold time, $\overline{HAS}$ low after $\overline{HSTROBE}$ low | $t_{h(HSTBL-HASL)}$ | | 2 | | |
| | **Switching characteristics over recommended operating conditions during host port interface cycles** 22/ 23/ | | | | | |
| 5 | Delay time, $\overline{HCS}$ to $\overline{HRDY}$ 25/ | $t_{d(HCS-HRDY)}$ | See figure 20 and 21 | 1 | 9 | ns |
| 6 | Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ high 26/ | $t_{d(HSTBL-HRDYH)}$ | | 3 | 12 | |
| 7 | Output hold time, HD low impedance after $\overline{HSTROBE}$ low for an HPI read | $t_{oh(HSTBL-HDLZ)}$ | | 4 | | |
| 8 | Delay time, HD valid to $\overline{HRDY}$ low | $t_{d(HDV-HRDYL)}$ | | P-3 | P+3 | |
| 9 | Output hold time, HD valid after $\overline{HSTROBE}$ high | $t_{oh(HSTBL-HDV)}$ | | 2 | 12 | |
| 15 | Delay time, $\overline{HSTROBE}$ high to HD high impedance | $t_{d(HSTBH-HDHZ)}$ | | 3 | 12 | |
| 16 | Delay time, $\overline{HSTROBE}$ low to HD valid | $t_{d(HSTBL-HDV)}$ | | 2 | 12 | |
| 17 | Delay time, $\overline{HSTROBE}$ high to $\overline{HRDY}$ high 27/ | $t_{d(HSTBH-HRDYH)}$ | | 3 | 12 | |
| 20 | Delay time, $\overline{HAS}$ low to $\overline{HRDY}$ high | $t_{d(HASL-HRDYH)}$ | | 3 | 12 | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| | **MULTICHANNEL BUFFERED SERIAL PORT TIMING** | | | | | | |
| **Timing requirements for McBSP** 6/ 28/ | | | | | | | |
| 2 | Cycle time, CLKR/X | $t_{c(CKRX)}$ | See figure 22 | CLKR/X ext | 2P 29/ | | ns |
| 3 | Pulse duration, CLKR/X high or CLKR/X low | $t_{w(CKRX)}$ | | CLKR/X ext | P-1 30/ | | |
| 5 | Setup time, external FSR high before CLKR low | $t_{su(FRH-CKRL)}$ | | CLKR int | 9 | | |
| | | | | CLKR ext | 2 | | |
| 6 | Hold time, external FSR high after CLKR low | $t_{h(CKRL-FRH)}$ | | CLKR int | 6 | | |
| | | | | CLKR ext | 3 | | |
| 7 | Setup time, DR valid before CLKR low | $t_{su(DRV-CKRL)}$ | | CLKR int | 8 | | |
| | | | | CLKR ext | 0 | | |
| 8 | Hold time, DR valid after CLKR low | $t_{h(CKRL-DRV)}$ | | CLKR int | 3 | | |
| | | | | CLKR ext | 4 | | |
| 10 | Setup time, external FSR high before CLKX low | $t_{su(FXH-CKXL)}$ | | CLKR int | 9 | | |
| | | | | CLKR ext | 2 | | |
| 11 | Hold time, external FSR high after CLKX low | $t_{h(CKXL-FXH)}$ | | CLKR int | 6 | | |
| | | | | CLKR ext | 3 | | |
| **Switching characteristics over recommended operating conditions for McBSP** 6/ 28/ 31/ | | | | | | | |
| 1 | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | $t_{d(CKSH-CKRXH)}$ | See figure 22 | | 3 | 10 | ns |
| 2 | Cycle time, CLKR/X | $t_{c(CKRX)}$ | | CLKR/X int | 2P 29/ | | |
| 3 | Pulse duration, CLKR/X high or CLKR/X low | $t_{w(CKRX)}$ | | CLKR/X int | C-1.3 32/ | C+1 32/ | |
| 4 | Delay time, CLKR high to internal FSR valid | $t_{d(CKRH-FRV)}$ | | CLKR int | -2 | 3 | |
| 9 | Delay time, CLKX high to internal FSX valid | $t_{d(CKXH-FXV)}$ | | CLKR int | -2 | 3 | |
| | | | | CLKR ext | 3 | 9 | |
| 12 | Disable time, DX high impedance following last data bit from CLKX high | $t_{dis(CKXH-DXHZ)}$ | | CLKR int | -1 | 4 | |
| | | | | CLKR ext | 3 | 9 | |
| 13 | Delay time, CLKX high to DX valid | $t_{d(CKXH-DXV)}$ | | CLKR int | -1 | 4 | |
| | | | | CLKR ext | 3 | 9 | |
| 14 | Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode | $t_{d(FXH-DXV)}$ | | CLKR int | -1 | 3 | |
| | | | | CLKR ext | 3 | 9 | |
| **Timing requirements for FSR when GSYNC = 1** | | | | | | | |
| 1 | Setup time, FSR high before CLKS high | $t_{su(FRHJ-CKSH)}$ | See figure 23 | | 4 | | ns |
| 2 | Hold time, FSR high after CLKS high | $t_{h(CKSH-FRH)}$ | | | 4 | | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Master | | Slave | | |
| | | | | Min | Max | Min | Max | |
| **MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)** | | | | | | | | |
| **Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0** 6/ 33/ | | | | | | | | |
| 4 | Setup time, DR valid before CLKX low | $t_{su(DRV-CKXL)}$ | See figure 24 | 12 | | 2-3P | | ns |
| 5 | Hold time, DR valid after CLKX low | $t_{h(CKXL-DRV)}$ | | 4 | | 5+6P | | |
| **Switching characteristics over recommended operating conditions for McBSP as SPI slave: CLKSTP = 10b, CLKXP = 0** 6/ 33/ | | | | | | | | |
| 1 | Hold time, FSX low after CLKX low 34/ | $t_{h(CKXL-FXL)}$ | See figure 24 | T-2 | T+3 | | | ns |
| 2 | Delay time, FSX low to CLKX high 35/ | $t_{d(FXL-CKXH)}$ | | L-2 | L+3 | | | |
| 3 | Delay time, CLKX high to DX valid | $t_{d(CKXH-DXV)}$ | | -2 | 4 | 3P+4 | 5P+17 | |
| 6 | Disable time, DX high impedance following last data bit from CLKX low | $t_{dis(CKXL-DXHZ)}$ | | L-2 | L+3 | | | |
| 7 | Disable time, DX high impedance following last data bit from FSX high | $t_{dis(FXH-DXHZ)}$ | | | | P+3 | 3P+17 | |
| 8 | Delay time, FSX low to DX valid | $t_{d(FXL-DXV)}$ | | | | 2P+2 | 4P+17 | |
| **Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0** 6/ 33/ | | | | | | | | |
| 4 | Setup time, DR valid before CLKX high | $t_{su(DRV-CKXH)}$ | See figure 25 | 12 | | 2-3P | | ns |
| 5 | Hold time, DR valid after CLKX high | $t_{h(CKXH-DRV)}$ | | 4 | | 5+6P | | |
| **Switching characteristics over recommended operating conditions for McBSP as SPI slave: CLKSTP = 11b, CLKXP = 0** 6/ 33/ | | | | | | | | |
| 1 | Hold time, FSX low after CLKX low 34/ | $t_{h(CKXL-FXL)}$ | See figure 25 | L-2 | L+3 | | | ns |
| 2 | Delay time, FSX low to CLKX high 35/ | $t_{d(FXL-CKXH)}$ | | T-2 | T+3 | | | |
| 3 | Delay time, CLKX low to DX valid | $t_{d(CKXL-DXV)}$ | | -2 | 4 | 3P+4 | 5P+17 | |
| 6 | Disable time, DX high impedance following last data bit from CLKX low | $t_{dis(CKXL-DXHZ)}$ | | -2 | 4 | 3P+3 | 5P+17 | |
| 7 | Delay time, FSX low to DX valid | $t_{d(FXL-DXV)}$ | | H-2 | H+4 | 2P+2 | 4P+17 | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Master | | Slave | | |
| | | | | Min | Max | Min | Max | |
| **MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)** | | | | | | | | |
| **Timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1** 6/ 33/ | | | | | | | | |
| 4 | Setup time, DR valid before CLKX high | $t_{su(DRV-CKXH)}$ | See figure 26 | 12 | | 2-3P | | ns |
| 5 | Hold time, DR valid after CLKX high | $t_{h(CKXH-DRV)}$ | | 4 | | 5+6P | | |
| **Switching characteristics over recommended operating conditions for McBSP as SPI slave: CLKSTP = 10b, CLKXP = 1** 6/ 33/ | | | | | | | | |
| 1 | Hold time, FSX low after CLKX high 34/ | $t_{h(CKXH-FXL)}$ | See figure 26 | T-2 | T+3 | | | ns |
| 2 | Delay time, FSX low to CLKX low 35/ | $t_{d(FXL-CKXL)}$ | | H-2 | H+3 | | | |
| 3 | Delay time, CLKX low to DX valid | $t_{d(CKXL-DXV)}$ | | -2 | 4 | 3P+4 | 5P+17 | |
| 6 | Disable time, DX high impedance following last data bit from CLKX high | $t_{dis(CKXH-DXHZ)}$ | | H-2 | H+3 | | | |
| 7 | Disable time, DX high impedance following last data bit from FSX high | $t_{dis(FXH-DXHZ)}$ | | | | P+3 | 3P+17 | |
| 8 | Delay time, FSX low to DX valid | $t_{d(FXL-DXV)}$ | | | | 2P+2 | 4P+17 | |
| **Timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1** 6/ 33/ | | | | | | | | |
| 4 | Setup time, DR valid before CLKX low | $t_{su(DRV-CKXL)}$ | See figure 27 | 12 | | 2-3P | | ns |
| 5 | Hold time, DR valid after CLKX low | $t_{h(CKXL-DRV)}$ | | 4 | | 5+6P | | |
| **Switching characteristics over recommended operating conditions for McBSP as SPI slave: CLKSTP = 11b, CLKXP = 1** 6/ 33/ | | | | | | | | |
| 1 | Hold time, FSX low after CLKX high 34/ | $t_{h(CKXH-FXL)}$ | See figure 27 | H-2 | H+3 | | | ns |
| 2 | Delay time, FSX low to CLKX low 35/ | $t_{d(FXL-CKXL)}$ | | T-2 | T+1 | | | |
| 3 | Delay time, CLKX high to DX valid | $t_{d(CKXH-DXV)}$ | | -2 | 4 | 3P+4 | 5P+17 | |
| 6 | Disable time, DX high impedance following last data bit from CLKX high | $t_{dis(CKXH-DXHZ)}$ | | -2 | 4 | 3P+3 | 5P+17 | |
| 7 | Delay time, FSX low to DX valid | $t_{d(FXL-DXV)}$ | | L-2 | L+4 | 2P+2 | 4P+17 | |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test condition $-40°C \le T_C \le +105°C$ $1.71\ V \le CV_{DD} \le 1.89\ V$ $3.14\ V \le DV_{DD} \le 3.46\ V$ unless otherwise noted | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| | **DMAC, TIMER, POWER DOWN TIMING** | | | | | |
| **Switching characteristics over recommended operating conditions for DMAC outputs** | | | | | | |
| 1 | Delay time, CLKOUT1 high to DMAC valid | $t_{d(CKO1H-DMACV)}$ | See figure 28 | 2 | 10 | ns |
| **Timing requirements for timing inputs** 6/ | | | | | | |
| 1 | Pulse duration, TINP high or low | $t_{w(TINP)}$ | See figure 29 | 2P | | ns |
| **Switching characteristics over recommended operating conditions for time outputs** | | | | | | |
| 2 | Delay time, CLKOUT1 high to TOUT valid | $t_{d(CKO1H-TOUTV)}$ | See figure 29 | 2 | 9 | ns |
| **Switching characteristics over recommended operating conditions for power-down outputs** | | | | | | |
| 1 | Delay time, CLKOUT1 high to PD valid | $t_{d(CKO1H-PDV)}$ | See figure 30 | 2 | 9 | ns |
| | **JTAG TEST PORT TIMING** | | | | | |
| **Timing requirements for JTAG test port** | | | | | | |
| 1 | Cycle time, TCK | $t_{c(TCK)}$ | See figure 31 | 35 | | ns |
| 3 | Setup time, TDI/TMS/ $\overline{TRST}$ valid before TCK high | $t_{su(TDIV-TCKH)}$ | | 10 | | |
| 4 | Hold time, TDI/TMS/ $\overline{TRST}$ valid after TCK high | $t_{h(TCKH-TDIV)}$ | | 9 | | |
| **Switching characteristics over recommended operating conditions for JTAG test port** | | | | | | |
| 2 | Delay time, TCK low to TDO valid | $t_{d(TCKL-TDOV)}$ | See figure 31 | -3 | 12 | ns |

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ TMS and TDI are not included due to internal pullups. $\overline{TRST}$ is not included due to internal pulldown.

3/ Measured with average activity (50% high / 50% low power). For more details on CPU, peripheral, and I/O activity, see the TMS320C6000 Power consumption Summary application report.

4/ The reference points for the rise and fall transactions are measured at $V_{IL}$ max and $V_{IH}$ min.

5/ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 50 MHz, use C = 20 ns.

6/ P = 1/CPU clock frequency in nanoseconds (ns). For example, when running parts at 200 MHz, use P = 5 ns.

7/ PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.

8/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be asynchronous input.

9/ The minimum delay is also the minimum output hold after CLKOUT1 high.

10/ When the PLL is used (CLKMODE x4), P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns. For CLKMODE x1, 0.5P is defined as PH (pulse duration of CLKIN high) for all outputs setup times; 0.5P is defined as PH (pulse duration of CLKIN high) for all output setup times; 0.5P is defined as PL (pulse duration of CLKIN low) for all output hold times.

11/ When the PLL is used (CLKMODE x4), P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns. For CLKMODE x1:

1.5P = P + PH, where P = 1/CPU clock frequency, and PH = pulse duration of CLKIN high.

0.5P = PL, where PL =is defined as PH pulse duration of CLKIN low.

12/ $\overline{HOLD}$ is synchronized internally. Therefore, if setup and hold times are not met, it will be either be recognized in the current cycle or in the next cycle. Thus, $\overline{HOLD}$ can be asynchronous input.

13/ All pending EMIF transactions are allowed to complete before $\overline{HOLDA}$ is asserted. The worst case for this is an asynchronous read or write with external ARDY used or a minimum of eight consecutive SDRAM reads or writes when RBTR8 =1. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.

14/ EMIF bus consists of $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, ED[31:0], EA[21:2], $\overline{ARE}$, $\overline{AOE}$, $\overline{AWE}$, $\overline{SSADS}$, $\overline{SSOE}$, $\overline{SSWE}$, SDA10, $\overline{SDRAS}$, $\overline{SDCAS}$, and $\overline{SDWE}$.

15/ This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x4 only when CLKIN and PLL are stable.

16/ This parameter applies to CLKMODE x4. The $\overline{RESET}$ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 µs to stabilize following device power up or after PLL configuration has been changed. During that time, $\overline{RESET}$ must be asserted to ensure proper device operation. See the clock PLL section for PLL lock times.

17/ CLKOUT1 cycles

18/ High group consists of: $\overline{HINT}$

Low group consist of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0 and TOUT1

Z group consist of: EA[21:2], ED[31:0], $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AOE}$, $\overline{SSADS}$, $\overline{SSOE}$, $\overline{SSWE}$, SDA10, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{XDWE}$, HD[15:0], CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, DX1, CLKR0, CLKR1, FSR0, FSR1.

19/ $\overline{HRDY}$ is gated by input $\overline{HCS}$.

If $\overline{HCS}$ = 0 at device reset, $\overline{HRDY}$ belongs to the high group.

If $\overline{HCS}$ = 1 at device reset, $\overline{HRDY}$ belongs to the low group.

20/ The interrupt signal are synchronized internally and are potentially recognized one cycle later if setup and hold times are violated. Thus, they can be connected to asynchronous inputs.

21/ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns. When the PLL is used (CLKMODE x4), 0.5P = 1/(2 x CPU clock frequency). For CLKMODE x1: 0.5P = PH, where PH is the high period of CLKIN.

22/ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [not($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

23/ The effects of internal clock jitter are included at test. There is no need to adjust timing numbers for internal clock jitter. P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

24/ Select signals include: HCNTRL[1:0], HR/$\overline{\text{W}}$, and HHWL.

25/ $\overline{\text{HCS}}$ enables $\overline{\text{HRDY}}$, and $\overline{\text{HRDY}}$ is always low when $\overline{\text{HCS}}$ is high. The case where $\overline{\text{HRDY}}$ goes high when $\overline{\text{HCS}}$ falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.

26/ This parameter is used during an HPID read. At the beginning of the first half word transfer on the falling edges of $\overline{\text{HSTROBE}}$, the HPI send the request to the DMA auxiliary channel, and $\overline{\text{HRDY}}$ remains high until DMA auxiliary channel loads the requested data into HPID.

27/ This parameter is used after second half-word of an HPID write or autoincrement read. $\overline{\text{HRDY}}$ remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the $\overline{\text{HRDY}}$ signal.

28/ CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signals are also inverted.

29/ The maximum bit rate for the C6202/02B/03 device is 100 Mbps or CPU/2 (the slower of the two). Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP to McBSP communications is 100 MHz; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 10 ns (100 MHz), whichever value is larger. For example, when running parts at 200 MHz (P = 5 ns), use 10 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 100 MHz (P = 10 ns), use 2P = 20 ns (50 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP to McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

30/ The minimum CLKR/X pulse duration is either (P-1) or 4 ns, whichever is larger. For example, when running parts at 200 MHz (P= 5 ns), use 5 ns as the minimum CLKR/X pulse duration. When running parts at 100 MHz (P = 10 ns), use (P-1) = 9 ns as the minimum CLKR/X pulse duration.

31/ Minimum delay times also represent minimum output hold times.

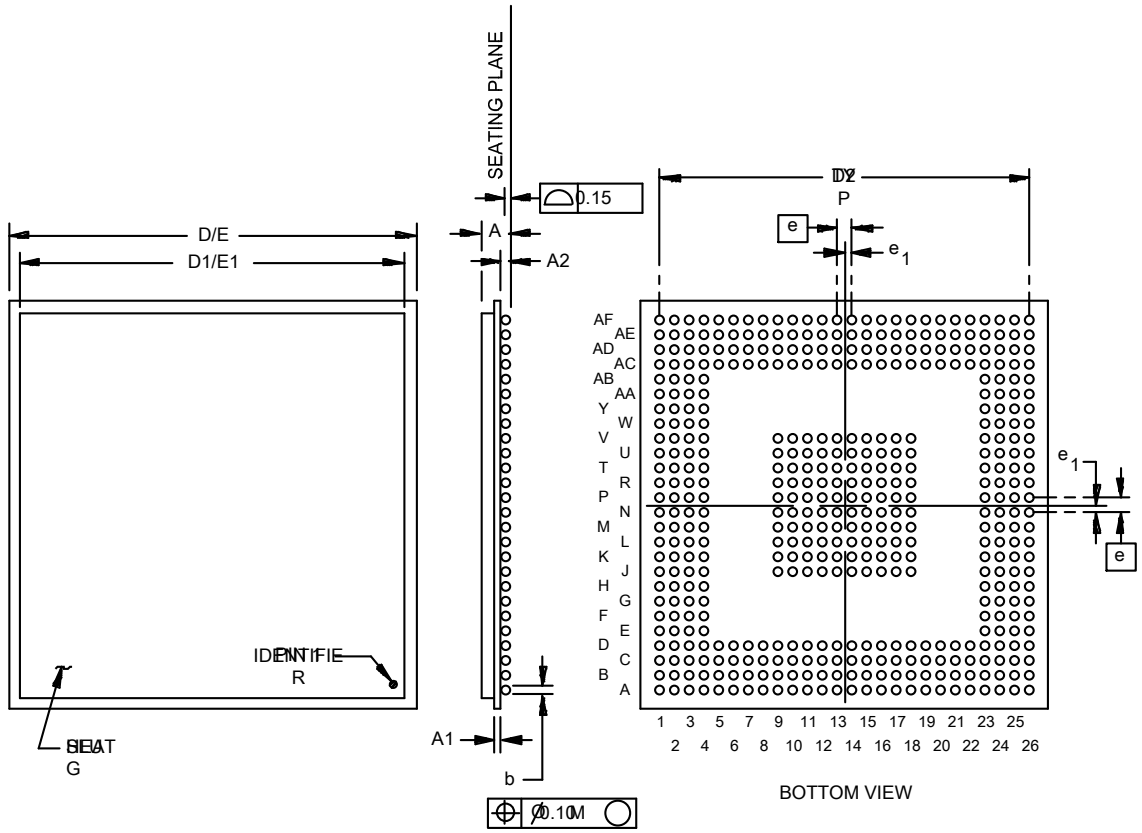
32/ C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1)*S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2)*S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero.

33/ For all SPI slave modes, CLKG is programmed as ½ of the CPU clock by setting CLKSM = CLKGDV = 1.

34/ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

35/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

Case X




| Dimensions | | | | | |
|---|---|---|---|---|---|
| Symbol | Millimeters | | Symbol | Millimeters | |
| | Min | Max | | Min | Max |
| A | | 3.50 | D1/E1 | 32.80 | 33.20 |
| A1 | 1.00 TYP | | D2/E2 | 21.00 NOM | |
| A2 | 0.50 | | D2 | 31.75 TYP | |
| b | 0.60 | 0.90 | e | 1.27 TYP | |
| D/E | 34.80 | 35.20 | e1 | 0.63 TYP | |

Notes:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Thermally enhanced plastic package with heat slug (HSL)
4. Flip chip application only.
5. Possible protrusion in this area, but within 3.50 max package height specification
6. Falls within JEDEC MO-151/BAR-2

FIGURE 1. Case outline.

| PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME |
|---|---|---|---|---|---|---|---|
| A1 | $V_{SS}$ | B1 | $V_{SS}$ | C1 | $DV_{DD}$ | D1 | DMAC1 |
| A2 | $V_{SS}$ | B2 | $CV_{DD}$ | C2 | $V_{SS}$ | D2 | DMAC3 |
| A3 | BOOTMODE2 | B3 | $V_{SS}$ | C3 | $CV_{DD}$ | D3 | PD |
| A4 | $V_{SS}$ | B4 | BOOTMODE3 | C4 | BOOTMODE0 | D4 | $CV_{DD}$ |
| A5 | $CV_{DD}$ | B5 | $V_{SS}$ | C5 | CLKMODE0 | D5 | BOOTMODE1 |
| A6 | RSV4 | B6 | $CV_{DD}$ | C6 | CLKMODE1 | D6 | $CV_{DD}$ |
| A7 | $\overline{HOLDA}$ | B7 | $DV_{DD}$ | C7 | $V_{SS}$ | D7 | $CV_{DD}$ |
| A8 | NC | B8 | NC | C8 | RSV5 | D8 | BOOTMODE4 |
| A9 | PLLFREQ3 | B9 | RSV3 | C9 | NC | D9 | $CV_{DD}$ |
| A10 | $DV_{DD}$ | B10 | PLLFREQ1 | C10 | CLKIN | D10 | NC |
| A11 | PLLF | B11 | $CV_{DD}$ | C11 | RSV2 | D11 | PLLFREQ2 |
| A12 | $CV_{DD}$ | B12 | $CV_{DD}$ | C12 | PLLG 1/ | D12 | PLLV 1/ |
| A13 | $V_{SS}$ | B13 | HD15 | C13 | $V_{SS}$ | D13 | $V_{SS}$ |
| A14 | $V_{SS}$ | B14 | HD14 | C14 | HD13 | D14 | $CV_{DD}$ |
| A15 | $DV_{DD}$ | B15 | HD12 | C15 | $CV_{DD}$ | D15 | HD11 |
| A16 | $CV_{DD}$ | B16 | HD10 | C16 | $V_{SS}$ | D16 | HD7 |
| A17 | HD9 | B17 | HD8 | C17 | $V_{SS}$ | D17 | $DV_{DD}$ |
| A18 | $DV_{DD}$ | B18 | HD6 | C18 | HD4 | D18 | $CV_{DD}$ |
| A19 | HD5 | B19 | HD3 | C19 | HD2 | D19 | $V_{SS}$ |
| A20 | $CV_{DD}$ | B20 | HD1 | C20 | $CV_{DD}$ | D20 | $CV_{DD}$ |
| A21 | $DV_{DD}$ | B21 | HD0 | C21 | RSV6 | D21 | NC |
| A22 | $DV_{DD}$ | B22 | RSV7 | C22 | $\overline{HAS}$ | D22 | $\overline{HDS1}$ |
| A23 | RSV8 | B23 | $\overline{HCS}$ | C23 | HR/ $\overline{W}$ | D23 | $CV_{DD}$ |
| A24 | $\overline{HDS2}$ | B24 | $V_{SS}$ | C24 | $CV_{DD}$ | D24 | $\overline{HBE0}$ |
| A25 | $V_{SS}$ | B25 | $CV_{DD}$ | C25 | $V_{SS}$ | D25 | HCNTL0 |
| A26 | $V_{SS}$ | B26 | $V_{SS}$ | C26 | HHWIL | D26 | DR1 |

1/ PLLV and PLLG are not part of external voltage supply or ground. See the Clock PLL section for information on how to connect these pins. $\overline{XWE}$ / $\overline{XWAIT}$ $\overline{XAS}$

FIGURE 2. Terminal connections.

| PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| E1 | $CV_{DD}$ | H1 | NC | L1 | CLKX0 | P1 | $V_{SS}$ | U1 | $CV_{DD}$ | Y1 | EMU1 |
| E2 | DMAC0 | H2 | NC | L2 | NMI | P2 | $CV_{DD}$ | U2 | $V_{SS}$ | Y2 | IACK |
| E3 | $V_{SS}$ | H3 | LENDIAN | L3 | TMS | P3 | FSX0 | U3 | EXT_INT7 | Y3 | $V_{SS}$ |
| E4 | RSV9 | H4 | $CV_{DD}$ | L4 | CLKS0 | P4 | FSR0 | U4 | EXT_INT4 | Y4 | $DV_{DD}$ |
| E23 | $\overline{HBE1}$ | H23 | CLKR1 | L23 | $V_{SS}$ | P23 | $CV_{DD}$ | U23 | $V_{SS}$ | Y23 | $\overline{BE1}$ |
| E24 | $V_{SS}$ | H24 | TOUT1 | L24 | EA19 | P24 | EA14 | U24 | $DV_{DD}$ | Y24 | $\overline{ARE}$ |
| E25 | CLKS1 | H25 | $DV_{DD}$ | L25 | $DV_{DD}$ | P25 | EA15 | U25 | EA9 | Y25 | $V_{SS}$ |
| E26 | FSR1 | H26 | $\overline{HINT}$ | L26 | $V_{SS}$ | P26 | $V_{SS}$ | U26 | EA10 | Y26 | EA2 |
| F1 | $CV_{DD}$ | J1 | DR0 | M1 | $CV_{DD}$ | R1 | DX0 | V1 | $V_{SS}$ | AA1 | INUM3 |
| F2 | $V_{SS}$ | J2 | NC | M2 | CLKR0 | R2 | NC | V2 | EXT_INT6 | AA2 | INUM1 |
| F3 | $DV_{DD}$ | J3 | $V_{SS}$ | M3 | $DV_{DD}$ | R3 | TCK | V3 | $V_{SS}$ | AA3 | $V_{SS}$ |
| F4 | DMAC2 | J4 | $CV_{DD}$ | M4 | TOUT0 | R4 | TDI | V4 | $CV_{DD}$ | AA4 | ED29 |
| F23 | FSX1 | J23 | $CV_{DD}$ | M23 | $V_{SS}$ | R23 | EA11 | V23 | $CV_{DD}$ | AA23 | $V_{SS}$ |
| F24 | $V_{SS}$ | J24 | $\overline{HRDY}$ | M24 | $CV_{DD}$ | R24 | $V_{SS}$ | V24 | EA4 | AA24 | $\overline{BE2}$ |
| F25 | FSX1 | J25 | $DV_{DD}$ | M25 | EA16 | R25 | EA13 | V25 | EA6 | AA25 | $\overline{HOLD}$ |
| F26 | CLKX1 | J26 | EA21 | M26 | EA17 | R26 | $DV_{DD}$ | V26 | EA7 | AA26 | $\overline{BE0}$ |
| G1 | NC | K1 | $CV_{DD}$ | N1 | $V_{SS}$ | T1 | $\overline{TRST}$ | W1 | EXT_INT5 | AB1 | INUM0 |
| G2 | RSV1 | K2 | $\overline{RESET}$ | N2 | $V_{SS}$ | T2 | RSV0 | W2 | TDO | AB2 | ED31 |
| G3 | $V_{SS}$ | K3 | NC | N3 | $DV_{DD}$ | T3 | $CV_{DD}$ | W3 | EMU0 | AB3 | $DV_{DD}$ |
| G4 | $V_{SS}$ | K4 | TINP0 | N4 | $CV_{DD}$ | T4 | $CV_{DD}$ | W4 | INUM2 | AB4 | $DV_{DD}$ |
| G23 | DX1 | K23 | $CV_{DD}$ | N23 | $DV_{DD}$ | T23 | EA8 | W23 | ARDY | AB23 | $V_{SS}$ |
| G24 | $DV_{DD}$ | K24 | TINP1 | N24 | $V_{SS}$ | T24 | $DV_{DD}$ | W24 | $DV_{DD}$ | AB24 | $\overline{CE1}$ |
| G25 | $DV_{DD}$ | K25 | EA20 | N25 | $CV_{DD}$ | T25 | $V_{SS}$ | W25 | EA3 | AB25 | $\overline{BE3}$ |
| G26 | $V_{SS}$ | K26 | EA18 | N26 | $V_{SS}$ | T26 | EA12 | W26 | EA5 | AB26 | $DV_{DD}$ |

FIGURE 2. Terminal connections - Continued.

| PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME | PIN No. | PIN NAME |
|---|---|---|---|---|---|---|---|
| AC1 | ED30 | AD1 | ED28 | AE1 | $V_{SS}$ | AF1 | $V_{SS}$ |
| AC2 | $V_{SS}$ | AD2 | $V_{SS}$ | AE2 | $CV_{DD}$ | AF2 | $V_{SS}$ |
| AC3 | ED27 | AD3 | $CV_{DD}$ | AE3 | $V_{SS}$ | AF3 | ED25 |
| AC4 | $CV_{DD}$ | AD4 | ED26 | AE4 | ED24 | AF4 | ED22 |
| AC5 | $V_{SS}$ | AD5 | ED23 | AE5 | ED21 | AF5 | $DV_{DD}$ |
| AC6 | $DV_{DD}$ | AD6 | ED20 | AE6 | ED19 | AF6 | $DV_{DD}$ |
| AC7 | $V_{SS}$ | AD7 | ED18 | AE7 | $V_{SS}$ | AF7 | ED16 |
| AC8 | ED17 | AD8 | $CV_{DD}$ | AE8 | $CV_{DD}$ | AF8 | $V_{SS}$ |
| AC9 | $CV_{DD}$ | AD9 | ED15 | AE9 | $V_{SS}$ | AF9 | ED13 |
| AC10 | $DV_{DD}$ | AD10 | ED14 | AE10 | ED11 | AF10 | $V_{SS}$ |
| AC11 | ED12 | AD11 | $DV_{DD}$ | AE11 | ED10 | AF11 | ED9 |
| AC12 | $CV_{DD}$ | AD12 | $V_{SS}$ | AE12 | $CV_{DD}$ | AF12 | $CV_{DD}$ |
| AC13 | $CV_{DD}$ | AD13 | $DV_{DD}$ | AE13 | $V_{SS}$ | AF13 | $V_{SS}$ |
| AC14 | $V_{SS}$ | AD14 | $CV_{DD}$ | AE14 | ED8 | AF14 | $V_{SS}$ |
| AC15 | ED4 | AD15 | $DV_{DD}$ | AE15 | ED6 | AF15 | ED7 |
| AC16 | $V_{SS}$ | AD16 | $V_{SS}$ | AE16 | $V_{SS}$ | AF16 | ED5 |
| AC17 | ED0 | AD17 | SSCLK | AE17 | ED3 | AF17 | $DV_{DD}$ |
| AC18 | $CV_{DD}$ | AD18 | $DV_{DD}$ | AE18 | $DV_{DD}$ | AF18 | ED2 |
| AC19 | $DV_{DD}$ | AD19 | $\overline{SSWE}$ | AE19 | $V_{SS}$ | AF19 | ED1 |
| AC20 | $\overline{SSADS}$ | AD20 | $V_{SS}$ | AE20 | SDCLK | AF20 | CLKOUT2 |
| AC21 | $DV_{DD}$ | AD21 | SDA10 | AE21 | $DV_{DD}$ | AF21 | $\overline{SSOE}$ |
| AC22 | $DV_{DD}$ | AD22 | $\overline{SDCAS}$ | AE22 | $\overline{CE3}$ | AF22 | CLKOUT1 |
| AC23 | $CV_{DD}$ | AD23 | $\overline{AWE}$ | AE23 | $V_{SS}$ | AF23 | $\overline{SDWE}$ |
| AC24 | $\overline{AOE}$ | AD24 | $CV_{DD}$ | AE24 | $V_{SS}$ | AF24 | $\overline{SDRAS}$ |
| AC25 | $DV_{DD}$ | AD25 | $V_{SS}$ | AE25 | $CV_{DD}$ | AF25 | $V_{SS}$ |
| AC26 | $\overline{CE0}$ | AD26 | $\overline{CE2}$ | AE26 | $V_{SS}$ | AF26 | $V_{SS}$ |

FIGURE 2. Terminal connections - Continued.

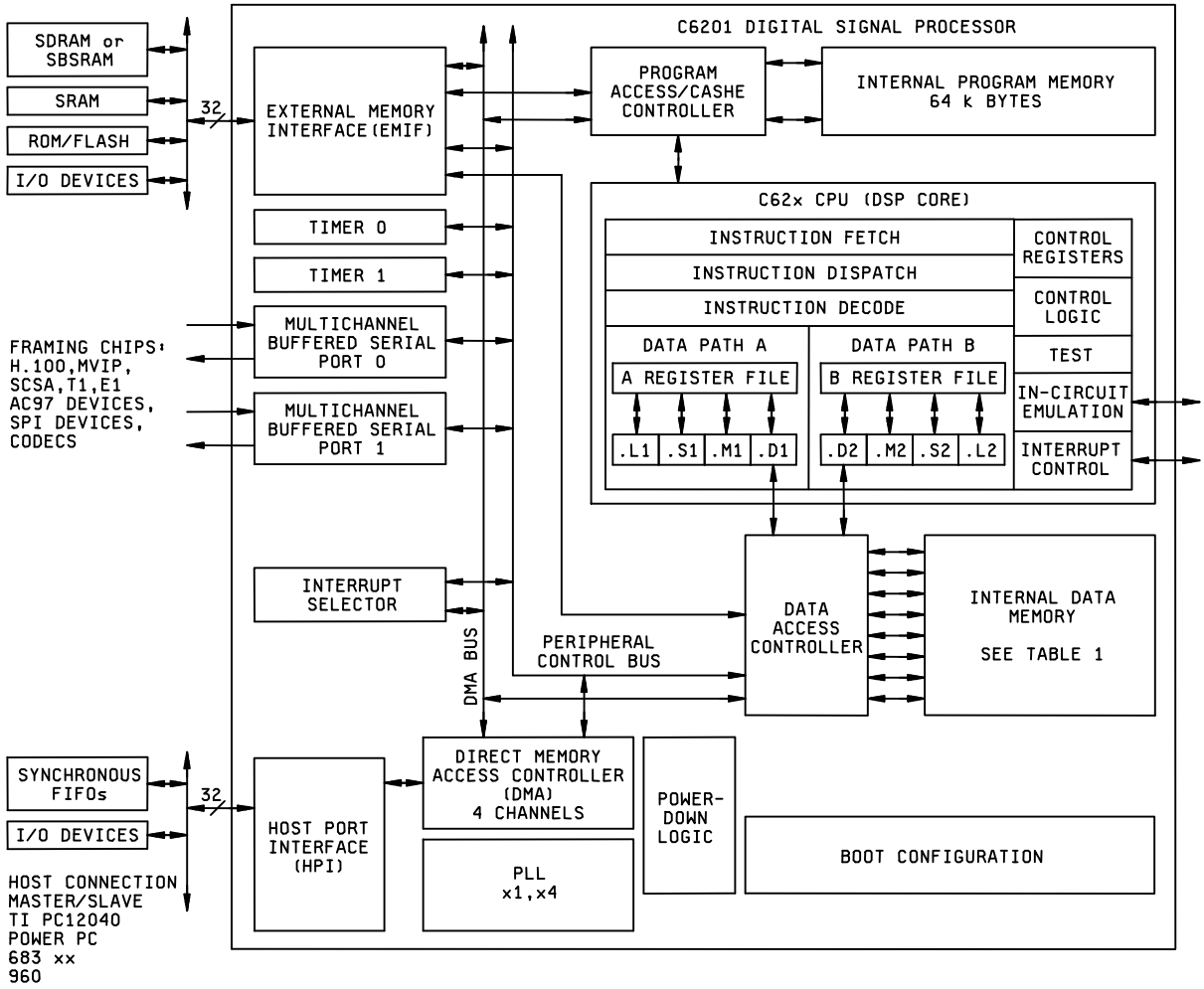
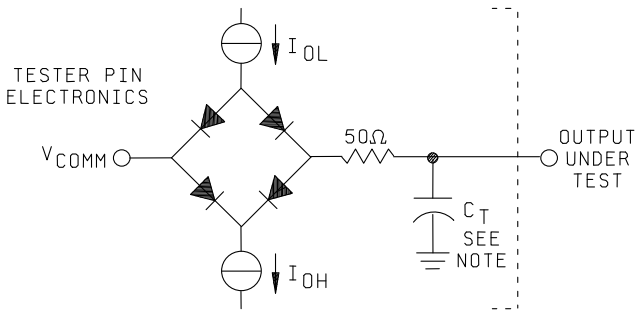
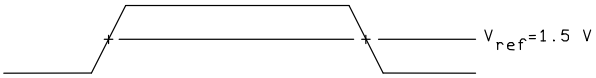



FIGURE 3. Block diagram.



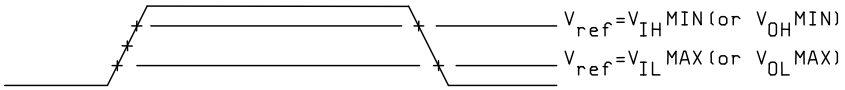

Where: $I_{OL}$ = 2 mA
$I_{OH}$ = 2 mA
$V_{COMM}$ = 0.8 V
CT = 15-30 pF typical load circuit capacitance.

FIGURE 4. Test circuit.



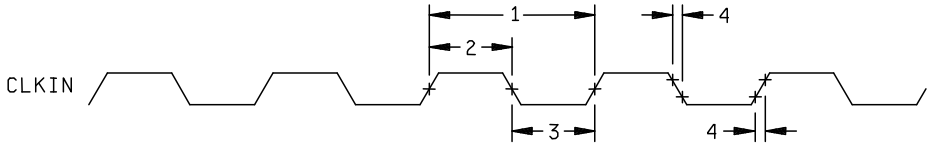

INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS

FIGURE 5. Timing waveforms.




RISE AND FALL TRANSITION TIME VOLTAGE REFERENCE LEVELS

FIGURE 6. Timing waveforms - Continued.




CLKIN TIMINGS

FIGURE 7. Timing waveforms - Continued.

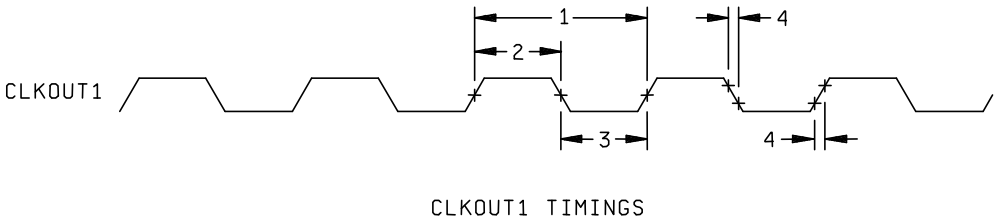



FIGURE 8. Timing waveforms - Continued.

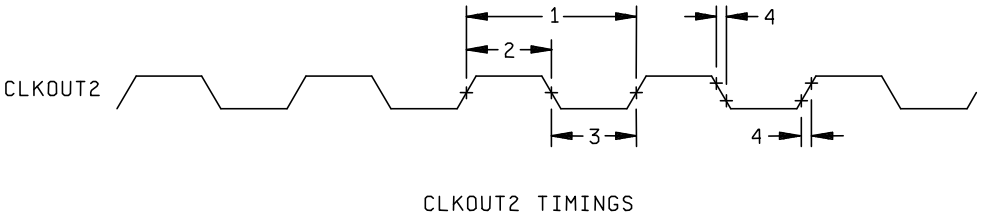



FIGURE 9. Timing waveforms - Continued.

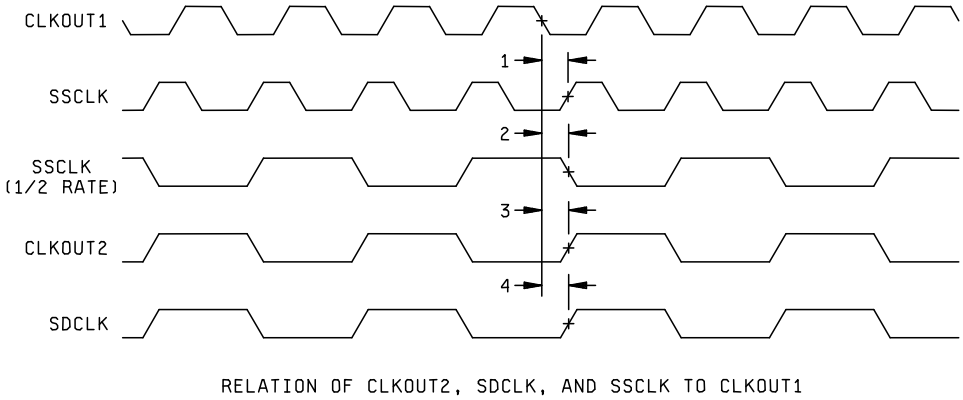
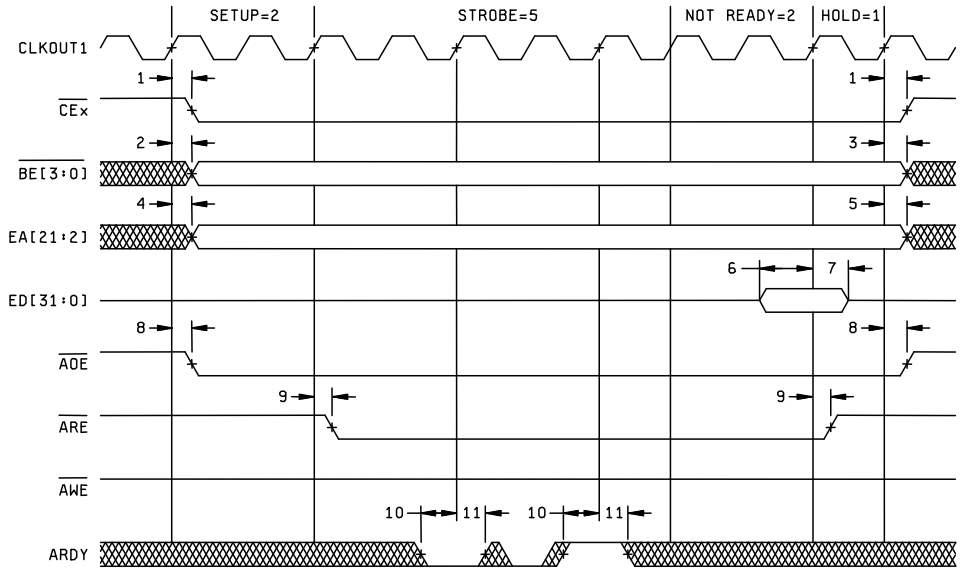
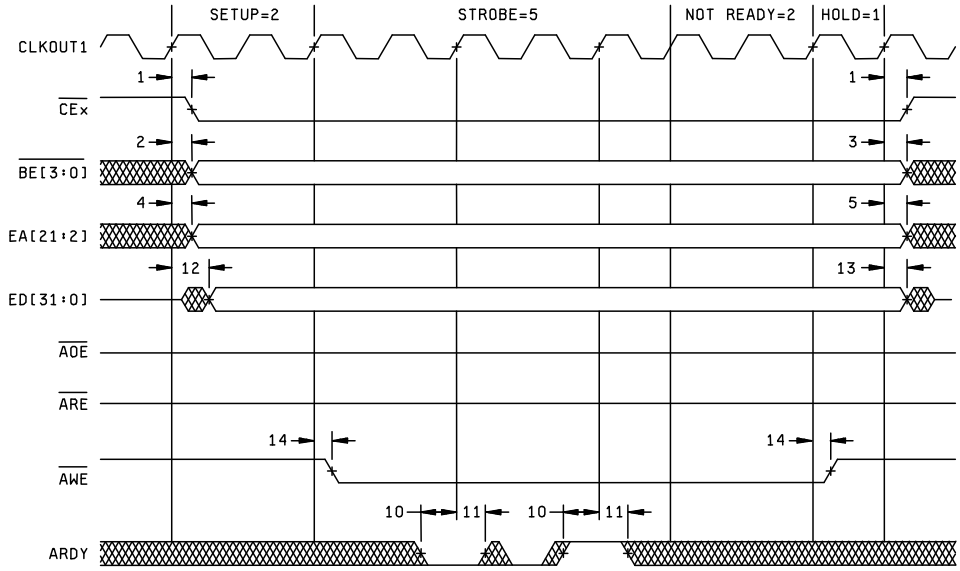



FIGURE 10. Timing waveforms - Continued.

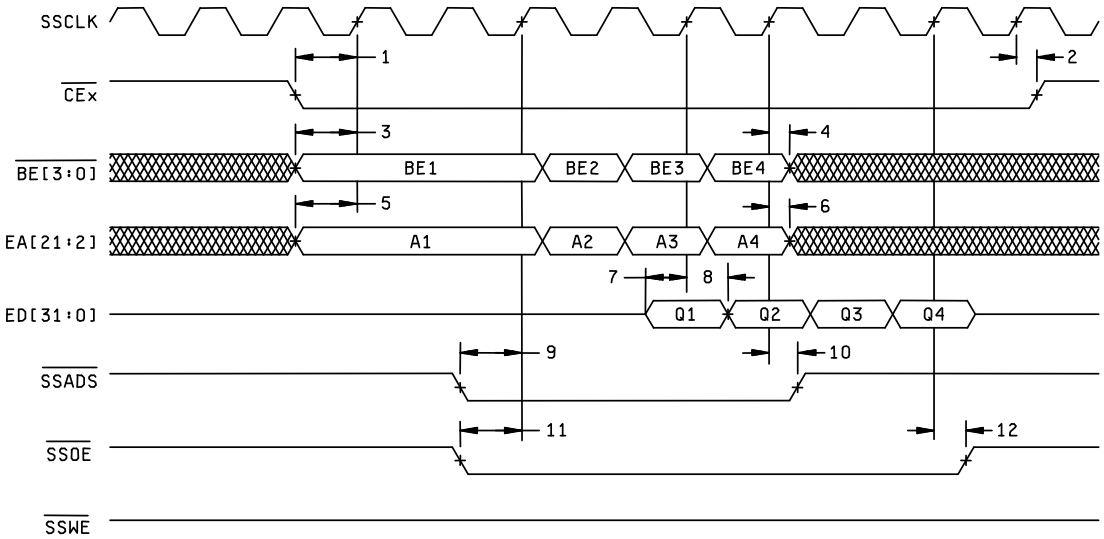



ASYNCHRONOUS MEMORY READ TIMING

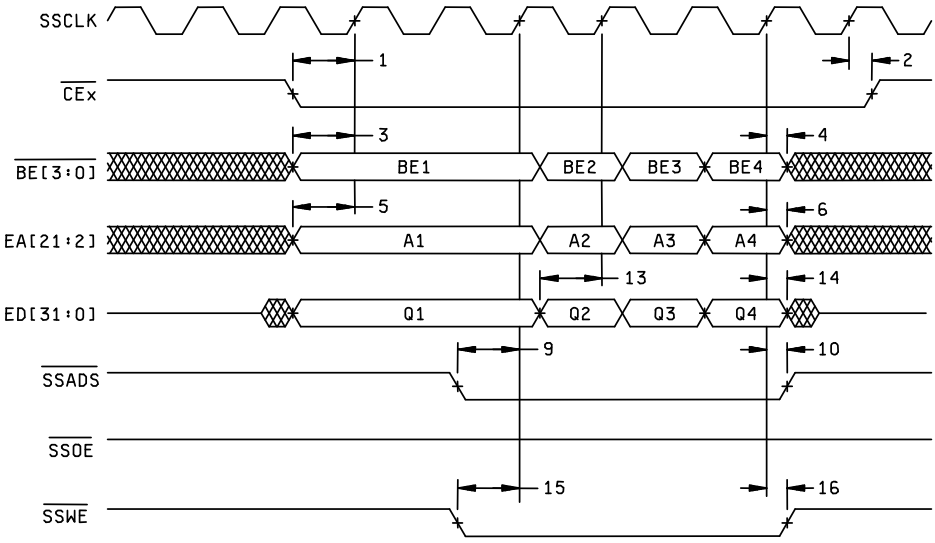



ASYNCHRONOUS MEMORY WRITE TIMING

FIGURE 11. Timing waveforms - Continued.

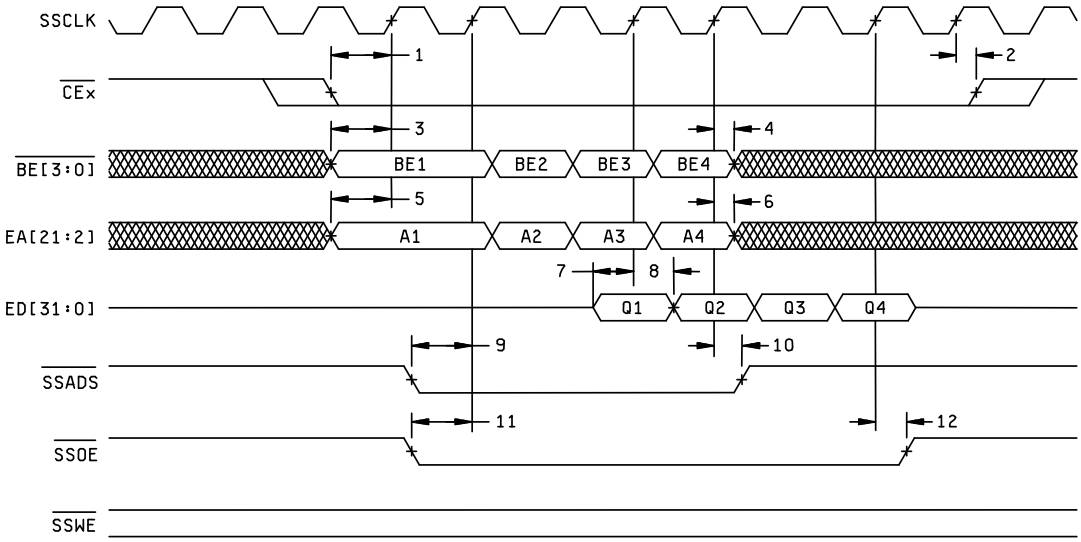



SBSRAM READ TIMING (FULL-RATE SSCLK)

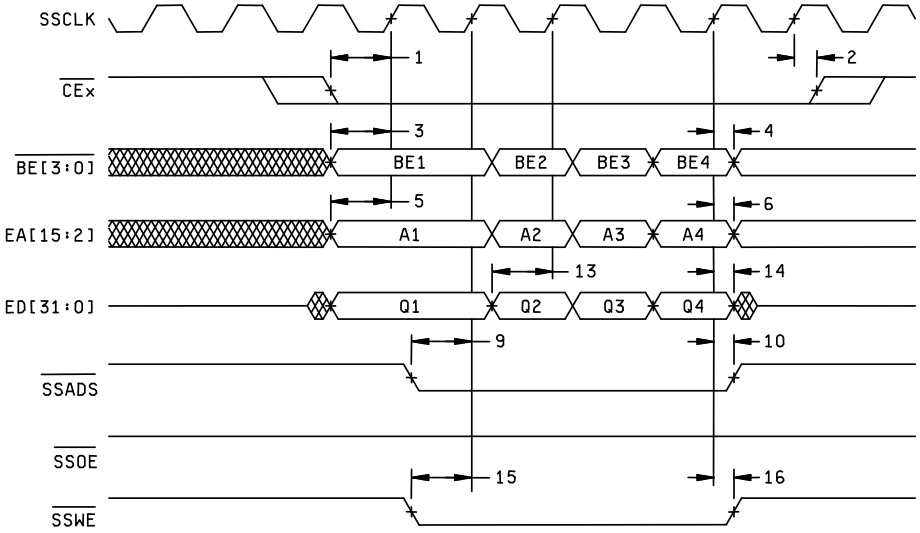



SBSRAM WRITE TIMING (FULL-RATE SSCLK)

FIGURE 12. Timing waveforms - Continued.

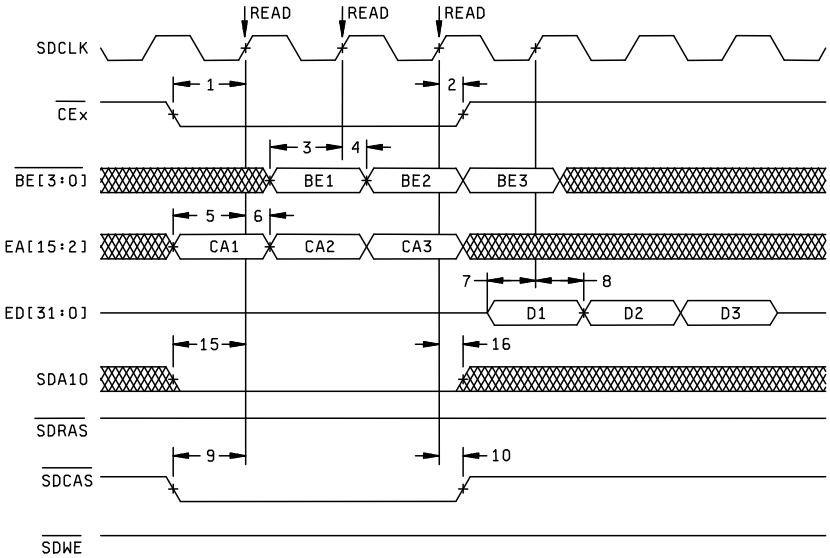



SBSRAM READ TIMING (1/2 RATE SSCLK)

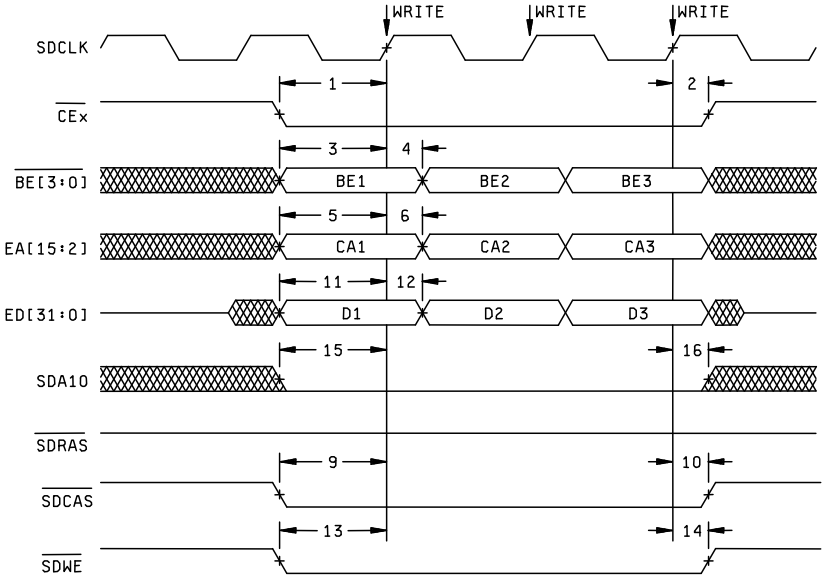



SBSRAM WRITE TIMING (1/2 RATE SSCLK)

FIGURE 13. Timing waveforms - Continued.

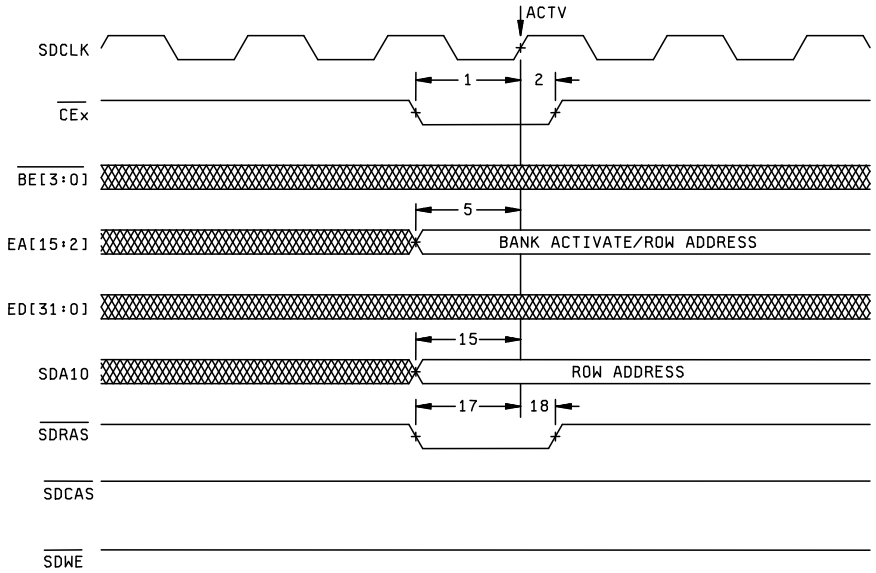



THREE SDRAM READ COMMANDS

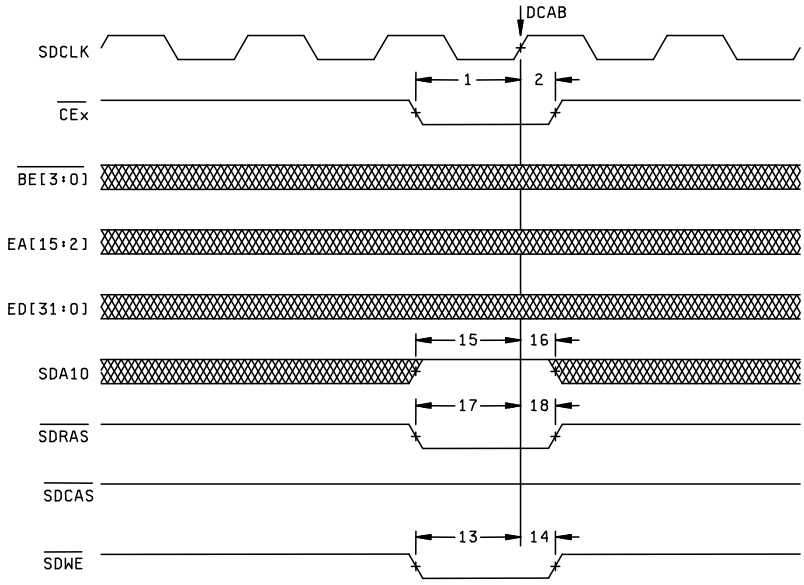



THREE SDRAM WRT COMMANDS

FIGURE 14. Timing waveforms - Continued.

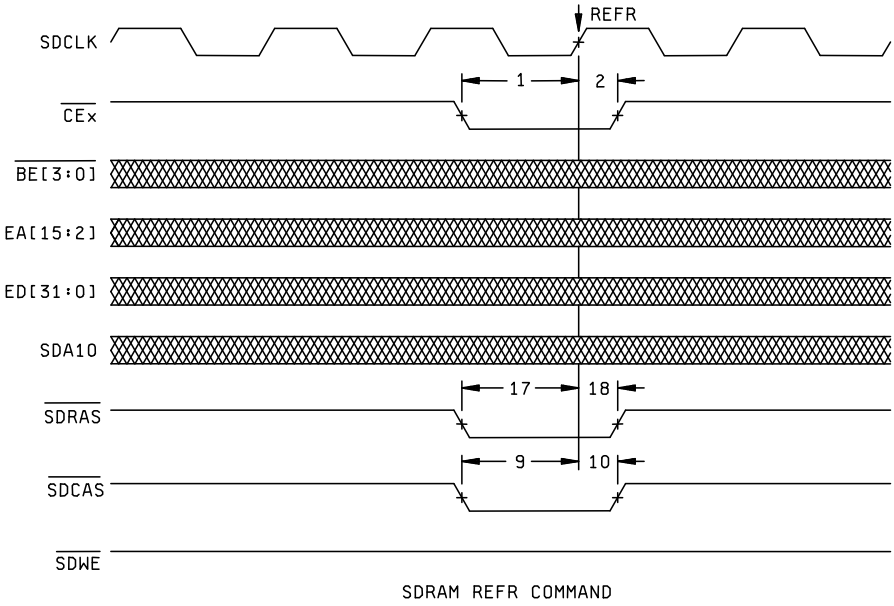



SDRAM ACTV COMMAND

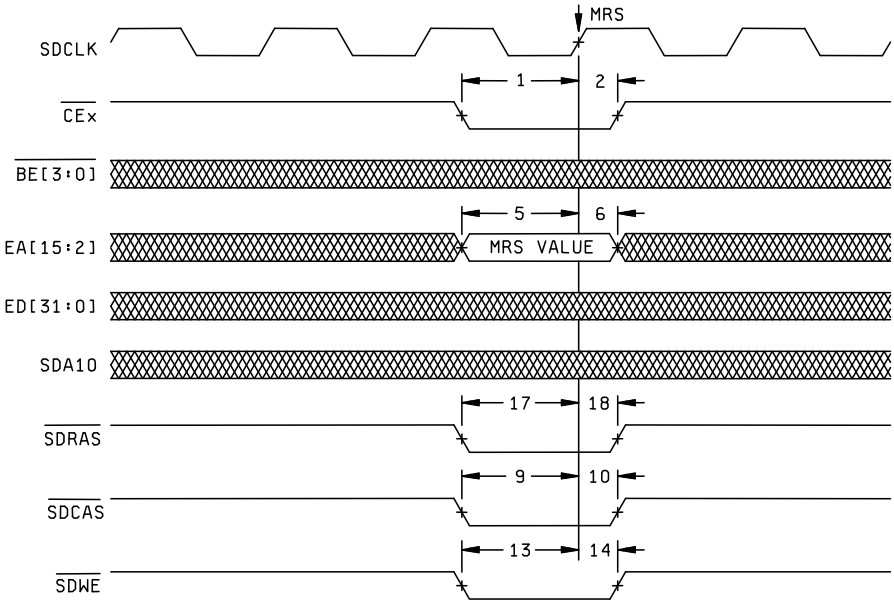



SDRAM DCAB COMMAND

FIGURE 15. Timing waveforms - Continued.

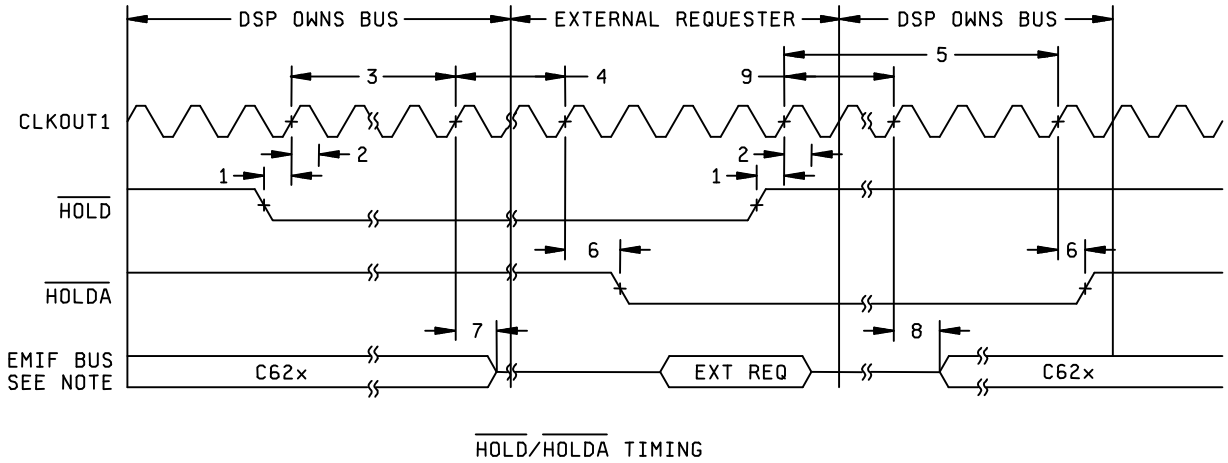



SDRAM REFR COMMAND




SDRAM MRS COMMAND

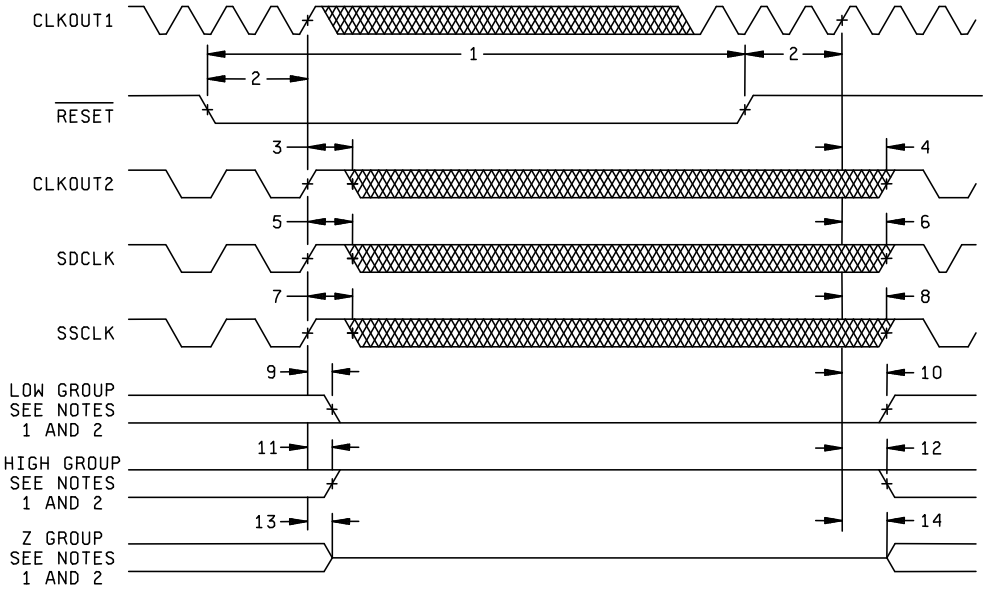
FIGURE 16. Timing waveforms - Continued.




Note:

1. EMIF bus consists of $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, ED[31:0], EA[21:2], $\overline{ARE}$, $\overline{AOE}$, $\overline{AWE}$, $\overline{SSADS}$, $\overline{SSOE}$, $\overline{SSWE}$, SDA10, $\overline{SDRAS}$, $\overline{SDCAS}$, and $\overline{SDWE}$

FIGURE 17. Timing waveforms - Continued.




RESET TIMING

Notes:

1. Low group consist of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0 and TOUT1.

   High group consists of: $\overline{\text{HINT}}$

   Z group consist of: EA[21:2], ED[31:0], $\overline{\text{CE[3:0]}}$, $\overline{\text{BE[3:0]}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AOE}}$, $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, $\overline{\text{SSWE}}$, SDA10, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{XDWE}}$, HD[15:0], CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, DX1, CLKR0, CLKR1, FSR0, FSR1.

2. $\overline{\text{HRDY}}$ IS GATED BY INPUT $\overline{\text{HCS}}$.

   If $\overline{\text{HCS}}$ = 0 at device reset, $\overline{\text{HRDY}}$ belongs to the high group.

   If $\overline{\text{HCS}}$ = 1 at device reset, $\overline{\text{HRDY}}$ belongs to the low group.

FIGURE 18. Timing waveforms - Continued.

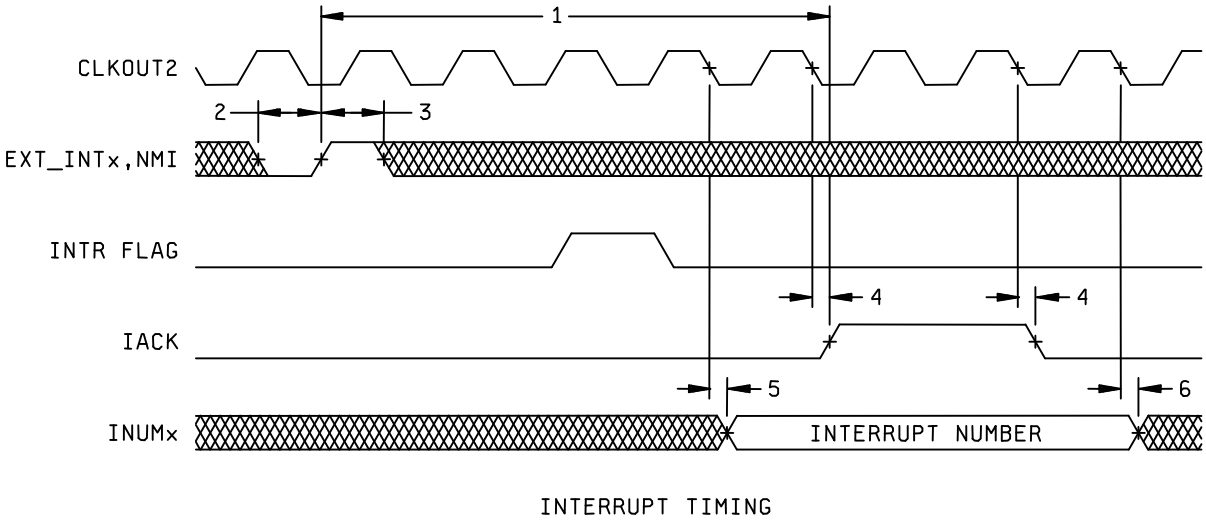
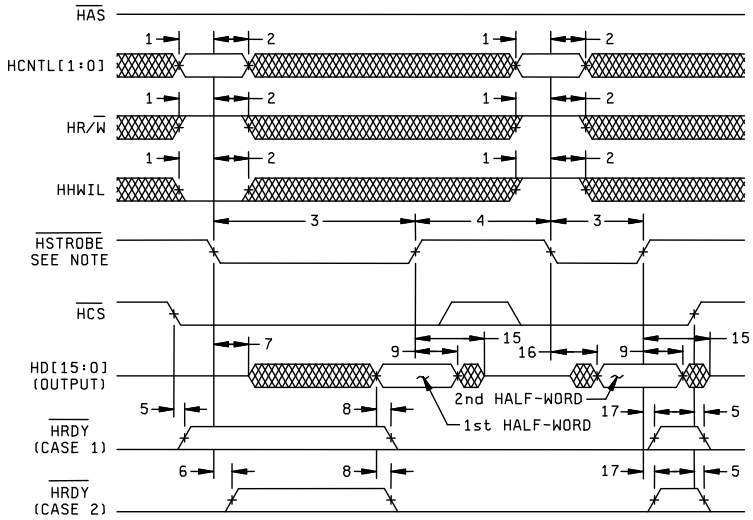
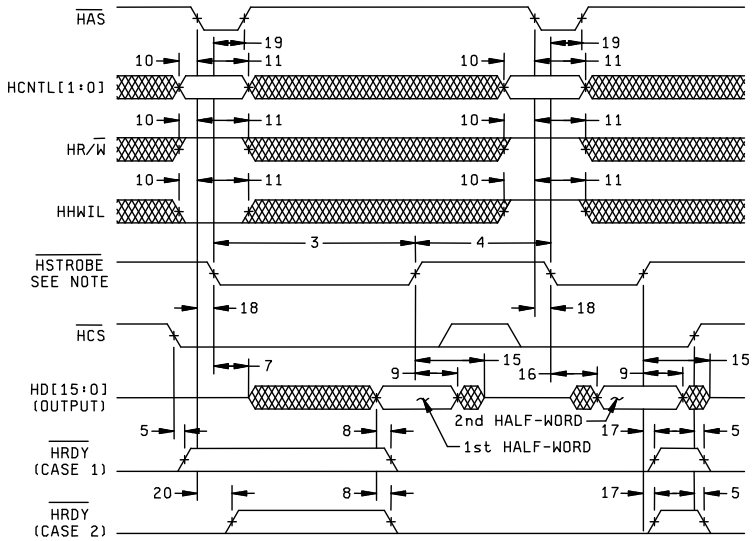



FIGURE 19. Timing waveforms - Continued.




HPI READ TIMING (HAS NOT USED,TIED HIGH)

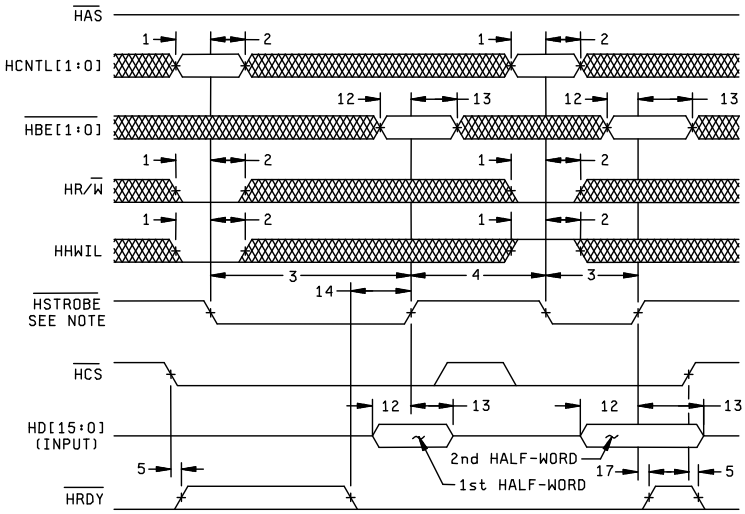



HPI READ TIMING (HAS USED)

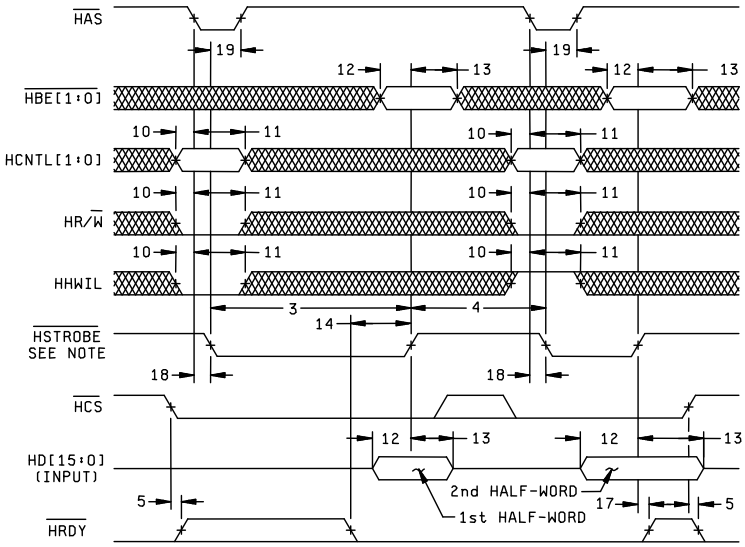
Note:

1. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [not($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

FIGURE 20. Timing waveforms - Continued.




HPI WRITE TIMING (HAS NOT USED,TIED HIGH)




HPI WRITE TIMING (HAS USED)

Note:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [not(HDS1 XOR HDS2)] OR HCS.

FIGURE 21. Timing waveforms - Continued.

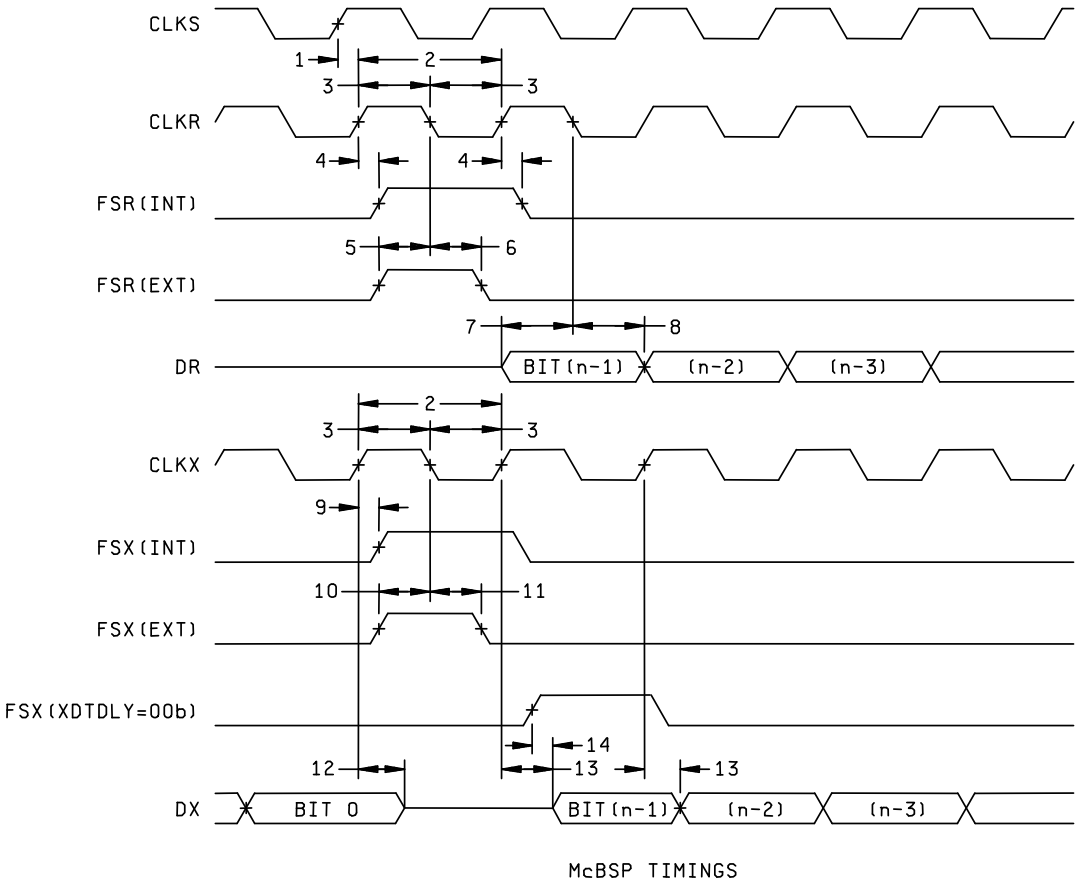



FIGURE 22. Timing waveforms - Continued.

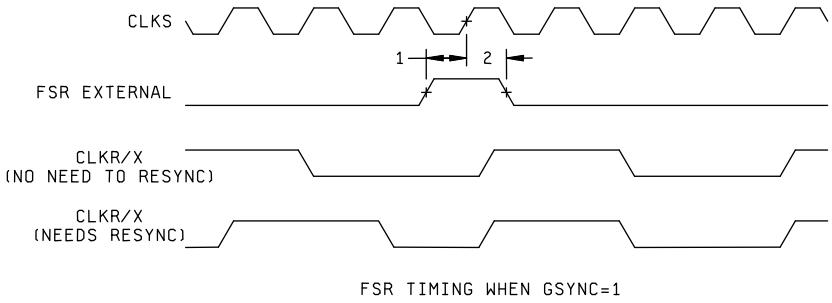



FIGURE 23. Timing waveforms - Continued.

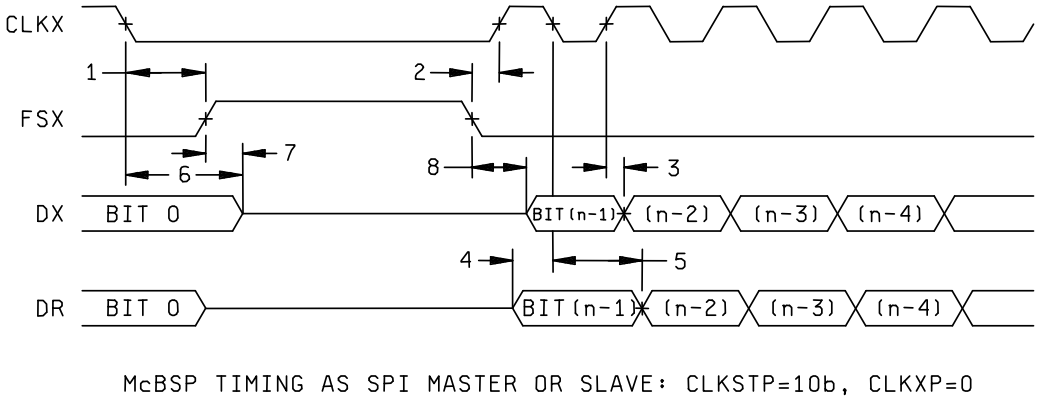



FIGURE 24. Timing waveforms - Continued.

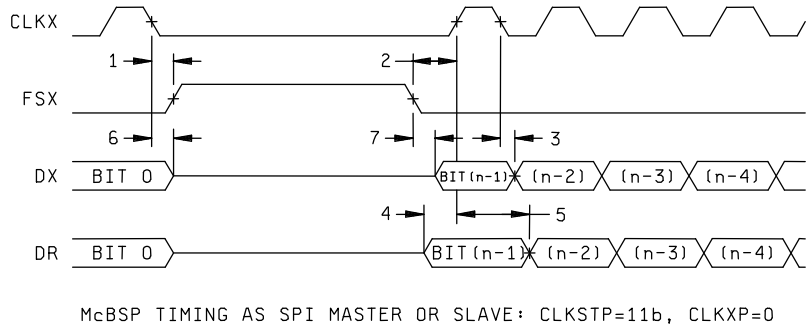



FIGURE 25. Timing waveforms - Continued.

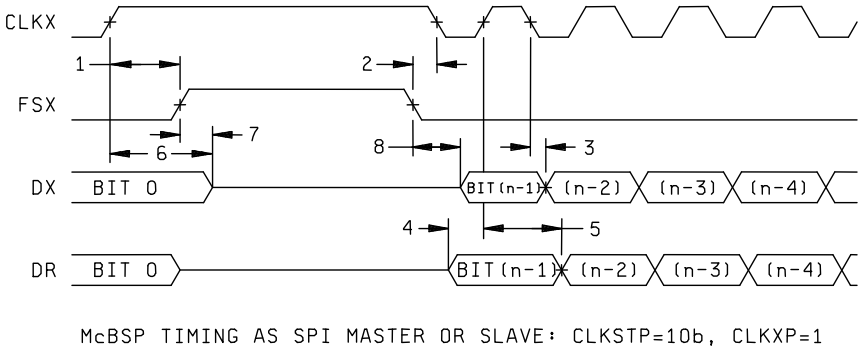



FIGURE 26. Timing waveforms - Continued.

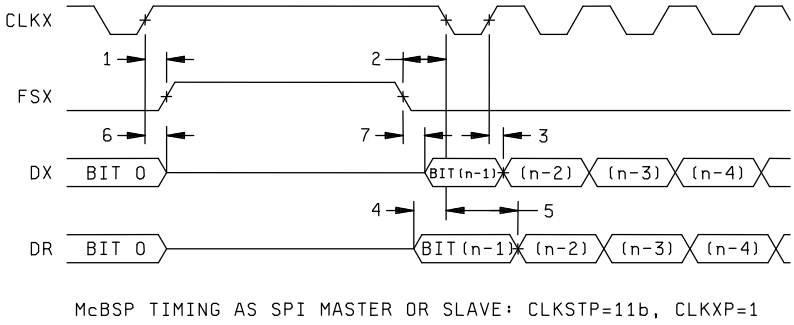



FIGURE 27. Timing waveforms - Continued.

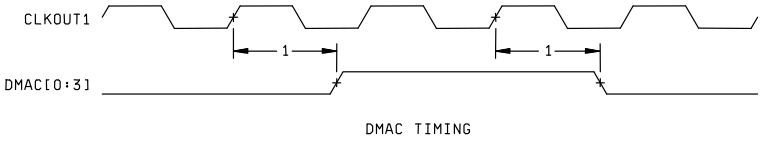



FIGURE 28. Timing waveforms - Continued.

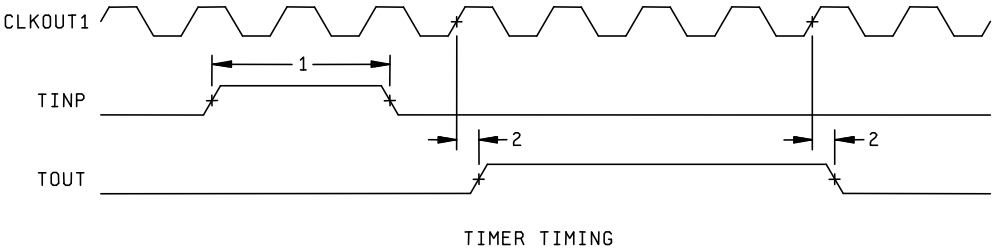



FIGURE 29. Timing waveforms - Continued.

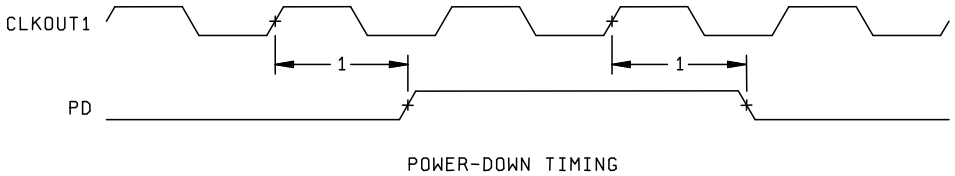



FIGURE 30. Timing waveforms - Continued.

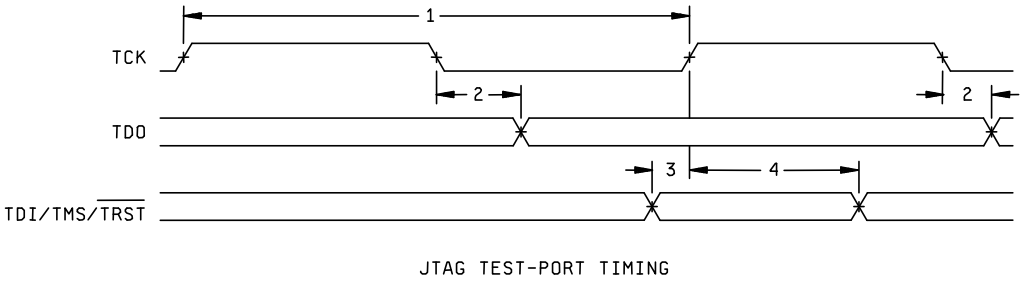



FIGURE 31. Timing waveforms - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Vendor part number |
|---|---|---|
| V62/04606-01XA | 01295 | SM320C6201GJCA20EP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243<br>Point of contact: U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |