REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02. - ro	04-07-08	R. MONNIN
B	Make changes to Electrostatic discharge section as specified under 1.3. - ro	05-03-04	R. MONNIN
C	JEDEC package MS-012 has been updated to MS-012-AA along with dimensions b, c, and L. Add notes to Figure 1. Update document paragraphs to current requirements. - ro	19-04-10	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	C	C																			
PAGE	18	19																			

REV STATUS OF PAGES	**REV**	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 03-08-21	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, DIFFERENTIAL BUS TRANSCEIVER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03671**
	REV **C**	**PAGE** 1 **OF** 19

AMSC N/A

5962-V032-19

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance differential bus transceiver microcircuit, with an operating temperature range of -40°C to +125°C for device type 01 and -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03671	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65LBC176AQ-EP	Differential bus transceiver
02	SN65LBC176AM-EP	Differential bus transceiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.3 V to 6 V 2/
Voltage range at any bus terminal (A or B) ..... -10 V to 15 V
Input voltage, (V_I) (D, DE, R, or $\overline{RE}$) ..... -0.3 V to V_{CC} + 0.5 V
Electrostatic discharge:
A, B bus terminals and GND ..... 400 V 3/
All A, B terminals ..... 400 V 3/
Continuous total power dissipation (P_D) ..... See dissipation rating table 4/
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... 4.75 V to 5.25 V
Voltage at any bus terminal (separately or common mode), (V_I or V_{IC}) ..... -7 V minimum and 12 V maximum
High level input voltage (V_{IH}) (output recessive) (D, DE, and $\overline{RE}$) ..... 2 V to V_{CC}
Low level input voltage (V_{IL}) (output dominant) (D, DE, and $\overline{RE}$) ..... 0 V to 0.8 V
Differential input voltage (V_{ID}) ..... -12 V to 12 V 5/ 6/
High level output current (I_{OH}):
Driver ..... -60 mA minimum
Receiver ..... -8 mA minimum
Low level output current (I_{OL}):
Driver ..... 60 mA maximum
Receiver ..... 8 mA maximum
Operating free-air temperature range (T_A) :
Device type 01 ..... -40°C to +125°C
Device type 02 ..... -55°C to +125°C

Case outline	$T_A \leq 25°C$ Power rating	Derating factor 7/ Above $T_A = 25°C$	$T_A = 70°C$ Power rating	$T_A = 85°C$ Power rating	$T_A = 125°C$ Power rating
X	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
3/ Tested in accordance with MIL-STD-883, test method 3015 (human body model).
4/ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
5/ The algebraic convention, in which the least positive (most negative) limit is designed as minimum, is used in this data sheet.
6/ Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
7/ This is the inverse junction-to-ambient thermal resistance when the board is mounted and with no air flow.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Test circuits. The test circuits shall be as shown in figures 4 and 5.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 6, 7,and 8.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics section							
Input clamp voltage	V_{IK}	I_I = -18 mA	-40°C to +125°C	01	-1.5		V
			-55°C to +125°C	02	-1.5		
Differential output voltage	$\|V_{OD}\|$	I_O = 0	-40°C to +125°C	01	1.5	6	V
		R_L = 54 Ω, see figure 4			0.9	6	
		V_{test} = -7 V to 12 V, see figure 5			0.9	6	
		I_O = 0	-55°C to +125°C	02	1.5	6	
		R_L = 54 Ω, see figure 4			0.9	6	
		V_{test} = -7 V to 12 V, see figure 5			0.9	6	
Change in magnitude of differential output voltage	$\Delta\|V_{OD}\|$	See figure 4 and 5	-40°C to +125°C	01	-0.2	0.2	V
			-55°C to +125°C	02	-0.2	0.2	
Steady state common mode output voltage	$V_{OC(SS)}$	See figure 4	-40°C to +125°C	01	1.8	3	V
			-55°C to +125°C	02	1.8	3	
Change in steady state common mode output voltage	$\Delta V_{OC(SS)}$	See figure 4	+25°C	01	-0.2	0.2	V
				02	-0.2	0.2	
High impedance output current	I_{OZ}	See receiver input currents under paragraph 1.4	-40°C to +125°C	01			
			-55°C to +125°C	02			
High level enable input current	I_{IH}	V_I = 2 V	-40°C to +125°C	01	-100		µA
			-55°C to +125°C	02	-100		
Low level enable input current	I_{IL}	V_I = 0.8 V	-40°C to +125°C	01	-100		µA
			-55°C to +125°C	02	-100		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics section – continued.							
Short circuit output current	I_{OS}	-7 V ≤ V_O ≤ 12 V	-40°C to +125°C	01	-250	250	mA
			-55°C to +125°C	02	-250	250	
Supply current	I_{CC}	V_I = 0 or V_{CC}, no load, receiver disabled and driver enabled	-40°C to +125°C	01		9	mA
		V_I = 0 or V_{CC}, no load, receiver disabled and driver disabled				0.7	
		V_I = 0 or V_{CC}, no load, receiver enabled and driver enabled				15	
		V_I = 0 or V_{CC}, no load, receiver disabled and driver enabled	-55°C to +125°C	02		9	
		V_I = 0 or V_{CC}, no load, receiver disabled and driver disabled				0.7	
		V_I = 0 or V_{CC}, no load, receiver enabled and driver enabled				15	
Driver switching characteristics section							
Propagation delay time, low-to-high level output	t_{PLH}	R_L = 54 Ω, C_L = 50 pF, see figure 6	-40°C to +125°C	01	2	12	ns
			-55°C to +125°C	02	2	12	
Propagation delay time, high-to-low level output	t_{PHL}	R_L = 54 Ω, C_L = 50 pF, see figure 6	-40°C to +125°C	01	2	12	ns
			-55°C to +125°C	02	2	12	
Pulse skew (t_{PLH} – t_{PHL})	$t_{sk(p)}$	R_L = 54 Ω, C_L = 50 pF, see figure 6	-40°C to +125°C	01		2	ns
			-55°C to +125°C	02		2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics section – continued.							
Differential output signal rise time	t_r	R_L = 54 Ω, C_L = 50 pF, see figure 6	-40°C to +125°C	01	1.2	11	ns
			-55°C to +125°C	02	1.2	11	
Differential output signal fall time	t_f	R_L = 54 Ω, C_L = 50 pF, see figure 6	-40°C to +125°C	01	1.2	11	ns
			-55°C to +125°C	02	1.2	11	
Propagation delay time, high impedance to high level output	t_{PZH}	R_L = 110 Ω, see figure 6	-40°C to +125°C	01		22	ns
			-55°C to +125°C	02		22	
Propagation delay time, high impedance to low level output	t_{PZL}	R_L = 110 Ω, see figure 6	-40°C to +125°C	01		25	ns
			-55°C to +125°C	02		25	
Propagation delay time, high level to high impedance output	t_{PHZ}	R_L = 110 Ω, see figure 6	-40°C to +125°C	01		22	ns
			-55°C to +125°C	02		22	
Propagation delay time, low level to high impedance output	t_{PLZ}	R_L = 110 Ω, see figure 6	-40°C to +125°C	01		22	ns
			-55°C to +125°C	02		22	
Receiver electrical characteristics section							
Positive going input threshold voltage	V_{IT+}	I_O = -8 mA	-40°C to +125°C	01		0.2	V
			-55°C to +125°C	02		0.2	
Negative going input threshold voltage	V_{IT-}	I_O = 8 mA	-40°C to +125°C	01	-0.2		V
			-55°C to +125°C	02	-0.2		
Hysteresis voltage (V_{IT+} - V_{IT-})	V_{hys}	I_O = 8 mA, V_{CC} = 5 V	25°C	01	50 typical		mV
				02	50 typical		
Enable input clamp voltage	V_{IK}	I_I = -18 mA	-40°C to +125°C	01	-1.5		V
			-55°C to +125°C	02	-1.5		

See footnote at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics section - continued							
High level output voltage	V_{OH}	V_{ID} = 200 mV, I_{OH} = -8 mA, see figure 7	-40°C to +125°C	01	4		V
			-55°C to +125°C	02	4		
Low level output voltage	V_{OL}	V_{ID} = 200 mV, I_{OL} = 8 mA, see figure 7	-40°C to +125°C	01		0.8	V
			-55°C to +125°C	02		0.8	
High impedance state output current	I_{OZ}	V_O = 0 to V_{CC}	-40°C to +125°C	01	-10	10	µA
			-55°C to +125°C	02	-10	10	
Bus input current	I_I	V_{IH} = 12 V, V_{CC} = 5 V, other input at 0 V	-40°C to +125°C	01		1	mA
		V_{IH} = 12 V, V_{CC} = 0 V, other input at 0 V				1	
		V_{IH} = -7 V, V_{CC} = 5 V, other input at 0 V			-0.8		
		V_{IH} = -7 V, V_{CC} = 0 V, other input at 0 V			-0.8		
		V_{IH} = 12 V, V_{CC} = 5 V, other input at 0 V	-55°C to +125°C	02		1	
		V_{IH} = 12 V, V_{CC} = 0 V, other input at 0 V				1	
		V_{IH} = -7 V, V_{CC} = 5 V, other input at 0 V			-0.8		
		V_{IH} = -7 V, V_{CC} = 0 V, other input at 0 V			-0.8		
High level enable input current	I_{IH}	V_{IH} = 2 V	-40°C to +125°C	01	-100		µA
			-55°C to +125°C	02	-100		
Low level enable input current	I_{IL}	V_{IL} = 0.8 V	-40°C to +125°C	01	-100		µA
			-55°C to +125°C	02	-100		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics section - continued							
Supply current	I_{CC}	V_I 0 or V_{CC}, no load, receiver enabled and driver disabled	-40°C to +125°C	01		7	mA
		V_I 0 or V_{CC}, no load, receiver disabled and driver disabled				0.7	
		V_I 0 or V_{CC}, no load, receiver enabled and driver enabled				15	
		V_I 0 or V_{CC}, no load, receiver enabled and driver disabled	-55°C to +125°C	02		7	
		V_I 0 or V_{CC}, no load, receiver disabled and driver disabled				0.7	
		V_I 0 or V_{CC}, no load, receiver enabled and driver enabled				15	
Receiver switching characteristics section							
Propagation delay time, output ↑	t_{PLH}	V_{ID} = -1.5 V to 1.5 V, see figure 8	-40°C to +125°C	01	7	30	ns
			-55°C to +125°C	02	7	30	
Propagation delay time, output ↓	t_{PHL}	V_{ID} = -1.5 V to 1.5 V, see figure 8	-40°C to +125°C	01	7	30	ns
			-55°C to +125°C	02	7	30	
Pulse skew ($t_{PHL} – t_{PLH}$)	$t_{sk(p)}$	V_{ID} = -1.5 V to 1.5 V, see figure 8	-40°C to +125°C	01		6	ns
			-55°C to +125°C	02		6	
Rise time, output	t_r	See figure 8	-40°C to +125°C	01		5	ns
			-55°C to +125°C	02		5	
Fall time, output	t_f	See figure 8	-40°C to +125°C	01		5	ns
			-55°C to +125°C	02		5	

See footnote at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver switching characteristics section – continued							
Output enable time to high level	t_{PZH}	C_L = 10 pF, see figure 8	-40°C to +125°C	01		50	ns
			-55°C to +125°C	02		50	
Output enable time to low level	t_{PZL}	C_L = 10 pF, see figure 8	-40°C to +125°C	01		50	ns
			-55°C to +125°C	02		50	
Output disable time to high level	t_{PHZ}	C_L = 10 pF, see figure 8	-40°C to +125°C	01		60	ns
			-55°C to +125°C	02		60	
Output disable time to low level	t_{PLZ}	C_L = 10 pF, see figure 8	-40°C to +125°C	01		40	ns
			-55°C to +125°C	02		40	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

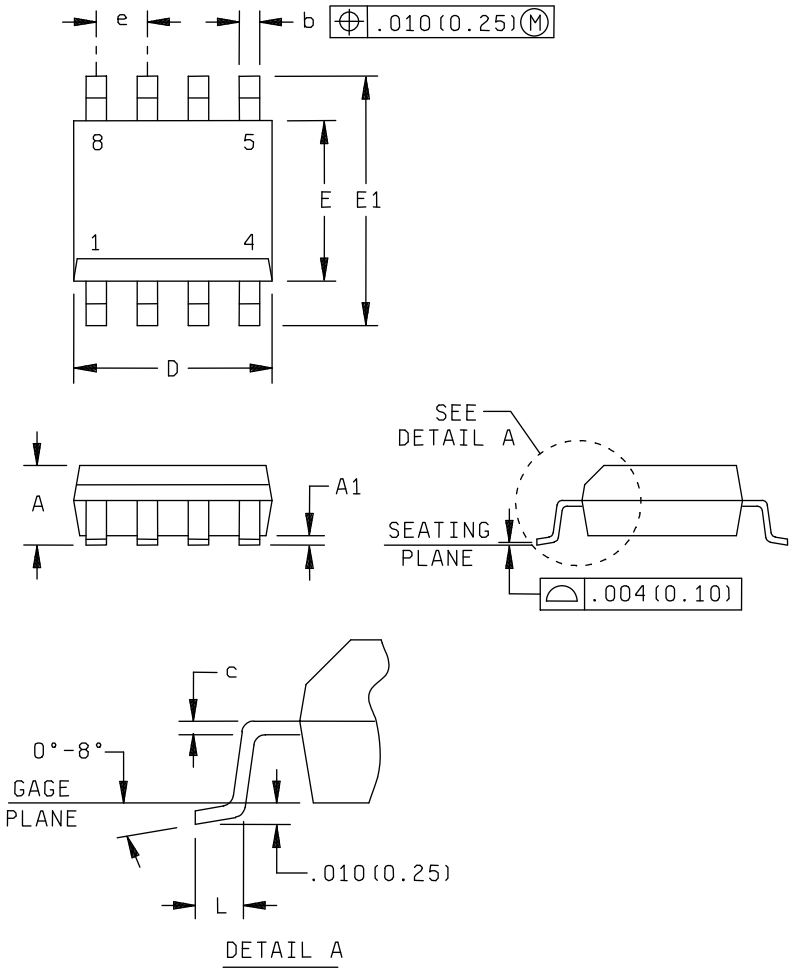


FIGURE 1. Case outlines.

Case X

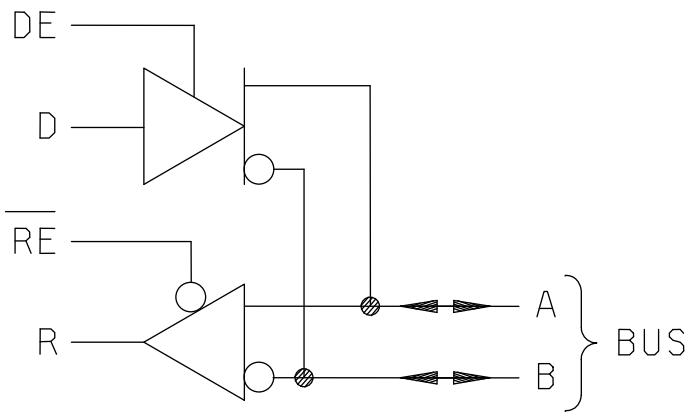
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	.197	4.80	5.00
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
L	0.016	0.040	0.41	1.02
n	8 leads		8 leads	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) each side.
4. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline. – continued.

Device types	01 and 02
Case outline	X
Terminal number	Terminal symbol
1	R
2	$\overline{RE}$
3	DE
4	D
5	GND
6	A
7	B
8	V_{CC}

FIGURE 2. Terminal connections.



Positive logic

DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS $V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq$ -0.2 V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

FIGURE 3. Logic diagram.

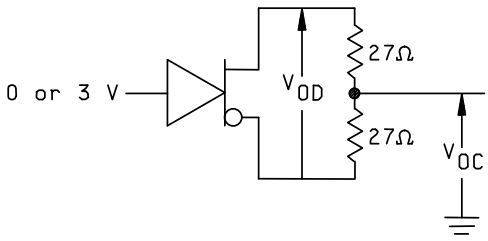


FIGURE 4. Driver V_{OD} and V_{OC} test circuit.

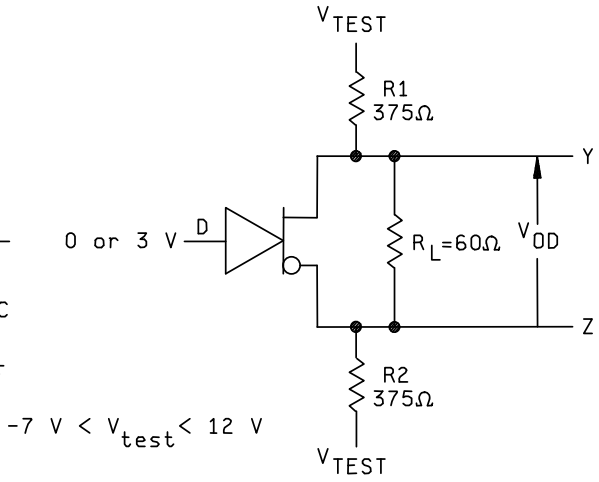
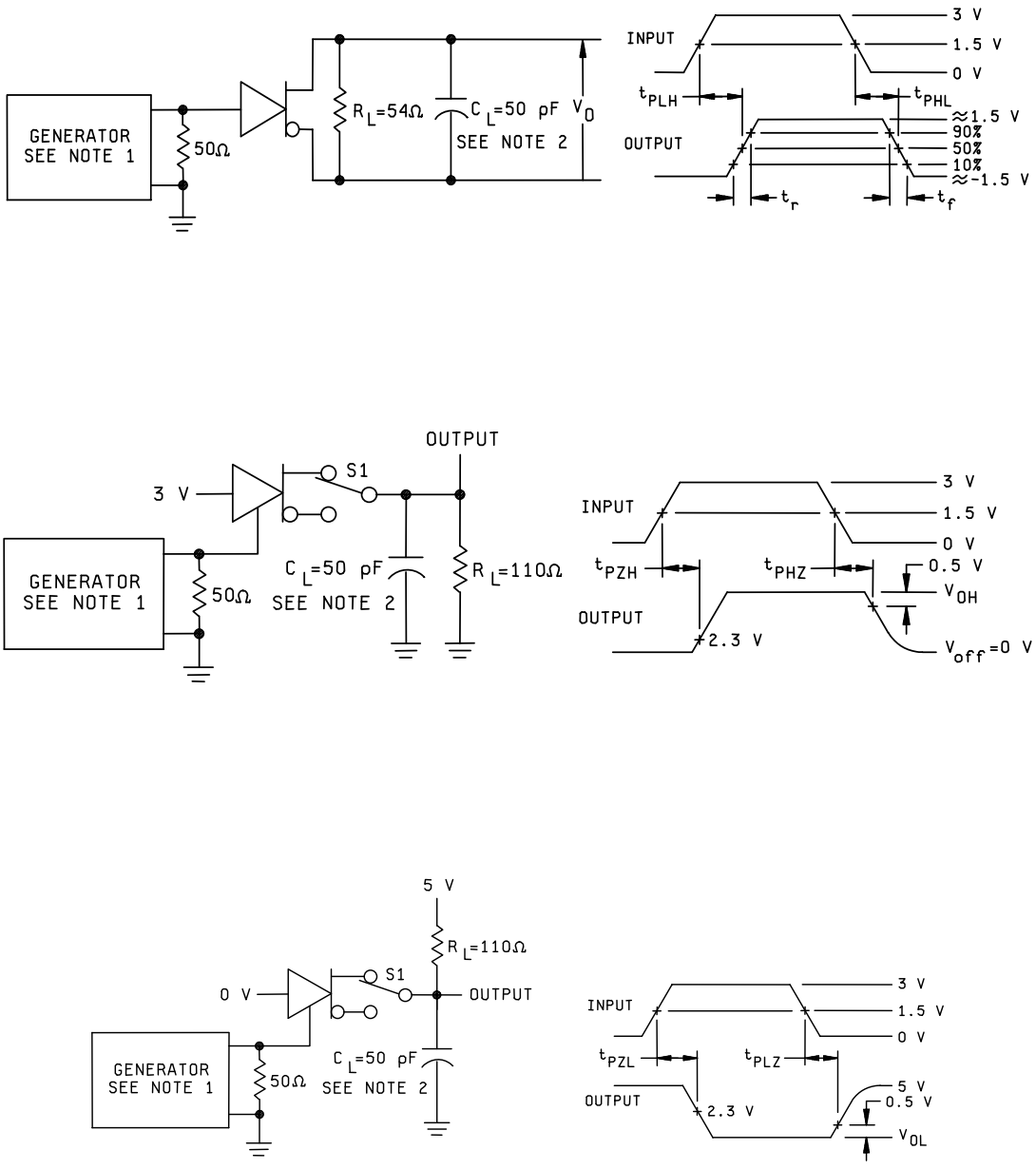


FIGURE 5. Driver V_{OD3} test circuit.



NOTES:

1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50 % duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, and Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

FIGURE 6. Driver test circuit and voltage waveforms – continued.

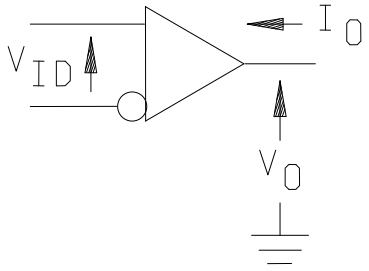
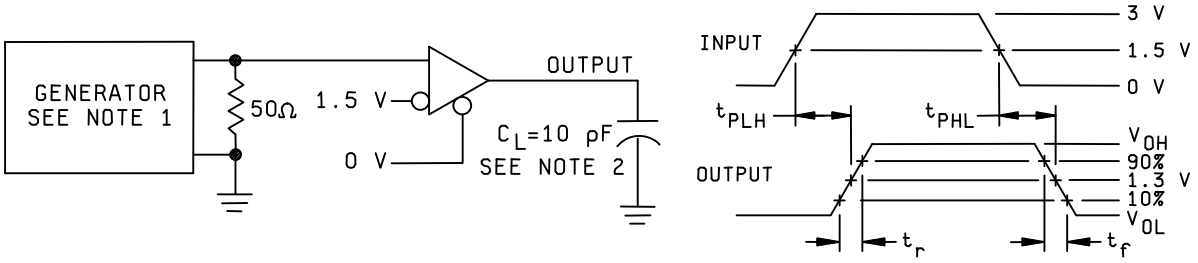
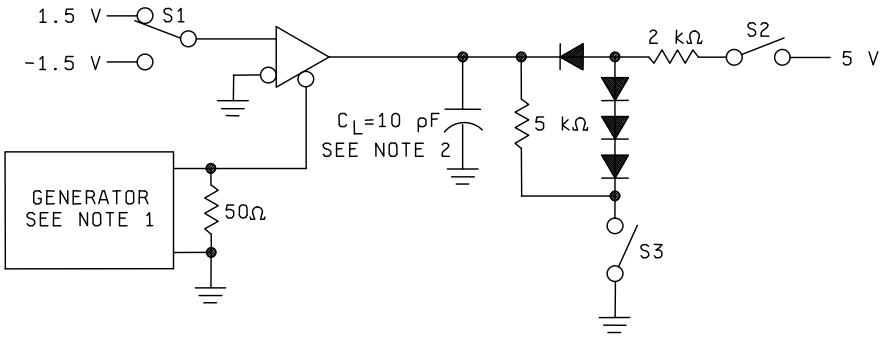


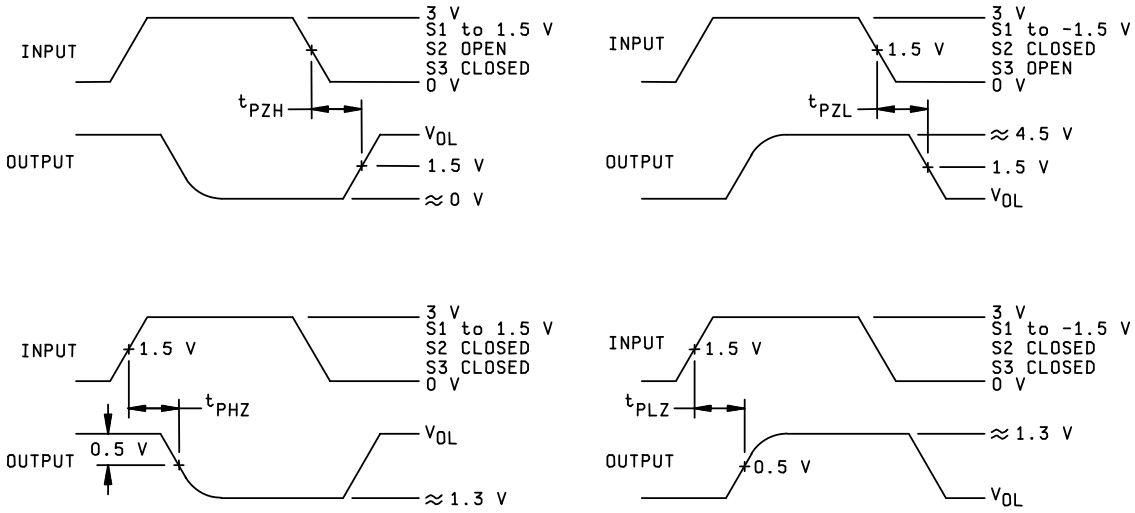
FIGURE 7. Receiver V_{OH} and V_{OL}.



NOTES:
1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50 % duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, and Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

FIGURE 8. Receiver test circuit and voltage waveforms.





NOTES:

1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50 % duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, and Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

FIGURE 8. Receiver test circuit and voltage waveforms – continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/03671-01XE	01295	176AEP	SN65LBC176AQDREP
V62/03671-02XE	01295	176MEP	SN65LBC176AMDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243